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Ultraprecision machining for single-crystal silicon carbide wafers: State-of-the-art and prospectives

Haoxiang WANG, Renke KANG, Zhigang DONG, Shang GAO*

State Key Laboratory of High-performance Precision Manufacturing, Dalian University of Technology, Dalian 116024, China

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Abstract: Silicon carbide (SiC) has a wide range of application prospects for the excellent characteristics. However, its high hardness, brittleness, and chemical inertia improve the processing difficulty, which restricts the popularization and application of single-crystal SiC semiconductor devices. This paper introduces the research progress of SiC from two parts: material removal mechanism and ultraprecision machining technology. The material removal and damage formation mechanism of SiC at home and abroad, as well as the research progress of lapping, polishing technology and ultraprecision grinding technology are introduced in detail. The analysis shows that there are some differences in the removal mechanisms of SiC studied by different scholars. In addition, the lack of a reasonable theoretical model for surface integrity hinders the selection of efficient and low-damage process parameters for grinding SiC wafers. In terms of single crystal SiC ultraprecision machining, the more mature machining methods at this stage mainly go through three steps: double-sided lapping, single-sided lapping and chemical mechanical polishing. The machining efficiency and surface integrity of each step affect the production efficiency and scrap rate of the final product. As SiC wafers develop towards larger sizes, ultraprecision grinding technology, which utilizes workpiece rotation grinding principles, emerges as an efficient and low-damage machining method of SiC wafers, has the potential to replace the traditional lapping.

Keywords: Single crystal SiC; Semiconductor material; Ultraprecision machining; Lapping; Polishing; Grinding

1. Introduction

The computation method of unsteady transonic flow based on N-S equations should be best accurate, but to three-dimensional complex problems, it can be achieved only on large computers, and moreover, the results are not ideal sometimes. [1] A viscous/inviscid interaction method is an applicable one and the computation time can be reduced by two orders.

The manufacturing of semiconductor devices such as integrated circuits, optoelectronic devices, and microsensors is a fundamental, strategic, and pioneering industry vital to the national economy and national security. It has become an important indicator of a country's technological level and comprehensive national strength. [1,2] The production of high-performance semiconductor devices relies on advanced semiconductor materials. In the development history of semiconductor materials, silicon (Si) and gallium arsenide (GaAs) are generally regarded as representatives of the first and second generations of semiconductor materials, respectively. Single-crystal silicon, with its excellent electrical properties and mature manufacturing processes, is widely used in integrated circuit manufacturing; gallium arsenide, with its superior high-frequency performance and photoelectric conversion efficiency, has become an important material for high-frequency and optoelectronic devices. [3] Over the past few years, significant advancements in fields such as new energy vehicles, high-speed rail, and quantum communication has led to an increasing demand for high-performance power devices and RF devices. Silicon carbide (SiC) and gallium nitride (GaN), as third-generation semiconductor materials, are preferred wafers for power devices and radio frequency (RF) devices due to their excellent physical properties such as critical breakdown electric field, high thermal conductivity, high carrier saturation velocity, and high-temperature resistance. [4, 5]

However, the large-size single-crystal growth technology of gallium nitride (GaN) is still immature, with some physical properties difficult to explain reasonably and low industrialization levels. In contrast, SiC wafers has achieved industrialization with 6-inch wafers already in production, and there are currently production lines for 8-inch SiC wafers. Therefore, in the coming years, large-size SiC wafers are expected to become a focal point of attention for wide bandgap semiconductor applications.

Alongside fulfilling the performance criteria of semiconductor materials themselves, the surface and subsurface quality, as well as the processing precision of the wafers, also play a crucial role in determining the operational performance of microelectronic and optoelectronic devices. [6] They must achieve processing quality requirements such as sub-nanometer surface roughness, nanometer-level

* Corresponding author. *E-mail address:* gaoshang@dlut.edu.cn (Shang GAO)
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surface damage depth, and sub-micrometer surface profile accuracy. [7, 8] To meet these high standards, after the single-crystal growth of SiC crystals, a series of complex and delicate processing steps including slicing, grinding, and polishing are necessary to obtain high-precision, ultra-smooth, nearly damage-free SiC wafers. But the hard and brittle nature of SiC poses challenges during the processing process.

Therefore, achieving high-precision and high-quality SiC wafers for high-performance semiconductor device manufacturing has made ultra-precision machining technology of SiC wafers as a hot research topic both domestically and internationally. This paper comprehensively and systematically summarizes the current research status of material removal mechanisms, damage formation mechanisms, process optimization, and other aspects in the processing of SiC wafers. It analyzes the current problems, challenges, and future development trends of manufacturing high-precision, high-quality large-size SiC wafers, aiming to provide guidance for the in-depth research of manufacturing technologies for large-size wide bandgap SiC wafers in the future.

2. SiC wafers processing flow

The manufacturing process of SiC wafers involves multiple steps, including single crystal growth, slicing, planar processing, and polishing, as illustrated in Fig. 1. Typically, the growth of SiC single crystals utilizes methods such as Physical Vapor Transport (PVT), High-Temperature Chemical Vapor Deposition (CVD), and Liquid Phase Epitaxy (LPE). Currently, the PVT method is predominantly used for large-scale industrial production of single crystals SiC. [9] However, the grown SiC single crystal ingots often have irregular shapes with surface protrusions and defects, including polycrystalline defects, especially at the bottom and outer edges of the crystal rod. Therefore, reshaping the SiC crystal ingots is necessary. After reshaping, the SiC crystal ingots are sliced into wafers of a specific thickness using a diamond wire saw [10] and undergo edge beveling to remove corner defects. Subsequently, the wafers are subjected to grinding, lapping, and chemical mechanical polishing (CMP) to achieve planar processing, resulting in high-quality SiC wafers.

3. Material removal mechanisms of SiC wafers

Achieving effective and minimally damaging processing of SiC wafers necessitates systematic study of the material removal mechanisms and the generation and evolution of surface damage during ultra-precision machining. Methods such as indentation or scratch tests, grinding tests, molecular dynamics (MD) simulations, and stress field analytical models are pivotal in exploring how SiC behaves during machining.

3.1. Indentation/scratch/grinding tests

The grinding process of SiC wafers can be considered a complex operation involving multiple abrasive grains on the grinding wheel, each contributing to the cutting action. Analyzing the formation mechanism of surface layer damage during grinding is particularly challenging due to the diverse geometries and dispersed nature of abrasive grains. Exploring the grinding mechanism can be enhanced through indentation/scratch tests conducted between individual abrasive grains and the workpiece. This approach facilitates analysis of the fundamental principles and mechanisms underlying ultra-precision grinding.

Scholars have conducted research on damage characteristics in single-crystal SiC through indentation/scratch tests. Huang et al. [11] conducted in-situ nano-scratch studies on 3C-SiC single crystals. Their findings revealed indicated that plastic removal in 3C-SiC is achieved through dislocation slip, lattice distortion, and polycrystallization. Compared to the <100> direction, the <110> direction showed increased hardness during the scratching process, leading to reduced material removal rates (MRR) and elevated friction coefficients, as depicted in Fig. 2. Meng et al. [12, 13] conducted nano-scratch experiments to study the plastic flow of surface-layer material and the expansion behavior of subsurface cracks in 6H-SiC. The experimental results indicated that when the load was below 7 mN, the chip morphology showed accumulation-shaped chips generated by material plastic flow, and the scratch morphology exhibited ductile scratching. When the load reached 10 mN, crushed particles began to appear in the chips, median cracks showed large-angle deviations, and in regions far from the scratch damage center, crack propagation tended towards basal plane cracking. Micro-cracks close to the scratch surface propagated along slip planes {10-13}, demonstrating that symmetrically distributed subsurface micro-cracks are induced by slip motion, as shown in Fig. 3. Duan [14] studied the interference phenomenon of scratching damage in 6H-SiC at the micrometer scale using simulations and single diamond grain scratching test. They found that performing secondary scratches at the same cutting depth can transition the region originally in a state of plastic removal to brittle removal. This occurs because during scratching, damage such as micro-cracks initiates first in the subsurface, which is difficult to observe on the surface. Multiple scratching actions during grinding can extend these micro-crack damages, eventually exposing them on the surface, leading to brittle removal. Nawaz et al. [15] performed nano-indentation studies

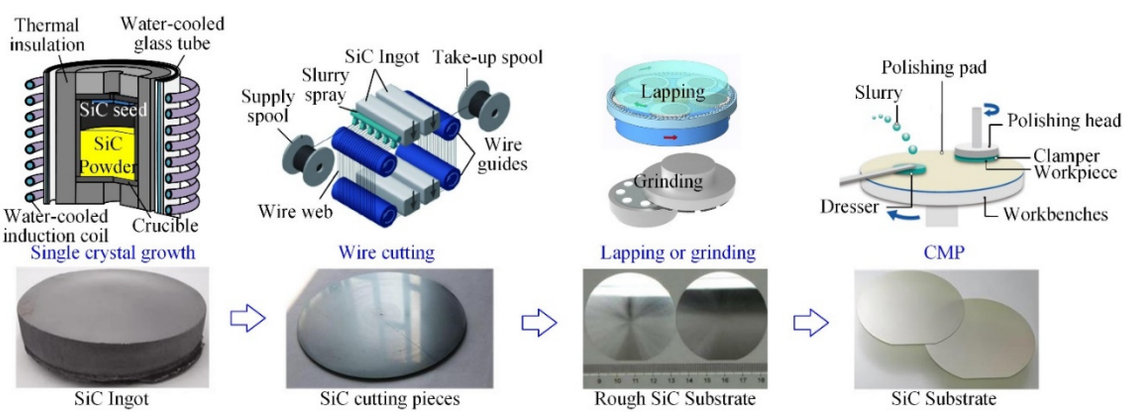

Fig. 1 Manufacturing process flowchart of SiC wafers.

on single-crystal 6H-SiC with a Berkovich indenter. During the experiments, researchers observed no phase transformation and further elucidated the deformation behavior, confirming slip on the primary plane through analysis of critical resolved shear stress and Schmid factor. Yan et al. [16] investigated dislocation motion in 6H-SiC through nano-indentation tests and TEM detection. The results showed that under loading on the (0001) plane, primary basal plane dislocations were primarily extended along the (0001)<1-210> and (0001)<01-10> directions in the subsurface, with cross-slip extending along the {1013}<1-210> and {1010}<1-210> directions. Duan et al. [17] used single diamond abrasives to scratch both the Si-face and C-face of 4H-SiC. They observed that microcutting damage was more prevalent on the C-face, leading to a higher rate of material removal. Hu et al. [18] performed nano-scratch experiments on 4H-SiC using AFM. Their investigation revealed that plastic deformation in 4H-SiC predominantly results from amorphous phase transformation and dislocation slip. Nakashima et al. [19] used a self-developed sliding micro-scratch tester to investigate the evolution of damage in SiC wafers during scratching. The study results showed that during the scratching process, an amorphous phase was first induced, followed by removal of the amorphous layer and initiation of phase separation. This process led to the formation of substances such as quasi-crystalline silicon, graphite, and graphene, as illustrated in Fig. 4.

The load-displacement curve in indentation/scratch tests is an important reference for analyzing material removal characteristics. Yin et al. [20] conducted nanoindentation tests on SiC wafers to investigate the characteristics of brittle-plastic deformation in SiC wafers. The experimental results indicated a size effect in SiC wafers, where the onset of cracks correlates closely with the applied load from the indenter. Before reaching the critical load, no notable cracks are visible; however, upon reaching this threshold, cracks propagate significantly. Cai et al. [21] studied how the coupling effect of dual scratches affects the material removal mechanism in nano-scratch tests. Experimental findings indicated that dual scratches induce increased lateral stress, resulting in overall slippage and material removal. The interaction between dual scratches results in elevated maximum principal stress in lateral cracks, peaking after the indenter is removed. Moreover, the interaction of transverse cracks leads to the general removal of workpiece material and the move-

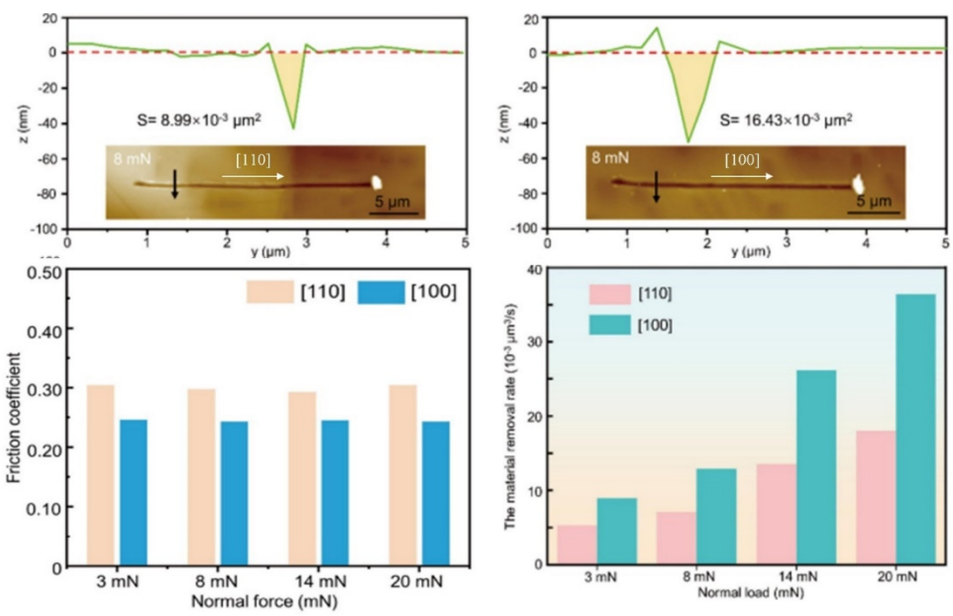

Fig. 2 Anisotropy of friction coefficient and hardness in 3C-SiC.[11]

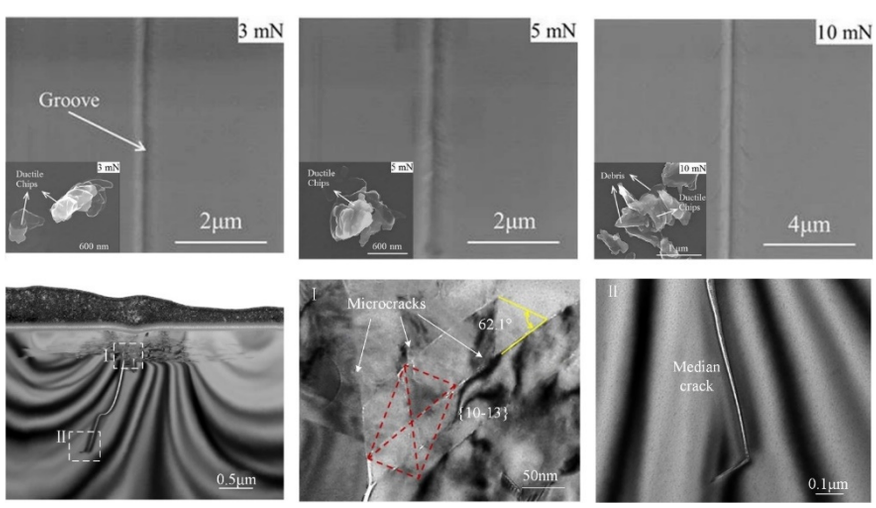

Fig. 3 Morphology of surface and cross-sectional TEM images of 6H-SiC affected by scratching.[12, 13]

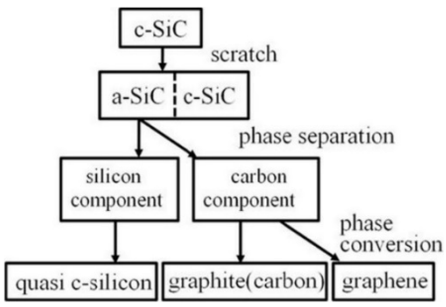

Fig. 4 Phase transformation process in single-crystal SiC.[19]

ment of the secondary scratch, as depicted in Fig. 5. Chai et al. [22] performed nano-scratch tests on 4H-SiC and examined the morphology of the scratched surface using SEM. They categorized the material removal process into three stages: dominated by elasticity, plasticity, and brittleness, as illustrated in Fig. 6. Building on the experiments, they further considered the phenomenon of elastic recovery after scratching and used scratch stress and cleavage strength to estimate the depth at which cutting becomes critical in 4H-SiC. They determined that the critical cutting depth for the brittle-to-ductile transition in single-crystal 4H-SiC is approximately 90 nm. Pan et al. [23] conducted quasi-static indentation experiments on the Si-face and C-face of 6H-SiC using a Berkovich indenter, increasing the load from 1 mN to 500 mN. The results demonstrated distinctive effects of indentation on the morphology of single-crystal SiC, revealing that hardness and elastic modulus gradually increased with greater load and indentation depth, particularly on the C-face. The theoretical critical loads for plastic deformation were 1.941 mN for C-face and 1.77 mN for Si-face, while for brittle fracture, they were 366.8 mN for C-face and 488.67 mN for Si-face.

Through stress analysis, further theoretical insights into the evolution of damage in single-crystal SiC have been uncovered. Zhao et al. [24] performed nanoindentation experiments to investigate the deformation and damage behavior in 3C-SiC. They analyzed the initiation of plasticity and crack initiation behavior based on the stress distribution during indentation and the evolution of damage. The results indicated that the first Pop-in indentation depth was 60 nm, corresponding to a shear stress of 39.3 GPa, which exceeds the critical shear strength of 3C-SiC (34.2 GPa), suggesting that the initial plasticity in 3C-SiC originates from shear action. Combined with subsurface TEM observations from scratch tests, it further illustrated that shear bands predominantly govern the deformation process in 3C-SiC, where the intersections of these bands initiate crack formation, as depicted in Fig. 7.

The above research results have deepened our understanding of the machining behavior of single crystal SiC materials, providing valuable experimental data and theoretical foundations for further understanding their mechanical properties and material behaviors. However, the cross-scale characteristics of single-grain scratching and grinding still require more attention and exploration in comprehensive studies to fully understand the machining characteristics of single crystal SiC materials.

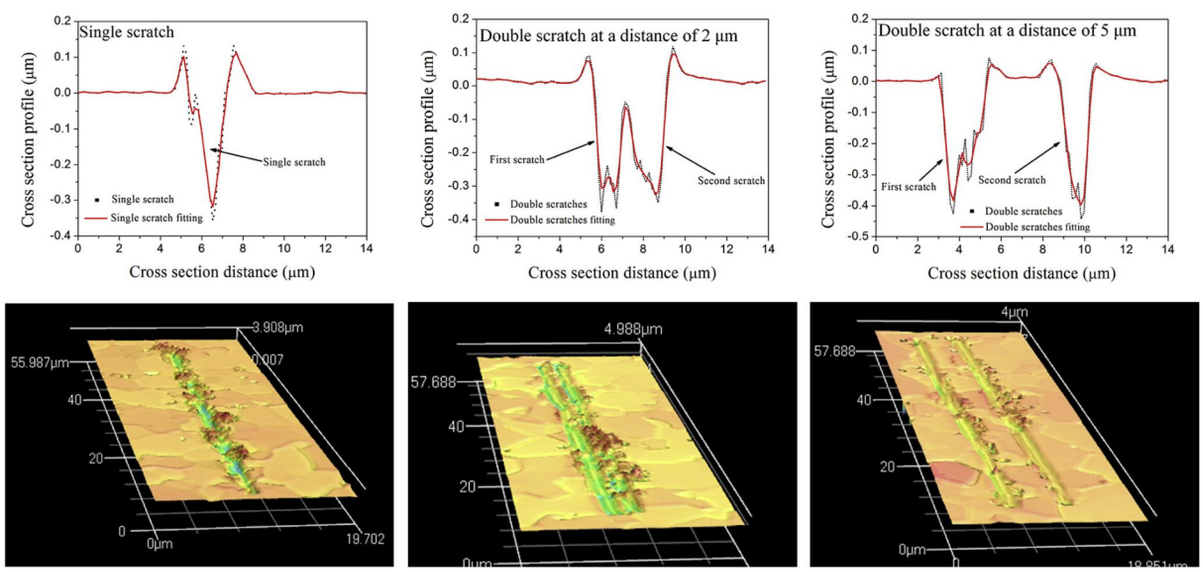

Fig. 5 Cross-sectional profile of nano scratch grooves.[21]

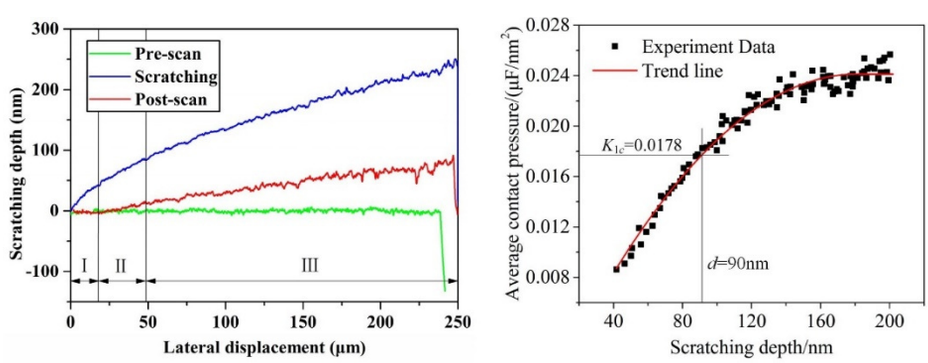

Fig. 6 Scratch depth and contact pressure at different material removal stages in 4H-SiC.[22]

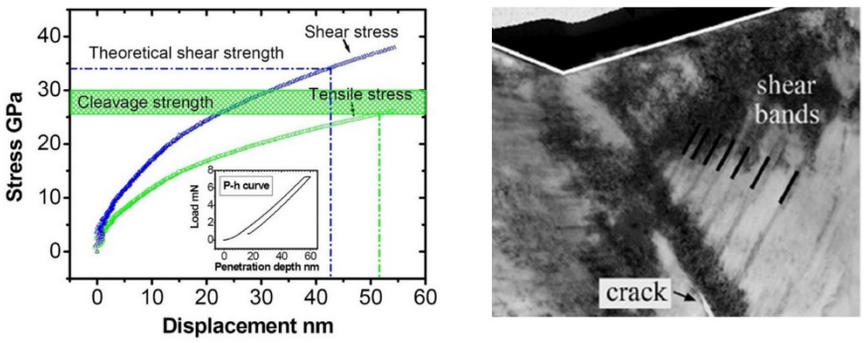

Fig. 7 Mechanisms of plastic deformation and crack formation in 3C-SiC.[24]

Although nano-indentation/scratch tests are effective methods for studying grinding mechanisms, the scratching speed in scratch experiments is several orders of magnitude smaller (10^3 to 10^6) compared to actual grinding speeds. This large difference in strain rates undermines the reliability of the results. To further elucidate the removal mechanisms of SiC wafer, grinding experiments are the most direct approach.

Currently, there is limited research on grinding experiments focused on the material removal mechanisms of SiC wafers. Most studies involve detecting surface and subsurface damage after grinding. Tsukimoto et al. [25] examined the crack distribution and dislocation slip behavior within the damaged subsurface layer of single-crystal SiC wafers using TEM. Their study revealed areas with significant damage and notable undulations beneath the surface post-grinding, where both median and radial cracks reached the depths of the defect regions, as illustrated in Fig. 8. Additionally, basal plane dislocations and their extended stacking faults were generated by the sliding of microcracks, forming basal plane dislocation-slip regions, as indicated in the area between the red and blue dashed lines in Fig. 8. Agarwal and Rao [26] studied the efficient grinding of SiC wafers, concentrating on the removal process and key grinding parameters. Their findings suggest that increasing the MRR does not impact surface texture or appearance.

Overall, studies on single-grain indentation/scratch tests and grinding experiments provide direct evidence for elucidating the removal mechanisms of SiC wafers. However, there is still an insufficient understanding of the material damage evolution process.

3.2. MD simulation

MD simulation is an effective method for studying the interactions between atoms, providing a deep understanding of deformation and material removal on an atomic level. This approach is widely employed to investigate how materials are removed during mechanical processing [27, 28]. By simulating the dynamic behavior of atoms and molecules, MD offers in-depth insights into the microscopic deformation and removal mechanisms of materials during processing.

Investigating how single-crystal SiC undergoes plastic deformation is a key area of focus in MD simulations. Szlufarska et al. [29] used MD simulations to explore the amorphization process of 3C-SiC, uncovering that dislocation loops expanding and merging lead to the transition from single-crystal to amorphous states. Sun et al. [30] employed MD simulations to investigate how prismatic dislocation loops form in 3C-SiC. Their findings demonstrated that these loops can originate from either a single shear loop or two separate shear loops, as depicted in Fig. 9. Mishra et al. [31] employed MD simulations to investigate dislocation dynamics in 3C-SiC. They observed that at a depth of 1.5 nm, dislocations undergo slip and cross-slip mechanisms. Deeper cuts, beyond 3.5 nm, lead to the formation of "V-shaped" dislocation half-loops within the contact deformation zone, as illustrated in Fig. 10. Zhu et al. [32] utilized MD simulations to explore the behavior of 3C-SiC under nanoindentation, uncovering insights into its structural deformation and directional dependencies. The study showed that indentations on the (010), (110), and (111) surfaces exhibited different symmetries, as illustrated in Fig. 11. High shear stress initiated the formation and spread of dislocations, facilitating stress dissipation across the sample. During plastic deformation, dislocations developed from initial forms to organized bands, culminating in the creation of prismatic dislocations. Liao et al. [33] explored the mechanisms of elastoplastic recovery in single-crystal 3C-SiC under fatigue unloading. Their findings highlighted variations in the formation and evolution of dislocation loops depending on the indenter size. Moreover, the hemispherical indenter exhibited an ultimate yield stress of 3.82 GPa and an ultimate strain of 1%, while the right quadrangular pyramid indenter demonstrated an ultimate yield stress of 6.60 GPa and an ultimate strain of 1.5%. Zhu et al. [34] studied the impact of shear stress on phase transformation in 4H-SiC using MD simulations. Higher shear stress promoted transformation from 4H-SiC to 3C-SiC. A shear stress of approximately 9 GPa induced the formation of a 3C-SiC layer, while about 12 GPa led to the formation of 3C-SiC grains, depicted in Fig. 12. Wang et al. [35] used MD simulations to explore the differences in damage behavior during plastic deformation among the three crystal structures of SiC. The results

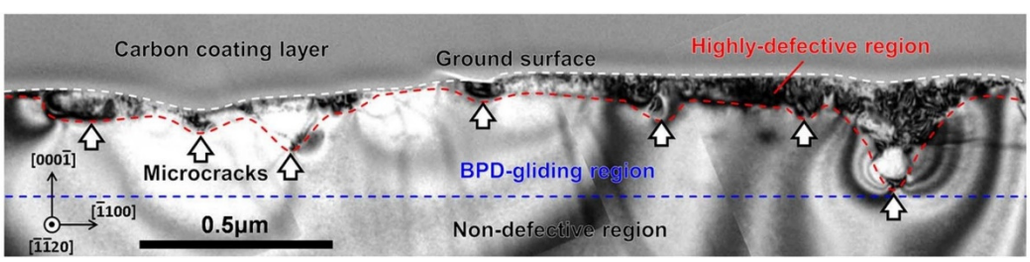

Fig. 8 4H-SiC (0001) cross-sectional TEM images showcasing the subsurface region.[25]

showed that all three crystal forms of SiC underwent an amorphous phase transformation during plastic deformation. For 3C-SiC, full dislocations first appeared in the subsurface and glided along the {111} planes. When the full dislocations reached the surface, they tapered at both ends and coalesced, eventually forming an individual loop of dislocations, separating from the affected surface. In 4H- and 6H-SiC, full dislocations were distributed on (0001) plane, while partial dislocations were distributed on the (0001) and {1-100} planes, with dislocation glide mainly occurring on the basal plane.

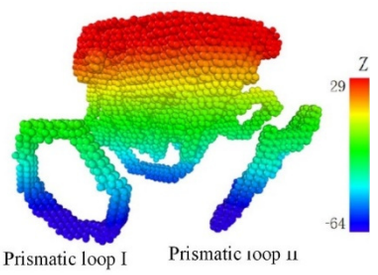

Fig. 9 Mechanisms behind the formation of prismatic dislocation loops in 3C-SiC.[30]

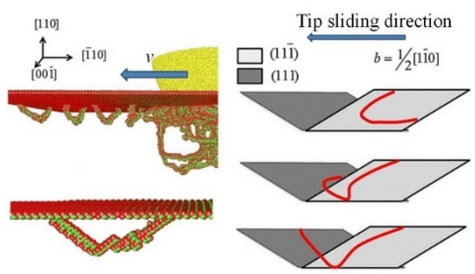

Fig. 10 Dislocation motion in 3C-SiC during nano-cutting.[31]

Furthermore, MD simulations are applicable for investigating the material removal mechanisms involved in abrasive machining of single-crystal SiC. Luo et al. [36] analyzed diamond abrasive interactions with 6H-SiC wafer surfaces in ultra-precision polishing using MD simulations. Their focus was on the impact of varying cutting depths and abrasive front angles on material removal. The findings indicated that deeper cutting depths tended towards brittle removal, while the abrasive front angle showed negligible influence on the removal process. Noreyan et al. [37] explored the mechanical behavior of 3C-SiC during scratching using MD simulations. Their findings revealed anisotropic scratch hardness and friction coefficients, with higher values observed on the <110> crystal orientation compared to <100>. Gao et al. [38] utilized MD simulations to investigate nano-grinding of 4H-SiC, focusing on atomic-scale damage evolution mechanisms. Their study revealed that plastic deformation initially arises from amorphization and dislocation nucleation. With increasing abrasive cutting depth, subsurface slip bands develop, leading to the initiation and propagation of cracks, as depicted in Fig. 13. Wu et al. [39] employed MD simulations to investigate how material anisotropy affects single-grain scratching of 6H-SiC. They identified the (0001) <1$\bar{1}$00> orientation as the plane of least resistance to machining, showing the shallowest subsurface damage after scratching. In contrast, the (11$\bar{2}$0) <0001> orientation exhibited the deepest subsurface damage and poorest scratch quality, illustrated in Fig. 14. Xiao et al. [40, 41] explored how 6H-SiC behaves under scratching using MD simulations. They found that dislocation motion and high-pressure phase transformations predominantly govern plastic deformation in 6H-SiC, with dislocation motion particularly influential in inducing a shift towards a rock-salt structure during cutting, depicted in Fig. 15. With increasing undeformed chip thickness, the material removal process transitions from ductile to brittle, as illustrated in Fig. 16. Zhou et al. [42] used MD simulations to investigate the mechanical removal process of SiC wafers during fixed abrasive polishing. They found that the height and distribution pattern of abrasives significantly impact the material removal process of SiC wafers. Specifically, the random distribution of abrasives adversely affects the quality of the polishing process.

In summary, there is ongoing debate and no consensus on the plastic deformation and removal mechanisms of SiC materials. Research on crack initiation and evolution in single-crystal SiC remains constrained by modeling scale and computational costs. Future studies should delve deeper into the micro-mechanisms of single-crystal SiC to reveal essential aspects of elastic and plastic deformation, material removal, and crack behavior. This exploration promises to enhance understanding and practical utilization of SiC materials.

3.3 Stress field analysis models

Stress field analysis models are theoretical frameworks that use mathematical methods to describe the distribution of stresses during abrasive scratching processes, providing a basis for predicting stress distribution and evolution. These models integrate considerations of elastoplastic behavior, material mechanical properties, and grinding parameters. By enhancing the understanding of crack initiation and propagation mechanisms during scratching processes, these models can guide the optimization of grinding processes.

Wang et al. [43] developed a model in cylindrical coordinates to predict stress distribution in brittle material scratching processes. Combining experimental results from scratching tests, it was shown that during the process, initial median cracks are followed by lateral cracks originating in the plastic yield region and propagating to the surface, facilitating material removal, as depicted in Fig. 17. Yang et al. [44-46] utilized stress field theory to analyze the coupled ef-

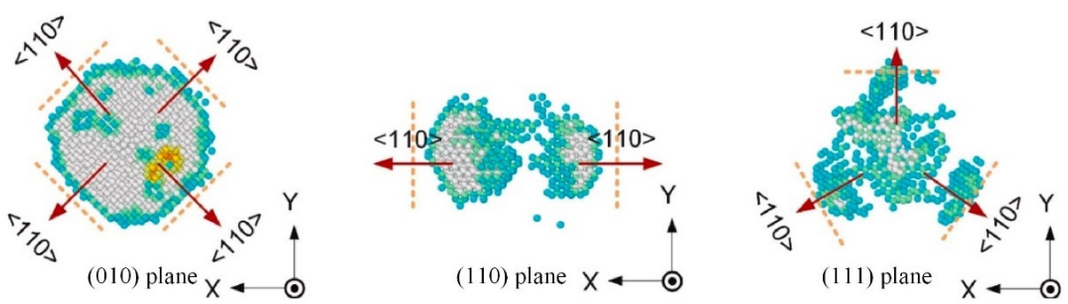

Fig. 11 Symmetry observed in nanoindentation on various crystal planes of 3C-SiC.[32]

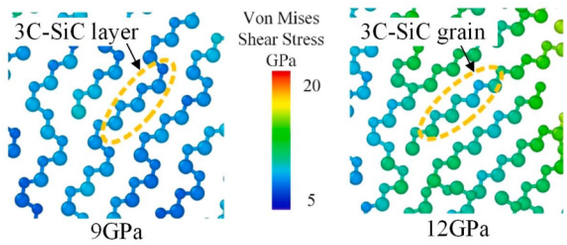

Fig. 12 Formation conditions of 3C-SiC grains and layers under varying shear stress.[34]

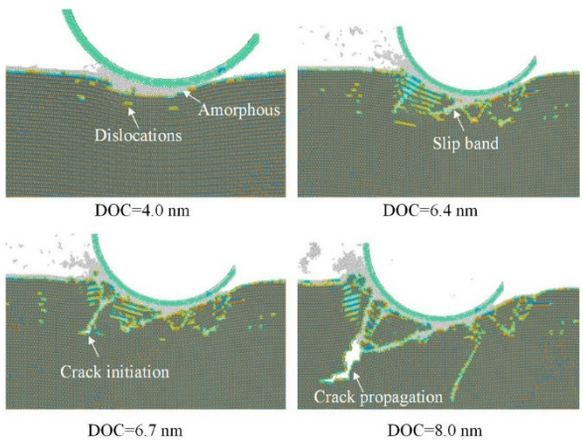

Fig. 13 Formation Mechanisms of Subsurface Damage in Nano-Grinding of 4H-SiC.[38]

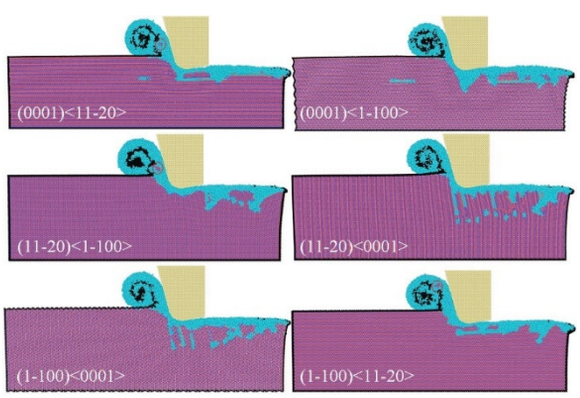

Fig. 14 Surface and subsurface damage in 6H-SiC under single-grain scratching.[39]

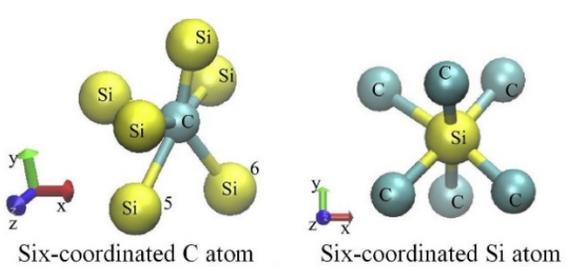

Fig. 15 Phase transformation in 6H-SiC during scratching.[40]

fects of dual scratching and, through nano-scratching experiments, revealed the material removal mechanisms during glass ceramic scratching processes. Zhang et al. [47] combined stress field models, nano-scratching experiments, and MPM simulations to reveal the mechanisms of abrasive particle-induced damage evolution in single-crystal SiC during scratching. The results indicate that the sides of the abrasive particle are prone to cracking under tensile stress, while the front end of the particle and the edge of the scratch groove are primarily affected by compressive stress, leading to plastic flow, as shown in Fig. 18. Additionally, abrasives with a large front angle induce greater tensile stress intensity, while those with a small front angle are more likely to cause cracks perpendicular to the groove.

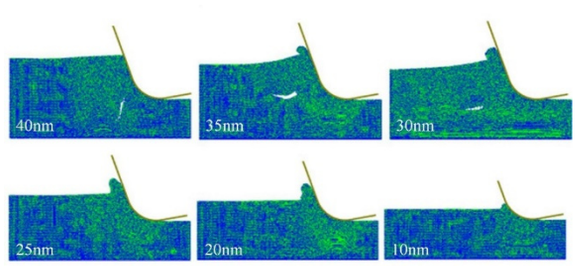

Fig. 16 Ductile and brittle material removal in 6H-SiC at different cutting depths.[41]

In a word, the stress field analysis model is a powerful method for predicting susceptible cracking zones in processing brittle materials, but it is not suitable for studying crack propagation. Therefore, further research is needed on the stress principles governing crack propagation in single-crystal SiC.

3.4 Issues in mechanism research

Current literature analysis indicates that the mechanisms of material removal and damage evolution in single-crystal SiC are not fully elucidated. The prevailing view suggests that the plastic deformation of SiC involves coupled behaviors such as amorphization and dislocation slip. However, debates continue regarding whether phase transformation occurs in single-crystal SiC and which phases are involved. Furthermore, stress field analysis models can only assist in predicting the potential locations of crack initiation but cannot reveal the crack propagation mechanisms in single-crystal SiC.

4. Ultra-precision machining process for SiC wafers

Monocrystals SiC exhibit extreme hardness and brittleness, coupled with chemical inertness, which greatly limits their applications. Typically, SiC wafers are planarized through lapping and polishing processes. [48] Initially, SiC wafers are lapped to achieve certain parallelism and uniformity, followed by polishing to remove residual defect layers from the grinding process. In recent years, ultra-precision grinding technologies have been widely applied in the flattening and back-thinning processes of hard and brittle semiconductor wafers [49], showcasing significant potential in SiC monocrystal processing. The following sections will discuss the current research status of lapping, polishing, and ultra-precision grinding technologies in the ultra-precision processing of SiC monocrystals.

4.1. Lapping

Lapping of single crystal SiC typically involves two steps: double-side lapping and single-side lapping. Double-side grinding achieves required parallelism and uniformity, while single-side grinding further reduces surface defects left from double-side grinding, thereby enhancing CMP efficiency.

To study the impact of double-side lapping on the surface damage layer of SiC wafers, Zhou et al. [50] utilized the Hill model incorporating ideal material porosity expansion to investigate the impact

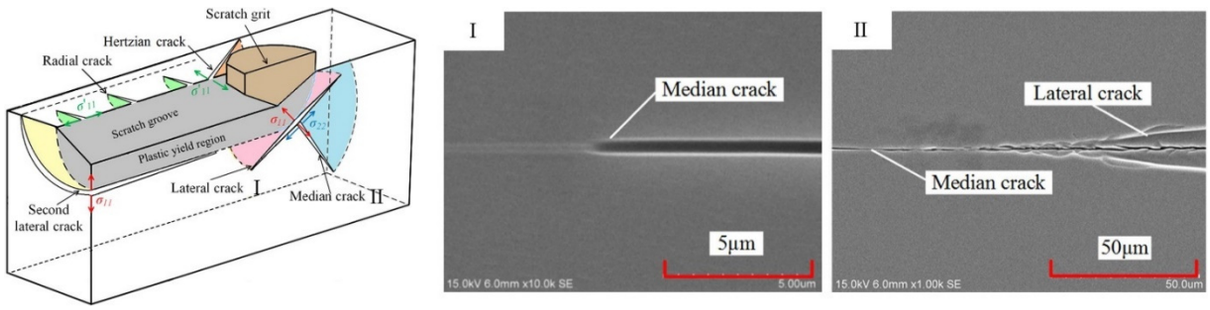

Fig. 17 Scratch crack system and experimental verification.[43]

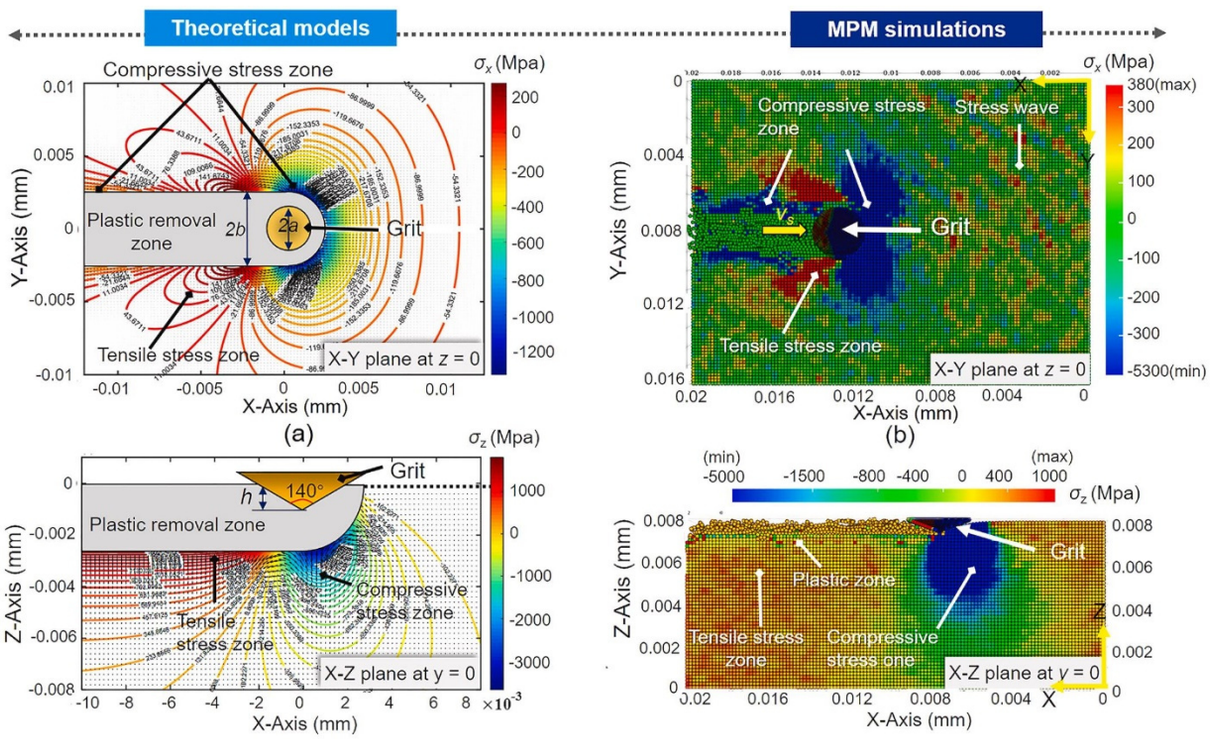

Fig. 18 Stress distribution under different front angle abrasive scratches.[47]

of double-sided grinding on surface damage of SiC wafers. This model correlates microcrack depth and scratch depth in the double-sided grinding of SiC wafers. Yu et al. [51] designed a novel hard honeycomb-structured lapping pad, as shown in Fig. 19. The honeycomb structure is filled with diamond abrasive in a soft gel, serving a semi-fixed grinding function. They conducted double-sided lapping experiments using two types of SiC crystals with the new grinding wheel. The lapped wafers exhibited surface roughness ranging from 75 to 125 nm. Hu et al. [52] conducted comparative experiments between ultrasonic vibration-assisted lapping and conventional lapping on single-crystal SiC. The results showed that the addition of ultrasonic vibration increased the MRR but also resulted in deteriorated surface roughness.

From the literature reviewed, it is clear that the surface/subsurface damage and surface roughness of SiC wafers after double-side lapping still exceed 0.1 μm, which falls short of meeting the semiconductor industry's application standards. Therefore, subsequent steps involving single-side lapping and polishing are essential to further reduce the damage. Single-side lapping is used to minimize residual defects from double-side lapping, thereby improving the efficiency of CMP processing. Thus, single-side lapping plays a crucial role in the flattening process. Hu et al. [52] conducted experimental research on ultrasonic-assisted single-side grinding of single-crystal SiC wafers. They utilized grey relational analysis to study the effects and optimization of ultrasonic-assisted lapping. They proposed multi-response optimization of lapping parameters and employed the Grey Taguchi method to maximize MRR and minimize surface roughness. Based on the above, the MRR of current single crystal SiC wafer grinding is low, and there is still a significant damage layer that needs subsequent polishing for removal.

4.2 Polishing

After lapping, the SiC wafers still exhibit a certain thickness of damage layer, requiring subsequent polishing to achieve nearly damage-free SiC wafers. Chemical Mechanical Polishing (CMP) is widely employed in semiconductor wafer fabrication for achieving flat surfaces. It involves using a polishing slurry that interacts chemically with the material, facilitating easier material removal and enhancing surface quality.

Shi et al. [53, 54] studied the CMP process of (0001) surfaces of 4H- and 6H-SiC using colloidal SiO2 polishing slurry. Experimental results indicated that large-sized SiO2 abrasives achieved high MRR but poor surface quality, while small-sized SiO2 abrasives had lower planarization efficiency but better surface quality. Zhou et al. [55]

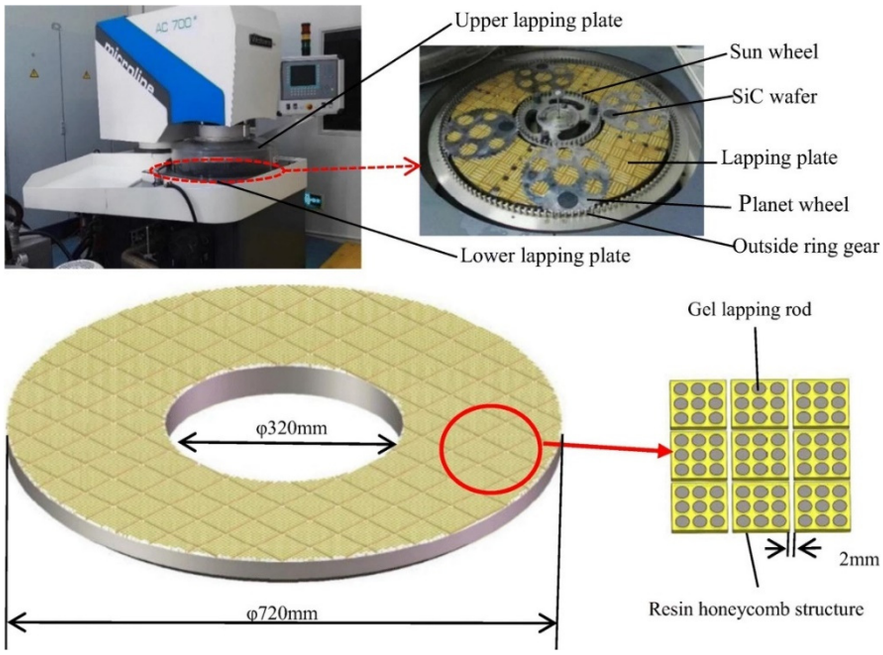

Fig. 19 Using hard honeycomb-structured grinding wheel for grinding operations.[51]

proposed incorporating catalyst nanoparticles into the CMP slurry for processing 4H-SiC wafers on Si-face to enhance MRR and achieve highly smooth surfaces without defects. The results showed that this catalyst could induce oxidation reactions of SiC by activating *OH hydroxyl radicals generated from hydrogen peroxide, achieving efficient removal. Surface measurements indicated atomic-level step structures and Ra = 0.05 nm surface roughness across the entire SiC wafer, as shown in Fig. 20.

In addition to CMP, scholars both domestically and internationally have developed new polishing technologies, such as electrochemical mechanical polishing (ECMP), laser-assisted polishing (LAP), and ultraviolet-assisted polishing (UAP). These technologies primarily employ external energy sources such as electrochemical energy and radiation to induce surface oxidation of SiC wafers, creating an altered layer that facilitates subsequent removal. This approach reduces the damaging effects of abrasives on SiC wafer.

Yang et al. [56] introduced slurry-free ECMP for sliced wafers, depicted in Fig. 21. This innovation optimizes anodic oxidation and polishing performance separately, potentially enhancing efficiency. By avoiding slurries and strong chemicals, it offers environmentally friendly SiC polishing. The method uses #8000 cerium oxide ceramic abrasive in sodium chloride solution at 10 mA/cm² for 2 hours to achieve scratch-free mirror surfaces, reducing Sq roughness from 286 nm to 1.352 nm. Cerium oxide proved optimal for ECMP of 4H-SiC, achieving atomic-level smoothness (Sq = 1-2 nm) and a high MRR of 23 μm/h, with minimal residual oxide. ECMP effectively delivers damage-free, flat 4H-SiC surfaces, confirmed by spectroscopy, showcasing superior quality over conventional methods. These results highlight how non-slurry ECMP enhances MRR, reduces costs, and simplifies SiC manufacturing.

Kim et al. [57] proposed LAP, combining CO2 laser with conventional polishing, as shown in Fig. 22. It enhances SiC wafer MRR via: (1) typical polishing controlled by Preston's equation, involving mechanical wear; (2) laser-induced cracks and surface oxidation reducing local hardness, facilitating material removal; (3) stress corrosion trapping abrasives in cracks, enhancing contact area. Comparative experiments (N/P, CO/P, C/P, N/LAP, CO/LAP) on untreated SiC, laser-induced cracked SiC in argon and air with oxi-

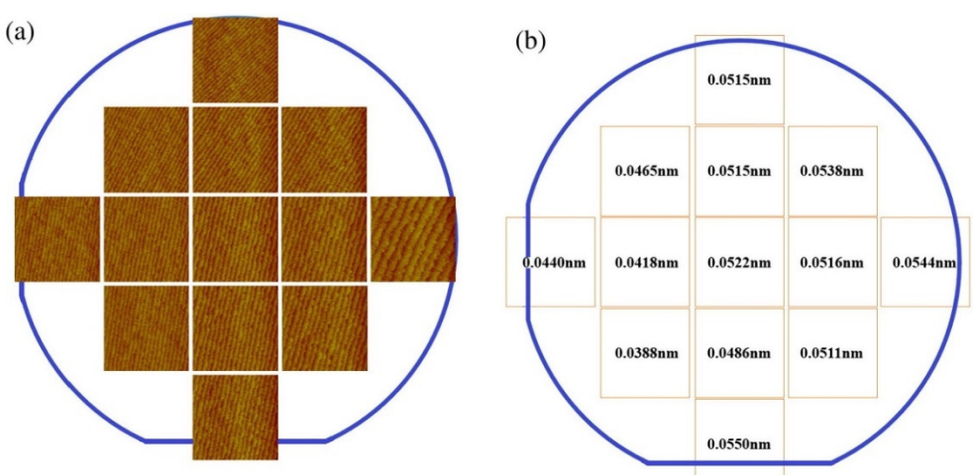

Fig. 20 Surface measurement results of CMP process on 4H-SiC wafer using catalyst nanoparticles.[55]

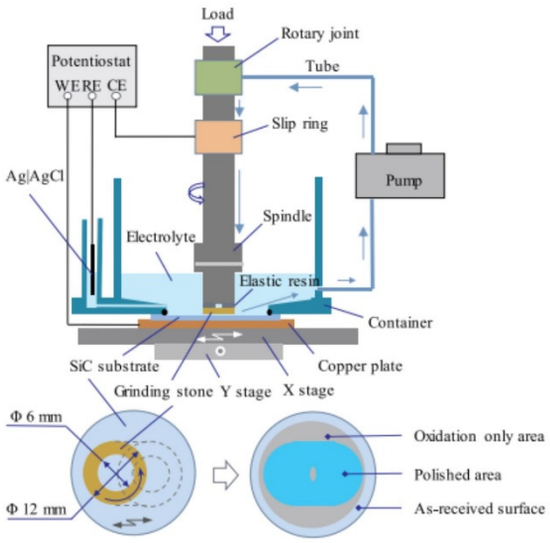

Fig. 21 Schematic of slurry-free ECMP.[56]

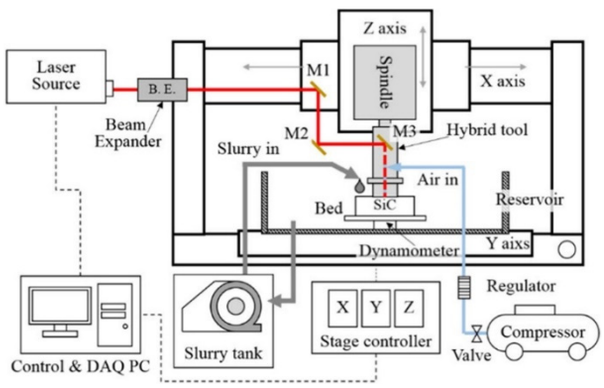

Fig. 22 Schematic diagram of LAP process principle [57]

dation showed LAP increased MRR by 79.0% versus mechanical polishing. Laser-induced cracks were key to LAP's efficiency.

UAP refers to a polishing method that uses a polishing solution composed of photocatalysts and abrasives under UV irradiation conditions [58-63], as shown in Fig. 23. UV-induced electron-hole pairs generate •OH from H2O near SiC wafers, enhancing surface oxidation efficiency and MRR. Tsai et al. [63] introduced catalytic etching mechanical polishing (CEMP) with TiO2-graphene solution under UV, improving SiC sample surface quality and MRR compared to conventional CMP.

However, traditional CMP processing is still used for single-crystal SiC in industrial production, resulting in very low MRR. New polishing technologies, on the other hand, have low processing stability, and their material removal mechanisms are not yet fully understood. Additionally, the high cost of equipment development means these methods currently lack economic value in practical applications.

4.3 Ultraprecision grinding

Lapping causes significant surface/subsurface damage depth on SiC wafers, increasing the duration of subsequent lapping processes, and controlling the shape accuracy of large wafers is difficult. Ultra-precision grinding technology, utilizing workpiece rotation as depicted in Fig. 24, offers several advantages including high abrasive efficiency, cost-effectiveness, precise processing capabilities, and process automation feasibility. Unlike lapping, it minimizes damage depth, reduces polishing time, and lowers overall costs. While it has replaced lapping for large silicon wafers, its application in SiC wafer processing remains relatively underexplored.

Ultra-precision grinding technology relies on high-performance grinding equipment. Currently, Japan's DISCO and ACCRETECH companies hold a leading market position in the field of ultra-precision grinders and specialized high-performance grinding wheels for ultra-hard semiconductor wafers. The DFG8830 ultra-precision grinder developed by DISCO has three rough grinding spindles and one fine grinding spindle, supporting up to 6-inch SiC wafers, as shown in Fig. 25.[64] To ensure the grinding efficiency and processing quality of SiC wafers, ACCRETECH has equipped its SiC wafer grinders with high-rigidity spindles. They have developed the HRG200X and HRG300 high-rigidity grinders, suitable for the grinding of 8-inch and 12-inch SiC wafers, respectively, as shown in Fig. 26. These grinders can achieve a TTV less than 3 μm and an inter-wafer thickness deviation less than ±3 μm for SiC wafers.[65, 66]

In recent years, domestic efforts have begun to develop specialized equipment for ultra-precision grinding of semiconductor wafers. For ultra-precision grinding of new-generation wafers like SiC, domestic companies have gradually developed ultra-precision grinders for SiC wafers. Examples include the TFG-3200 grinder developed by Beijing TSD Equipment Manufacturing Co., Ltd. [67], the CMG200 grinder from the Semiconductor Advanced Manufacturing Innovation Center in Wuxi [68] and the MX-SSG grinder by Suzhou MAXWELL Technology Co., Ltd. [69]. These grinders feature a dual-spindle, three-station structure capable of processing up to 8-inch SiC wafers, as shown in Fig. 27.

Currently, in the field of ultraprecision SiC wafer grinders, although foreign companies have certain advantages over domestic ones, there is no dominant player yet, making it a key competitive area for both domestic and international enterprises in the future. Despite the advantages of diamond grinding wheels such as high grinding efficiency, long service life, and high processing accuracy, they inevitably cause damage, such as microcracks and scratch grooves. To improve the surface integrity of SiC wafers after grinding, scholars have conducted experimental studies on ultra-precision grinding processes for single crystal SiC wafers and modeling of surface integrity prediction.

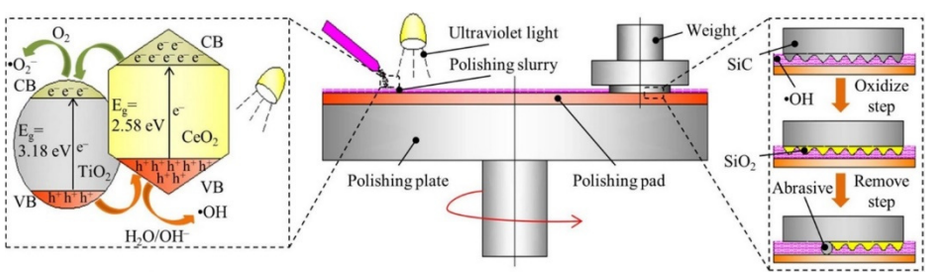

Fig. 23 Processing principle of UAP [58]

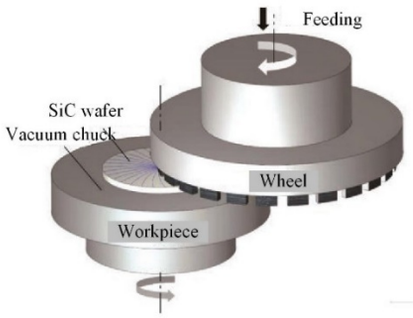

Fig. 24 Ultra-precision grinding technology employs workpiece rotation method

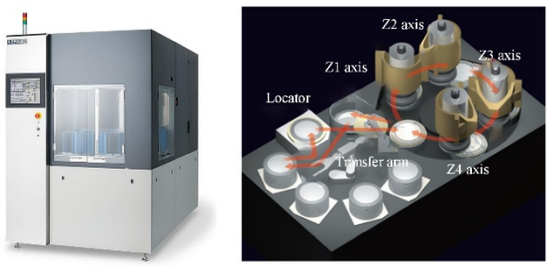

Fig. 25 DFG8830 SiC wafer grinder by DISCO.[64]

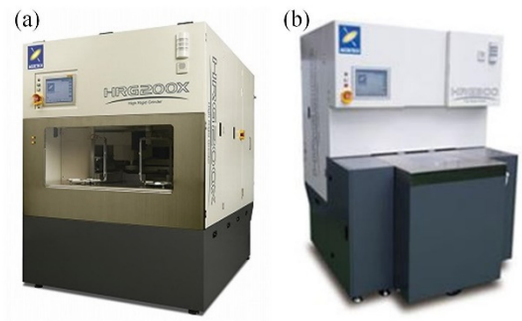

Fig. 26 SiC wafer Grinder by ACCRETECH: (a) HRG200X, (b) HRG300.[65, 66]

Through process experiments, systematic improvements can be made to the grinding process of SiC wafers, enhancing surface integrity and processing quality. Huo et al. [70] utilized fine-grained grinding wheels for nano-grinding SiC wafers, achieving smoother wafers with lower subsurface damages compared to traditional techniques at higher MRR. Grinding test results demonstrate that SiC wafer surface roughness can reach as low as 0.42 nm post-nano-grinding. Yan et al. [71] investigated damage in 6H-SiC under varied grinding conditions, identifying dominant slip systems: (0001)<1-100> and (0001)<11-20>. They found <1-100> orientation more susceptible to cleavage. Experimental findings (Fig. 28) depict surface/subsurface morphologies. Large grinding depth generates numerous crushing pits and extensive median/lateral cracks, indicating brittle fracture. With reduced grinding depth, crushing pit size diminishes, plowing scratch furrows narrow, shifting from brittle to plastic removal, thereby lowering surface roughness. Gopal et al. [72] explored the impact of abrasive grain size and grinding parameters on material removal rate (MRR) through variance analysis. They developed mathematical models to predict surface roughness and defect quantities based on their findings.

To achieve precise control over the surface integrity of SiC wafers after grinding and reduce the damage caused by abrasive grains to the surface/subsurface, some scholars have conducted predictive modeling of surface integrity in grinding of SiC wafers. Accurate prediction and control of surface integrity provide theoretical foundations for guiding ultra-precision grinding of SiC wafers. Current research focuses primarily on modeling aspects such as grain depth of cut, surface roughness, and depth of subsurface damage.

Grain depth of cut, also known as undeformed chip thickness, denotes the thickness of material typically removed from the workpiece surface by active abrasive particles during grinding. [73] It varies depending on factors including the distribution and size of abrasive particles, processing parameters, and wheel structure. Therefore, it comprehensively reflects the influence of grinding conditions and is crucial for achieving precise control over the surface integrity of SiC wafers. Previous studies primarily focused on the interaction between the grinding wheel and workpiece during rotational grinding processes, establishing predictive models for grain depth of cut. Young et al. [74] simplified the arrangement of abrasive protrusions on the wheel surface. They computed the material removal area per wheel revolution to devise an average prediction method for grain depth of cut in grinding. However, in practical grinding, the heights of abrasive protrusions on the wheel surface do not exhibit uniformity. To address this issue, Sun et al. [75] studied the stochastic nature of abrasive protrusion heights on the wheel surface and developed mathematical relationships between grain depth of cut and processing parameters, depicted in Figure 29. They also investigated how abrasive grain size, material properties, and wheel circumference influence grain depth of cut.

The aforementioned predictive models for grain depth of cut mainly consider the relative motion between the grinding wheel and workpiece during rotational grinding processes. However, practical grinding operations involve rebound effects of abrasive grains on both the workpiece and the grinding wheel due to normal contact forces. Addressing this, Zhang et al. [76] introduced an elastic coefficient to quantify abrasive grain rebound on these surfaces, developing a model that also considers subsurface damage depth on the grinding wafer. Experimental validation on silicon wafers

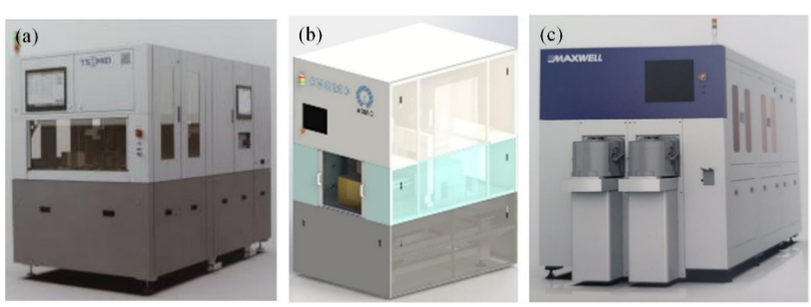

Fig. 27 Domestically-produced ultraprecision SiC wafer grinder: (a) TFG-3200, (b) CMG200, (c) MX-SSG.

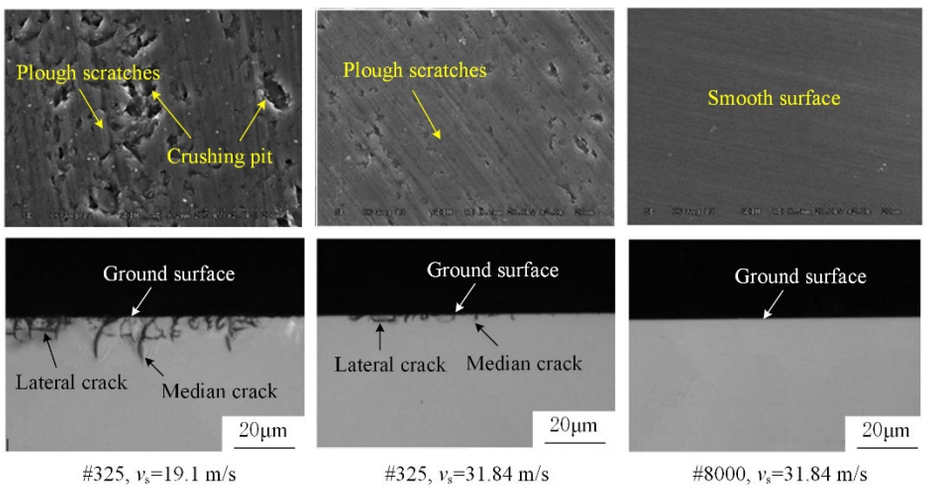

Fig. 28 Surface/subsurface characteristics of 6H SiC wafers ground under different grinding conditions [71]

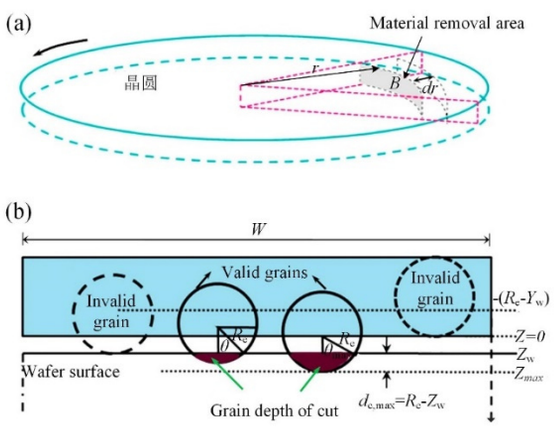

Fig. 29 Model of abrasive cutting depth based on the motion relationship between wheel and workpiece: (a) Material removal area of grinding wheel rotation, and (b) random distribution of abrasive cutting depth.[75]

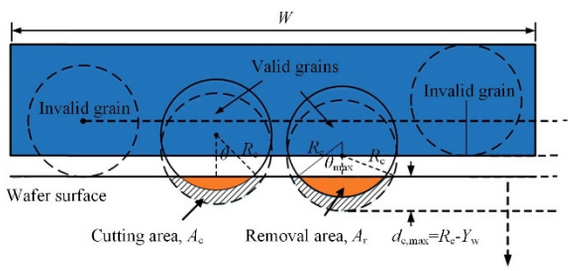

Fig. 30 Depth modulus of abrasive cutting considering rebound.[76]

showed prediction errors of less than 10%, as in Fig. 30. To enhance model accuracy, researchers like Lin et al. [77] analyzed irregular polyhedral abrasive grains with varied blade circle radii, refining predictive models based on groove depth and shape measurements on ground wafers. Zhang et al. [78] simplified abrasive shapes to tetrahedrons, investigating dynamic interactions between grinding components and developing models integrating wheel structure and material properties. Validation on silicon wafers demonstrated improved surface roughness predictions, reducing errors by 40% to 60% compared to existing approaches.

However, a comprehensive understanding of grain depth of cut in ultra-precision grinding, which fully incorporates the material properties of SiC wafers and the dynamics of rotational grinding processes, remains lacking.

The surface quality of semiconductor chips is crucial for subsequent processing efficiency and costs, with surface roughness being a critical evaluation metric. To address this, Wu et al. [79] assumed a Rayleigh distribution for the heights of abrasive grain protrusions. They took into account material properties and process parameters, distinguishing between ductile and brittle grinding modes for individual abrasive grains. They developed a model to predict surface roughness for SiC wafer grinding and calibrated it through a series of experiments. Zhang et al. [80], based on nano-indentation results, examined how RB-SiC is removed and categorized its grinding into ductile and brittle modes. They formulated a theoretical approach to estimate surface roughness in ultra-precision grinding. Through grinding experiments, they validated the model with an average error of only 5.87%, as illustrated in Fig. 31.

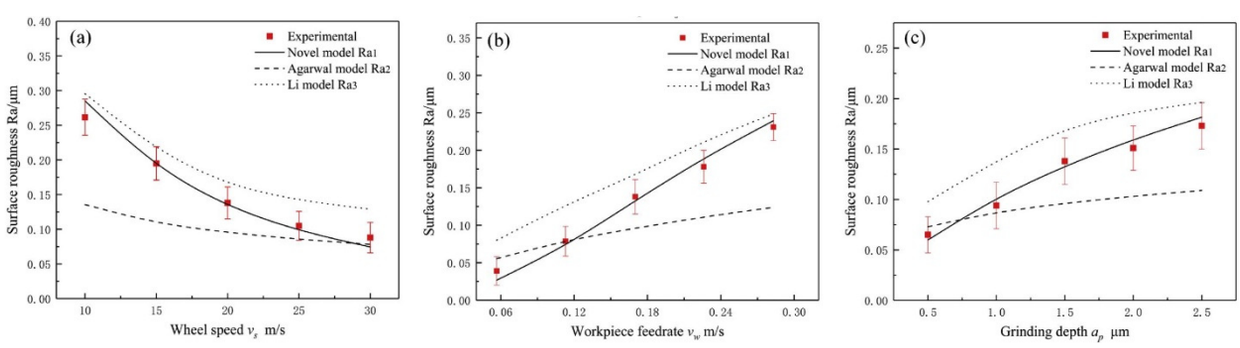

Fig. 31 Comparison between predicted and actual surface roughness across different grinding parameters: (a) a_p=1.5μm, v_w=0.170m/s; (b) a_p=1.5μm, v_s=20m/s; (c) v_w=0.170m/s, v_s=20m/s. [80]

Existing surface roughness prediction models for silicon carbide grinding are primarily developed for circumferential grinding. However, there is currently no theoretical modeling research on the surface roughness of SiC wafers after rotational grinding. This lack of theoretical modeling makes it difficult to precisely control the surface roughness in the ultra-precision grinding of SiC wafers.

Grinding SiC wafers with diamond wheels results in mechanical action from abrasive grains, which creates damage layers both at the surface and below. These damage layers increase the time required for subsequent chemical mechanical polishing, reducing processing efficiency and yield rates of the wafers. Moreover, they can adversely affect the functionality and lifespan of devices. Therefore, predicting and controlling subsurface damage depth is essential for ensuring efficient and minimally damaging SiC wafer grinding. To address the issue of grinding damage control, researchers have developed predictive models for damage in hard brittle materials. Lawn et al. [81] analyzed the stress field of median/radial crack systems based on a single-grain indentation model for hard brittle materials. They established a relationship model between crack length and normal force applied to the workpiece, as depicted in Fig. 32. It is noteworthy that the normal force here results from the coupling of elastic and plastic forces, generated respectively by elastic stress and residual stress. They emphasized that when the ratio of material hardness to elastic modulus is less than 0.1, plastic forces induced by residual stress dominate, a condition satisfied by most hard brittle materials. Building upon this foundation, Lambropoulos et al. [82] refined the stress coefficients of the aforementioned model, which has been widely used for predicting subsurface damage depth in subsequent research on hard brittle material grinding. Li et al. [83] and Yin et al. [84] simplified the normal force during single-grain scratching processes to elastic forces and introduced the effect of strain rate on normal force through empirical fitting. By incorporating the geometric characteristics of rotational grinding, they uncovered the mathematical relationship linking normal force with grain depth of cut, thereby establishing a theoretical model for grinding damage depth, strain rate, and grain depth of cut.

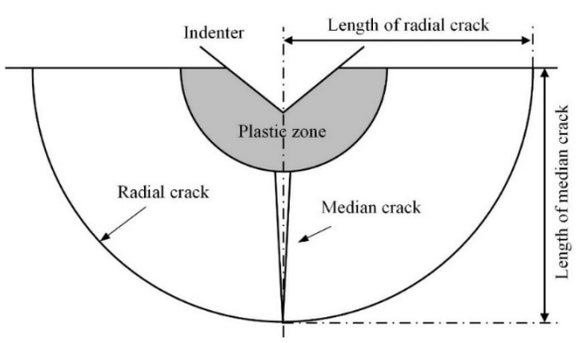

Fig. 32 Median/radial crack model for indentation models of hard and brittle materials.[81]

From existing literature, it is evident that the interaction force between grains and the workpiece is a key input parameter for developing models of damage depth. This model hinges significantly on the interplay of elastic and plastic forces within the workpiece, where plastic forces exert the predominant influence. However, in studying subsurface damage depth during grinding processes, the expression of plastic forces induced by residual stress presents challenges. Typically, the normal force is overly simplified to elastic forces, and coefficients are adjusted based on experimental fittings, thereby limiting the generality and scientific validity of the final model.

Therefore, accurately modeling the interaction forces between abrasive grains and the workpiece remains a significant challenge. To address this, Li et al. [85] proposed a hypothesis regarding the lateral crack depth being equivalent to the surface roughness Rz during grinding, and derived a nonlinear relationship between them independent of the normal force parameter. Through grinding experiments on BK7 glass, they found an average error of 20% in validating this relationship. Chen et al. [86] considered the influence of grinding wheel vibration during the grinding of brittle materials and established a quadratic polynomial correlation between subsurface crack depth and surface roughness Rz. However, the constants in the polynomial need adjustment based on specific processing conditions and process parameters. Yao et al. [87] investigated how the geometric interactions between the grinding wheel, abrasive grains, and workpiece affect the precision grinding process of optical glass. They explored how various grinding parameters influence the depth of damage beneath the surface and developed mathematical correlations linking this damage depth, surface roughness Rz, and the depth of abrasive grain penetration. Building upon this work, Li et al. [88, 89] further improved the quantitative model relating damage depth beneath the surface, surface roughness Rz, and grain depth of cut. They validated this model through ultra-precision grinding experiments on BK7 and Si wafers.

Currently, there are no predictive models for subsurface damage in SiC wafers during grinding. The models for subsurface damage depth assume a correlation where surface roughness Rz approximately equals lateral crack depth. This assumption becomes inappropriate for ductile machining processes where no cracks exist. Furthermore, predicting subsurface damage depth solely based on surface roughness Rz cannot establish the correlation between subsurface damage depth and grinding process parameters, thus failing to guide process control for subsurface damage depth.

4.4 Issues in process research

The current research on ultra-precision machining of SiC wafers highlights challenges posed by its inherent hardness, brittleness, and chemical inertness. These characteristics not only induce significant surface damage but also hinder processing efficiency, falling short of high-efficiency, low-damage production requirements. Ultra-precision grinding technology, based on rotational principles, offers advantages like uniform abrasive distribution, low grinding forces, and potential for ductile machining, promising for SiC machining. However, domestically developed high-performance grinding machines lag behind international standards. Moreover, understanding surface/subsurface damage mechanisms in SiC during ultra-precision grinding remains incomplete, presenting substantial research opportunities. Systematic exploration of the relationship between grinding parameters, wheel characteristics, and their effects on efficiency and damage is lacking. Future efforts should prioritize developing specialized equipment and comprehensively investigating damage mechanisms to optimize efficient, low-damage grinding processes for industrial SiC wafer applications.

5. Summary and Outlook

To summarize the current research progress in ultra-precision machining SiC wafers, both domestically and internationally, and to highlight some existing shortcomings, along with providing research prospects, the main points are as follows:

(1) Limited Understanding of Material Removal and Damage Mechanisms in Single Crystal SiC. Current knowledge regarding

material removal and damage mechanisms in single crystal SiC is superficial, often based on simplistic descriptions and assumptions derived from simulations and experimental observations. There are significant discrepancies among different conclusions. It is crucial to methodically examine how material is removed during both ductile and brittle stages of single crystal SiC and explore the microscopic mechanisms and conditions under which damage forms. This will reveal the general laws governing material removal mechanisms in single crystal SiC.

(2) Challenges with Grinding and Mechanical Chemical Polishing Combination Method. Presently, the predominant method for machining single crystal SiC involves a combination of grinding and mechanical chemical polishing. This process is intricate, susceptible to damage during processing, and inefficient, posing challenges in achieving the requirements for effective and minimally damaging processing of large-sized SiC wafers. To address this, optimizing the combination method by introducing new processes to replace certain steps, thereby improving precision and efficiency, and optimizing process parameters for each step while rationalizing their proportions, is recommended.

(3) Need for Development of Specialized Ultra-Precision Grinding Equipment for SiC Wafers. The primary suppliers of specialized ultra-precision grinding equipment for single crystal SiC are concentrated in Japan and the United States. There is an urgent need for domestic efforts to advance and strongly support the research and development of equipment for ultra-precision grinding of single crystal SiC and high-performance grinding wheels. Key challenges include overcoming integration, scaling up to larger chip sizes, developing high-performance grinding equipment, and enhancing automation. This initiative is crucial for achieving significant progress in the third-generation semiconductor industry.

(4) Incomplete Research on Ultra-Precision Grinding Technology for SiC Wafers. The current understanding of material removal mechanisms and guiding principles for ductile domain grinding processes is not yet sufficiently profound. It is crucial to delve deeper into the diamond ultra-precision grinding mechanisms for SiC wafers, establish models for abrasive grain depth of cut and surface integrity prediction specific to single crystal SiC, guide the selection of grinding wheel characteristics and process parameters, design efficient, low-damage grinding processes, and explore the potential of introducing combined processes to improve machining effects.

Acknowledgements

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