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High-Speed Column Level ADC Design of Full Parallel Two-Step Nested TDC for CMOS Image Sensor

Zhongjie Guo*, Yangle Wang, Ruiming Xu, Ningmei Yu and Longsheng Wu

Abstract: This study presents a column-level analog-to-digital converter (ADC) designed specifically for CMOS image sensors. It is characterized by a two-phase fully parallel architecture combined with time-to-digital conversion (TDC) technology, resulting in high-speed performance. After the coarse-to-fine conversion process is completed, the output of the comparator is restricted by the clock signal. This results in the generation of a time difference value during the last clock cycle of the conversion. TDC is used to convert the difference into the corresponding numerical code and compare it with the ADC conversion results presented in this article. While realizing high-precision A/D conversion, the conversion speed of ADCs has greatly improved. The circuit proposed in this article is developed and validated based on 55 nm CMOS technology. In a design environment, the analog voltage is set at 3.3 V, the digital voltage at 1.2 V, and the input signal range at 1.5 V. The entire system operates at a clock speed of 100MHz. In this instance, the paper presents a 12-bit ADC that achieves an integral nonlinearity (INL) of +1.47/-1.74 LSB, a differential nonlinearity (DNL) of +0.8/-0.8 LSB, and a signal-to-noise ratio (SNDR) of 68.272 dB. The ADC main architecture designed in this paper adopts a fully parallel design that is not limited to a fixed design accuracy. It achieves a high parallel time multiplexing rate of up to 100% through an adaptive time multiplexing mechanism. Additionally, the ADC architecture includes a 3-bit time-to-digital converter, enhancing the efficiency of the analog-to-digital conversion process. The column ADC circuit presents an efficient ADC design solution that is well-suited for high frame rates and large-area array CMOS image sensors.

Key words: column-level ADC, CMOS image sensors, two-phase, fully parallel, time-to-digital conversion.

1 Introduction

The complementary metal oxide semiconductor (CMOS) image sensor (CIS) is widely used in various fields due to its advantages, such as energy efficiency, cost-effectiveness, and high integration capabilities. As a result, it is gradually replacing traditional charge-coupled device (CCD) image sensors [1,2]. CIS first utilizes the ordered pixel arrays in the face array to complete the photoelectric conversion process. Then, the column readout circuits for sampling, analog-to-digital conversion, and driving the output of a number of processes, each of which will have an impact on the quality of imaging. Therefore, it is crucial to thoroughly analyze the requirements of the subject and explore the appropriate architecture for the CIS readout circuit. On this basis, determine the timing control design of digital circuits, algorithm design, and analog circuit design such as analog-to-digital converters[3]. The system

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framework of CIS is shown in Figure 1. The ADC, as the core of the column readout circuit, will determine the overall quality of the imaging in terms of both accuracy and speed.

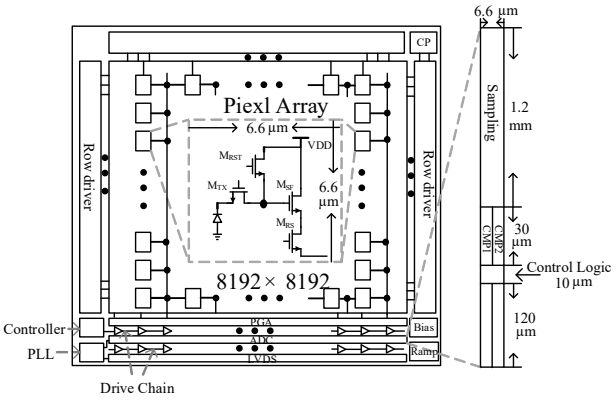

Figure 1. Schematic diagram of CMOS image sensor system framework

Recently, there has been a focus on the various column-level ADC architectures used in CMOS image sensors. There are different types of ADCs available, including successive approximation register (SAR ADC), cyclic ADC, and single slope ADC (SS ADC) [4–6]. However, SAR ADCs and cyclic ADCs are not ideal for large-pixel array CIS. On the one hand, due to the large chip area requirement for each column-level SAR ADC that includes a digital-to-analog converter (DAC), on the other hand, cyclic ADCs have a small silicon wafer area and a high conversion rate, which leads to increased power consumption of the chip [7–11].

Regardless of the exposure mode, whether it's the CIS mainstream global exposure mode or the roller shutter exposure mode, the current speed limit for exposure is determined by the read-out and quantification stage of the electrical signal. The ADC is the key part of the constrained signal quantification processing. Therefore, to ensure a higher frame rate, a higher ADC sampling rate is necessary. At the same time, to ensure imaging quality, higher ADC accuracy is essential. Therefore, under the line-by-line readout of CIS, the conversion time of the column-level ADC becomes the maximum limit of the pixel signal readout. Equation (1) illustrates the correlation between the frame rate of the column-level ADC and the number of rows in the array, and the conversion time. The specific performance is as follows:

$$f = 1/(T \times R) \tag{1}$$

where f represents the frame rate, T is the time required for the column-level ADC to quantize a row, and R is the number of pixel rows.

Figure 2 shows the system framework of SS ADC. The accuracy and speed of the entire column readout depend on the analog-to-digital conversion accuracy and sampling rate of the SS ADC, which serves as the core module of the CMOS image sensor column readout. The SS ADC is mainly composed of a ramp generator to generate V_{ramp}, a sampling circuit to collect the voltage signal Vin after pixel exposure, a comparator, and a digital counting circuit with counters and registers as the core.

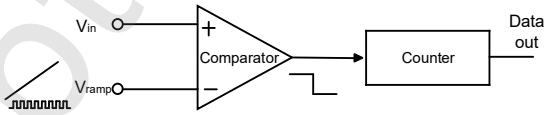

Figure 2. SS ADC system framework

In the industry, SS ADC is widely used in CMOS image sensors due to its simple design and high efficiency [12,13]. However, in the case of N-bit precision conversion, the quantization of the SS ADC requires 2N clock cycles. The primary drawback of SS ADCs is their restricted conversion rate, which consequently affects the readout rate of the image sensor [14,15]. To capture high-speed photographs in various situations, it is necessary for the frame rate of the entire CIS to exceed 100 frames. This means that when the pixel array reaches levels in the hundreds of millions, while maintaining a precision of over 12-bit, the A/D conversion rate must be kept at a minimum of 1μs, as mentioned in references [16–18]. Therefore, this paper addresses the issue and proposes an improved resolution. As shown in Figure 3, a schematic diagram of the column-level high-speed readout circuit proposed in this paper for use in the CIS system.

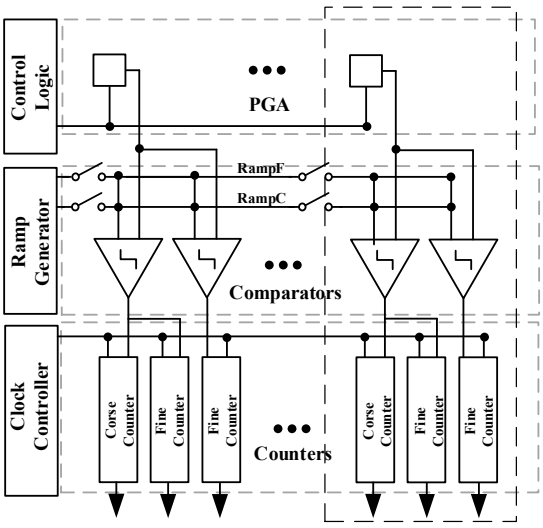

Figure 3. Schematic diagram of the readout circuit column-level ADC system framework

Next, we turn to the current evolution of high-speed SS ADC architectures in the field. The A/D conversion process of the two-step single-slope (TS-SS) ADC is divided into two parts: a coarse conversion with M bits of accuracy and a fine conversion with N bits of accuracy. TS-SS ADCs have a shorter conversion time of $2M+2N$ clock cycles compared to standard SS ADCs. This has been demonstrated in studies[19–24]. However, the conversion process could benefit from improved time management to avoid any unnecessary waste. In addition to two-step application, currently for the improvement of conversion efficiency, architectures are increasingly beginning to use time-to-digital conversion technology by improving its encoding method, nesting the time-to-digital conversion in the main SS ADC architecture as part of its third step of conversion, and exploring how to accomplish a higher speed and more efficient conversion process with the same accuracy [25–27].

Considering the research status and current issues, this paper aims to develop a fully parallel two-step single-slope ADC (PTS SS ADC) architecture using TDC to enhance the frame frequency of the CIS system. In addition, it presents a new idea for a high frame rate CIS system under the condition of a large-scale array.

2 Fully parallel conversion principle

This section introduces a high-speed and high-precision SS ADC that utilizes TDC technology. Referring to Figure 4, it includes a comparator CMP1 along the triggers DFF1; a comparator CMP2 along the triggers DFF2; a network controlled by a switching capacitor; COUNTER1; COUNTER2; a digital addition circuit with digital control logic.

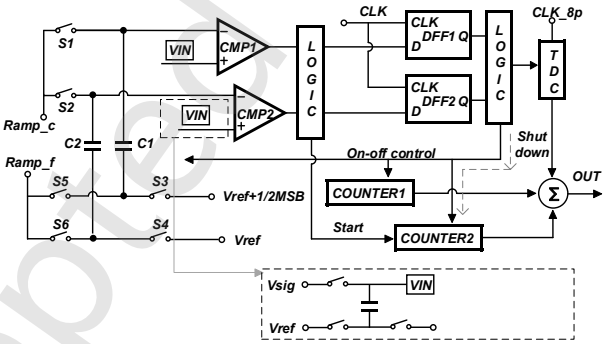

Figure 4. Specific circuit design.

The "completely parallel" mentioned in this paper refers to not only the coarse mode conversion, but also the fine conversion. The two modules start synchronously and share one conversion cycle, resulting in reduced conversion times for the ADC and achieving high speed. The time multiplexing rate of this architecture is determined by the relationship between the slope and the input signal, which can be applied to different design scenarios. The time multiplexing rate can reach 100%, which will be described next.

It is important that Vref remains constant in order to fix the capacitance values of capacitors C1 and C2 during the coarse conversion process. This value is 1LSB, which is the value of the dynamic range of a fine conversion, which remains unchanged in the specific circuit controlled by the switches S1 and S3. The thin slope's initial voltage is Vref, which is controlled by switches S5 and S6. After the connection, the voltage of the lower board remains unchanged, while there is a gradual transition from Vref to 0, resembling a step change process.

The oblique wave signal of coarse conversion and fine conversion is started synchronously. Firstly, the coarse slope control switches S1 and S2 are activated, causing S3 and S4 to be activated as well. At this point,

the upper plates of storage capacitors C1 and C2 contain the coarse ramp signal RAMP_C, while the lower plates hold the fixed levels Vref and Vref+1/2 most significant bit (MSB). To achieve the desired bottom pole plate signal, an additional circuit can be utilized to increase Vref by 1/2 MSB. It is important to mention that at this time, both the fine and coarse slopes in the slope generation system start simultaneously. In the initial step of the conversion, only the coarse slope is used to access the A/D conversion system in order to complete the coarse conversion. However, this does not affect the fine slope or the calibration of the signal to be converted. Next, we will thoroughly examine the parallel processes of coarse and fine calibration of the signals to be converted.

The rough conversion is performed until the signal's interval is determined. After detecting the signal's interval, comparators CMP1 and CMP2 operate simultaneously, and the coarse conversion step is determined by the input signal to capacitors C1 and C2 at the end of the operation. At this point, S1 and S2, which are responsible for controlling the coarse ramp voltage, are deactivated. The S3 and S4, both controlled by digital logic, are also disconnected. In this case, the tilt step voltage mVc is stored in the upper plates of the two fixed capacitors.

Then, the micro-oblique wave control switches S5 and S6 are activated. The smooth slope from VREF down to 0 is connected to the circuit system at this point. In accordance with the principle of charge conservation, the voltage of the upper panel of the capacitor decreases as a result of the pre-stored voltage information. All the timings for S1/S2, S3/S4, and S5/S6 remain unchanged. The entire analog-to-digital conversion switching process 1 is S1/2, S3/4 is closed, and S5/6 is disconnected. At this time, the capacitors CI and C2 store the signal of $m\Delta Vc$, and further, the signal is the signal of the signal VIN to be converted at a certain step on the rough slope, and the switching process 2 is S3/4 and S1/2 is disconnected and S5/6 is closed, allowing the completion of the specific ramp switching process shown in Figure 5.

It is worth noting that in the first timing action, the switches S1 and S3, S2 and S4 are used to control the upper and lower plates of the capacitors C1 and C2. At this time, the corresponding charges are stored on C1 and C2 respectively. In the second timing action, the switches S1, S2, S3, and S4 are disconnected, and S5 and S6 are connected to the lower plates of the capacitors C1 and C2 respectively. Since the capacitor does not have a charge discharge path at this time, that is to say, under the switching action of the capacitor, the upper and lower plates are high impedance nodes or can be equivalent to floating, so the capacitor's The lower board changes from Vref to Ramp_f after the second switching action. Therefore, the upper board will follow the voltage change action of the lower board to complete the coarse ramp switching. In more detail, the charge stored on the capacitor remains unchanged, causing the voltage difference between the upper and lower boards to remain unchanged.

During the coarse ramp conversion process, the switching action of the switch is that the switches S1, S2, S3, and S4 are all disconnected, and the switches S5 and S6 are closed. At this time, the thin ramp is connected to the system, but due to the conserved charge of C1 and C2, the voltage of the upper plate of the capacitor follows the voltage change of the lower plate.

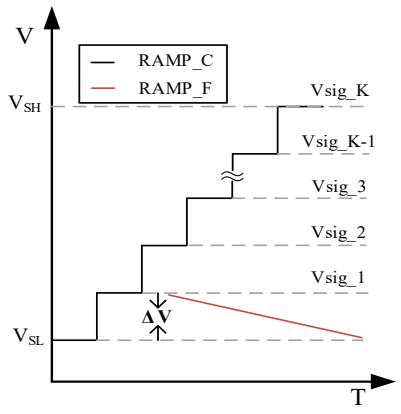

Figure 5. Schematic diagram of ramp switching.

However, before that, the fine and coarse ramps are issued simultaneously, with the fine conversion process being completed for the same duration as the coarse conversion. Therefore, when switches S5 and S6 are closed, the completed fine conversion information is instantly connected to the lower board of the capacitor and embodied in this coarse conversion

information. The mechanism used here involves a logarithmic time division multiplexing parallel conversion. This means that the rough conversion and calculation of the fine transformation are performed simultaneously, allowing them to share the same conversion time. As a result, the purpose of fast switching can be achieved.

Due to the fine ramp at the same time as the coarse ramp, in the coarse and fine switching processes, there may be a fine ramp at the early end of the situation. However, since the coarse ramp has not been fixed at this point, it is impossible to record the voltage value of the fine conversion. Therefore, it is necessary to complete the parallel conversion process of the two quantizers. This ensures that after the conversion is complete, we can obtain the desired value through a simple 1/2 data selector at the back-end. The accurate time of the corresponding comparator can be selected based on the slope of the accuracy conversion. Due to the need for parallel conversion, it is necessary to perform rough conversion before achieving accurate results. Further refinement is then required to obtain the final results. The final analog-to-digital conversion time is MAX (*T*coarse, *T*fine). The parallel two-step conversion method presented in this paper compresses the time of the fine conversion to fit entirely within the end of the coarse ramp, which can increase the time reuse rate to 100%.

3 Time Difference Conversion Principle

Multiple clock scales can be superimposed for digital measurement of time. This method utilizes several time-delay elements to generate multiple timing edges within the same clock cycle. Furthermore, the time difference is restricted by the multiphase clock edges, resulting in the successful conversion of time and number [28–30]. On this basis, after determining the fine conversion level, the SS ADC uses a higher-frequency polyphase clock to detect the conversion delay between the end moment of the comparison and the clock edge of the system termination signal. This allows for the measurement of the time difference between the beginning and end moments, which is then digitized to complete the quantization of the residual error of the SS ADC. This process helps to enhance the conversion accuracy and speed.

As shown in Figure 6, the IS model represents the initial value design circuit, comprising eight independent components with gates. The functional logic aims to modify the initial output state of the clock edge flip-flop by selecting to reset or set the flip-flop device, in order to achieve the desired initial value. 9 The input and gate cooperate with the STOP signal to stop the clock signal and maintain the trigger in its current state. The working logic is as follows: when the START signal is received, IS stops resetting the flip-flop based on the initial value design. When the multiphase clock is activated, the flip-flop will transition its output state based on the edge drive characteristics. The resulting output is then passed to the coding circuit for logic processing and eventual output, allowing for the quantification of values over time.

then a higher accuracy can be achieved at a certain time interval. To ensure the stability and successful

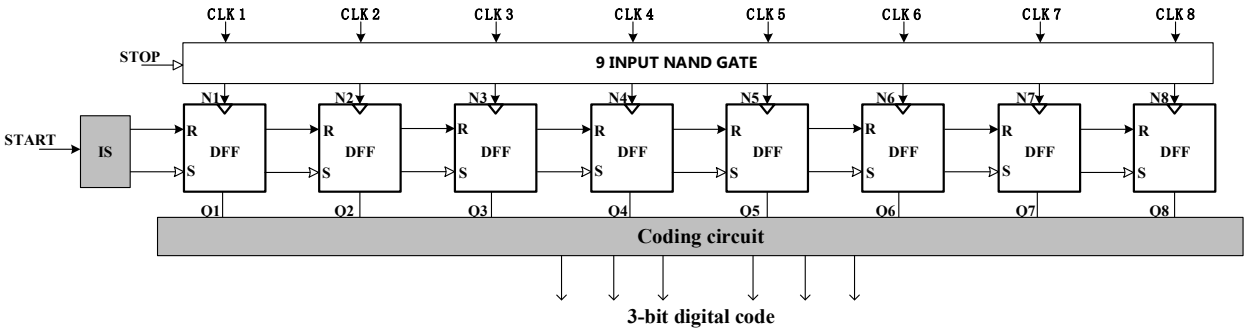

Figure 6. Column-level 3-bit TDC structure.

implementation of technology transfer agreements. On this basis, this paper utilizes a delayed phase-locked loop (DLL) to generate clock signals CLK1~CLK8 for controlling various factors such as temperature, voltage, and process angle. This method adopts a method based on time delay conversion. The start signal of the TDC architecture is provided by the output of the comparison circuit. Additionally, the rising edge of the last clock cycle after the end of the fine conversion is used as the stop signal for TDC. The TDC architecture is utilized to determine the shift that occurs between the start signal and the end signal.

The multi-phase clock will ensure that the phase difference remains consistent. The phase difference information can generate multi-bit time-to-digital conversion results using simple binary encoding. Given the design of this article as an 8-phase clock, the quantized interval can be divided into 8 parts. Finally, a digital signal responding to the time relationship of a 3-bit can be generated by encoding.

4 Slope Correction Technique

The Vref signal is the start of Ramp_f and the fine conversion begins from it. The VIN signal is generated by the pixel unit in the CMOS image sensor and is equivalent to the value of the signal to be converted by the ADC.

The positive input signal of the comparator uses the same sampling circuit as the corresponding ramp signal. The calibration circuit samples both the input signal and the ramp signal at the same time, resulting in the input signal having the same error as the ramp signal. The synchronization of the size and operational timing of the sampling circuits for the ramp and input signals ensures that the slope error aligns with the input signal error. Consequently, the impact of non-ideal factors on the output of the conversion process is eliminated, allowing for error calibration in both coarse and fine conversions. This approach enhances conversion accuracy while maintaining high-speed performance.

Both differential nonlinearity (DNL) and integrated nonlinearity (INL) are static parameters of analog-to-digital converters (ADC) that directly manifest as non-linearity. In the ADC system described in this paper, the main problem arises with non-linearity during the thickness ramp switching process. This is due to the occurrence of switching charge injection and clock feedthrough problems, as well as the introduction of non-ideal channel charge and parasitic capacitive coupling charge, resulting in the existence of non-linearity. The slope correction technology is designed to address this issue. The signal to be converted is about to undergo a switching process that aligns with the thickness of the slope, and an artificial non-ideal factor is introduced into VIN. The error correction method guarantees the relative difference between the slope voltage and the input signal voltage, minimizing the impact of non-ideal factors in the sampling circuit. The correction effect improves as the coarse slope voltage approaches the input signal voltage.

The proposed calibration technique offers several benefits:

① It features a straightforward structure that allows for integration into a single column;

② The correction precision is high, and the correction efficacy remains unchanged even as ADC accuracy improves;

③ The adaptive error matching under the pressure, volume, and temperature (PVT) conditions enhances the system's robustness.

5 Circuit Design and Implementation

The design structure of this paper is 4+5+3 bits. This circuit is shown in Figure 4, while its operation is illustrated in Figure 7. First of all, a two-stage complete parallel conversion is performed, consisting of a 4-bit rough conversion followed by a 5-bit fine conversion. RAMP_C is divided into 16 steps. In addition, the entire fine slope is the step value of the coarse slope. Both CMP1 and CMP2 can carry out both coarse and fine conversions simultaneously, allowing for the retrieval of results from both types of conversions.

During fine conversion, a compensation slope is used to determine whether to use the compensation slope conversion result CMP1 OUT or the normal

conversion result CMP2 OUT. This decision is made by the logic control unit. Based on this structure, a D trigger for generating time differences and a clock compressed TDC for time difference conversion have been integrated. The DFF OUT is generated in the final clock cycle of the A/D conversion using the D trigger and then measured by TDC. Through logical judgment, the final analog-to-digital conversion result is the count value of the coarse slope minus the counter value of the fine slope minus the count value of the TDC, and this addition and subtraction process can be realized by the subtractor circuit.

This architecture adopts a fully parallel analog-to-digital conversion method, which is similar to a time-interleaved ADC. The coarse conversion and the fine conversion are serial conversion methods in normal mode, but this article innovates in the architecture and adopts a fully parallel architecture and control timing. In the process of coarse conversion, although the fine slope cannot be connected to the system, the fine slope has been synchronized at the beginning and after the coarse conversion is over, the information to be converted at this time is synchronously connected to the system through the S1-6 switch control, and part of the fine slope is connected to the system synchronously. The information to be converted at this time is controlled by the S1-6 switch, and part of the fine slope is connected to the system synchronously. The conversion time is nested in the coarse conversion, and a parallel analog-to-digital conversion method is realized.

In the last quantization cycle of the fine conversion, this paper uses 3bit time-to-digital conversion technology to quantify the time value between the time value at the end of the fine conversion and the rising edge of the clock as the residual error in the system, and make a difference with the analog-to-digital conversion value of the SS ADC, and subtract this part of the residual error. At the same time, the system completes a higher-precision analog-to-digital conversion process.

In view of the quantitative mechanism in this structure, the core innovation of the architecture proposed in this paper lies in the parallelism of the thickness slope. The conversion mechanism can identify both the coarse range interval and the fine range of the signal to be converted simultaneously. After locking the coarse range, the fine range instantly stores the information of the 1MSB fine conversion exploration completed during this coarse conversion time in the system, and the time is multiplexed. The conversion method is similar to the current mainstream time-interleaving technology, but there are innovative ways to implement it in this system. Although the signal of the thin range must be completed once the coarse range address search is finished, this is a fundamental logic that any structure will have, but for the structure of this article, the specific conversion time is MAX(Tcoarse,Tfine). The further specific explanation of the conversion relationship is as follows:

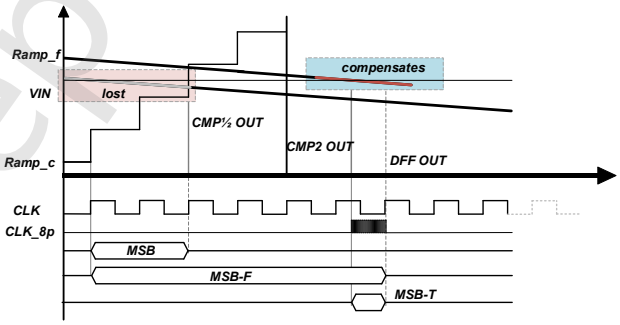

Figure 7. Timing diagram of the proposed ADC.

Initially, a coarse conversion is executed. At this stage, the ramp signal Vramp_ Start steps into full swing. The comparator compares the ramp signal with the input signal VIN for conversion. Following the M-step comparison, the output of the comparator transitions to a high level, resulting in the generation of a high-level M-bit digital code A by the coarse conversion counter.

$$m\Delta Vc < \mathrm{VIN} < (m+1)\Delta Vc \tag{2}$$

It should be noted that the N-bit fine conversion process is synchronous. Upon triggering the comparator. The ultimate numerical code output is as follows:

$$D_{out} = A - B \tag{3}$$

It is worth noting that A is the digital code for the coarse slope analog-to-digital conversion, and B is the digital code for the fine slope analog-to-digital conversion. After the two-step analog-to-digital conversion, the A digital code is used to subtract the B

digital code, which corresponds to the overall digital output result after the thickness analog-to-digital conversion at this time.

Throughout the entire process, both the coarse conversion of *M* bits and the subtle conversion of *N* bits are performed synchronously. On this basis, the input signal is finally transformed by using the time interval of the maximum binary conversion, and a smaller N-bit digital signal is obtained. The digital signal of all *Q* bits can be obtained by performing a simple logic operation on the data of a high *M*-bit and a low *N*-bit.

This conversion logic enables the simultaneous execution of conversions. However, the limitations of the circuit structure can affect its readability. In this way, it is impossible to quantify some intervals efficiently. The accuracy of the conversion is significantly reduced by this, resulting in the introduction of a compensation slope to the system. Regardless of the initial voltage differences, it maintains a consistent gradient during the fine conversion process. The full switching time interval can be accurately quantified thanks to the compensated inclination. By adjusting the counter's weight, the corresponding *N*-digit code can be efficiently retrieved.

The fully parallel architecture designed in this paper is in parallel with the coarse conversion, and the fine conversion is also in progress. After the coarse conversion is over, the information of the fine conversion at this moment is connected to the system through the action of the switch S1-6, and due to the conserved charge of the capacitors C1 and C2, the voltage of the upper plate of the capacitor will follow the voltage value of the fine slope to change (the voltage difference between the upper and lower plates remains the same), and then the comparator will make a decision. However, in this process, there will be quantitative information about the fine slope that precedes the completion of the coarse slope, which may cause the comparator to flip incorrectly. Therefore, in order to solve this problem, the author has slope compensation for the architecture, that is, the lower boards of capacitors C1 and C2 are connected to Vref and Vref+1/2MSB respectively, and the lower boards are fixed at different voltage values. After the fine slope is connected, if the fine conversion has been completed before the coarse conversion, there will be a comparator that does not flip, and the input terminal of the other comparator compensates for the fine slope by 1/ 2MSB, so the flip point of the fine conversion will be delayed, and the conversion information of the second paragraph of the fine conversion will be read out normally, which is the value of the digital code B described in equation (3).

In the last stage of coarse tuning and fine-tuning in ADC, the order of the two corresponding comparators is initially reversed. When the D-type trigger circuit is set at a specific time, it causes the trigger circuit to reverse, resulting in the counter that controls the coarse and fine conversions stopping counting. In this case, the starting signal of the 3-bit TDC is applied to the 3-bit TDC, so that the reset of the TDC is terminated and the 3-bit time-to-number conversion is completed. Once the termination signal from the trigger circuit is received, the TDC stops counting and remains in its original working mode. This action keeps the ADC in a constant read state. A 12-bit value is derived by subtracting the values of the ADC and TDC. At the end of the switching period, the control signal resets the SS ADC and the comparator resets the TDC, allowing for the start of the next switching cycle.

The design structure of this paper is 4+5+3 bits. The conversion time of 320ns is specifically expressed in this article as the coarse conversion time of 4bit, the fine conversion time of 5bit, and the time difference time of 3bit. In the analog-to-digital conversion schematic of Figure 7, the coarse conversion of 4bit is performed simultaneously with the fine conversion of 5bit. Once the coarse conversion is completed, the fine conversion process must be conducted for a certain duration. In this scenario, the actual required time is manifested as follows:

$$\mathrm{MAX}(T_{\mathrm{coarse}}, T_{\mathrm{fine}}) = T_{\mathrm{fine}} \tag{4}$$

Since the clock frequency of this article is 100MHz, the conversion time required for the above process is as follows:

$$\frac{1}{100}\mathrm{MHz} \times 2^5 = 0.32\mathrm{us} = 320\mathrm{ns} \tag{5}$$

Due to the time difference technology being

integrated into the final clock cycle of the fine conversion, there is no need for additional time consumption in the 3-bit conversion. This guarantees that the speed can be increased by 23 times while maintaining the same accuracy. As a result, the final actual analog-to-digital conversion time is actually 320ns. It is worth noting that the description in this article is only a specific design case under the application scenario. The specific timetable can be adjusted accordingly in different circumstances.

6 Circuit Design and Implementation

Figure 8 shows the chip verification platform utilized in the architecture of this article. The 8192 x 8192 CIS architecture utilizes PTS SS ADC and TDC circuits that are designed using 55nm 1P4M technology. Based on the existing chip simulation platform, the detailed hardware circuit and hardware structure are designed. Finally, the ADC's parameters are provided. Based on this, the deviation between the measured values and the existing prototype has consistently remained below 10% when compared with the existing prototype for many times.

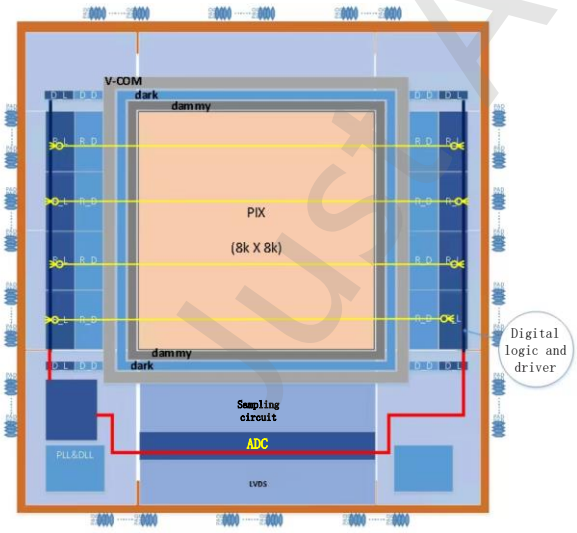

Figure 8. CIS chip overall simulation platform.

Following the 64-line multi-channel signal processing, the signals processed by each signal processing module are connected in series by calling each module, resulting in a 64-line multi-channel signal processing result as shown in Figure 9. Based on this, the digital-analog mixers are kept separate to prevent any interference between signals. Each unit is equipped with a combination of analog and digital components, along with a series of FD capacitors in the longitudinal slots to enhance their resistance to digital noise. For analog-to-digital conversion, the row signals flow from top to bottom (left to right). 64 columnar multiplexing elements are utilized with an operating area of 1200 μm x 422.4 μm.

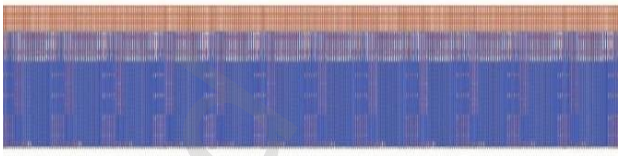

Figure 9. 64-column multiplexing unit physical layout design

The system realizes 12-bit analog-to-digital conversion, 1.6V dynamic range, and 100MHz clock output. Based on this system, the extended ADC and TDC modules of PTS are designed in detail. This paper is structured around the power consumption of both the pre-stage analog circuit and the post-stage digital circuit. The following is the distribution of the power consumption of each module: The comparator is designed to be continuous low-power, with each of the two comparators consuming 14 μW. The switching capacitor uses 17uW, while the post-stage digital circuit and TDC circuit consume 45 μW under full-scale count. In total, the full-architecture power consumption is 76 μW.

The outcomes of the static performance verification for the ADC can be seen in Figures 10 and 11. The INL is +1.47/1.74 least significant bit (LSB), and the measured DNL is +0.8/-0.8 LSB.

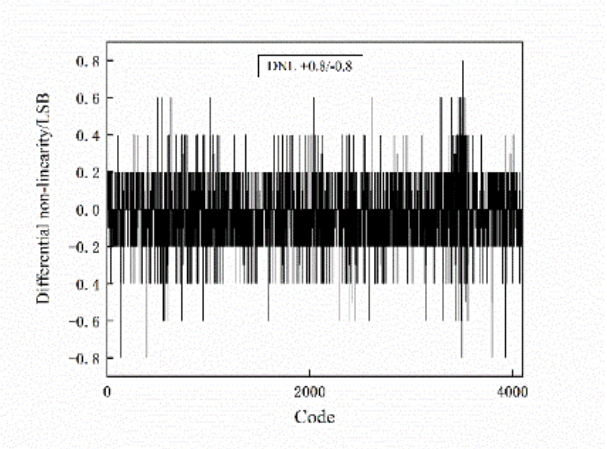

Figure 10. DNL simulation result.

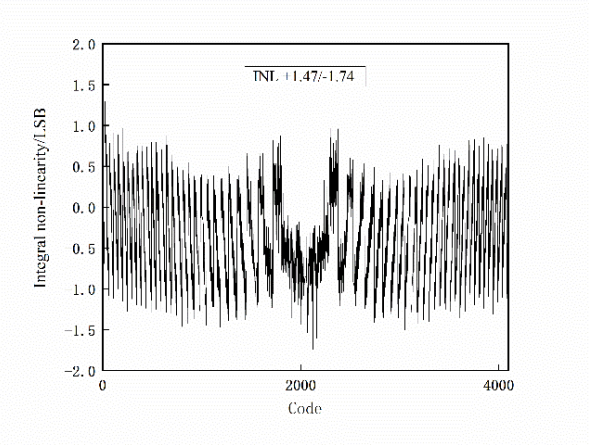

Figure 11. INL simulation result.

Figure 12 shows the analog fast Fourier transform (FFT) spectrum at a sampling frequency of 1.4 MHz. The output signal has a frequency of 147.964 Hz, where the fundamental frequency corresponds to the line with the largest energy in the FFT resolution. The other components in the signal are due to harmonic and noise interference from the input signal. PTS SS ADC combined with TDC results in a signal-to-noise ratio of 68.272 dB versus TDC of 11.049 bits. The power consumption of the entire ADC is 72 μW. The above conclusions are obtained through a simulation test platform, and analyzed and calculated by numerical software.

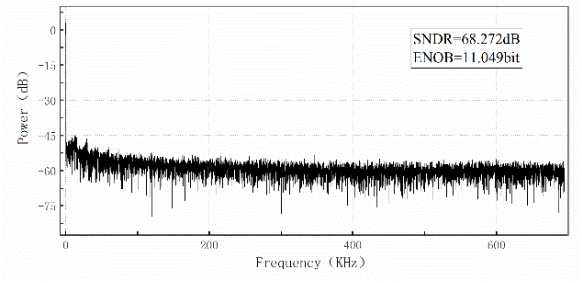

Figure 12. Signal-to-noise ratio analysis.

Compared with current research progress, the architecture adopted in this article has significant advantages. The design parameters are presented in Table 1 for easy comparison.

In [1, 2, 3, 16], a comparison was made between the ADC architecture in the table and the accuracy of 12-bit A/D conversion. In [1], despite having a conversion time of only 1 μs, it sacrifices 177 μW of power consumption. Reference [2] shares the same power consumption as this article. However, its conversion time is 10 μs, which remains unsuitable for large-scale image sensors. In [3], the power consumption is the lowest, measuring only 39 μW. However, its conversion speed falls short of meeting the high-speed requirements of image sensors, which is a significant drawback. Reference [16] discusses a solution that attempts to address the limitations of the three structures mentioned earlier. However, it does not fully meet the requirements for column-level ADCs in the CIS.

Table 1. Comparison with other advanced ADC.

reference	[1]	[2]	[3]	[16]	This work
technology(nm)	130	130	90	-	55
structure	SS-TDC	TS-SS	TS-SS	TS-SS	PTS-SS+TDC
precision(bit)	12	12	12	12	12
conversion range(V)	-	1.2	-	-	1.5
conversion time	1μs	10μs	39.68μs	6.38μs	320ns
DNL (LSB)	+1.1/-0.4	0.76/-0.8	+5.73/-7.3	+1.34/-0.49	+0.8/-0.8
INL (LSB)	+5.8/-8.2	1.06/-0.84	+4.25/-1.00	+2.44/-2.47	+1.47/-1.74
ENOB (bit)	-	11.25	-	-	11.049
Power(μw)	177	72	39	112.5	72

7 Conclusions

A completely parallel two-stage parallel architecture is designed to address the issue of low read rates of single-channel ADC. The SS ADC presented in this paper achieves a conversion time of 320ns while maintaining 12-bit accuracy. Additionally, the fully parallel quantization mode maximizes time utilization. This paper presents a practical solution for the design and manufacturing of CMOS image sensors with a high-speed ADC.

It adopts a fully parallel analog-to-digital conversion method, which is similar to a time-interleaved ADC. The coarse conversion and the fine conversion are serial conversion methods in normal mode, but this article innovates in the architecture and adopts a fully parallel architecture and control timing. In the process of coarse conversion, although the fine slope cannot be connected to the system (because the coarse conversion has not yet been completed), the fine slope has been synchronized at the beginning and after the coarse conversion is over, the information to be converted at this time is synchronously connected to the system through the S1-6 switch control, and part of the fine slope is connected to the system synchronously. The information to be converted at this time is controlled by the S1-6 switch, and part of the fine slope is connected to the system synchronously. The conversion time is nested in the coarse conversion, and a parallel analog-to-digital conversion method is realized.

The verification results listed in Table 1 are all based on the process platform of multiple fabricated tests by the project team, and the agreement between the actual test and simulation verification is over 90%. Therefore, the parameters presented in this paper encompass a wide range of results, including the physical parasitic parameters of the back-end. These results have been carefully considered for their engineering feasibility.

In future work, it is important to address the challenge of achieving high precision while meeting the requirements for higher-speed analog-to-digital conversion. This article focuses on providing solutions to the issues encountered in two-dimensional oversized array CIS. However, it is worth exploring whether the proposed technology in this article can be applied and studied further in the context of 3D CIS, such as lidar in the automotive field and ultra-high-speed photography of digital cameras.

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