Nano Research

ISSN 1998-0124 CN 11-5974/O4
https://doi.org/10.26599/NR.2026.94909305

Research Article

Scalable p-type $Te_{1-x}Se_x$ thin-film transistors and low-power complementary logic gates

Yu Wang[1], Yubo Hao[1], Junli Du[2], Zhenjia Xie[3], Zhiwen Zhou[4](✉), Quanyang Tao[1], Canjun Ke[1], Di Wu[1], Longhui Zeng[1], Yuen Hong Tsang[5,6](✉), Pei Lin[1](✉)

[1] Henan Key Laboratory of Advanced Optoelectronic Materials and Devices, Key Laboratory of Materials Physics of Ministry of Education, School of Physics, Zhengzhou University, Zhengzhou 450052, China

[2] Academy for Advanced Interdisciplinary Science and Technology, University of Science and Technology Beijing, Beijing 100083, China

[3] State Key Laboratory for Advanced Metals and Materials, University of Science and Technology Beijing, Beijing 100083, China

[4] School of Materials Science and Engineering, Harbin Institute of Technology, Harbin 150001, China

[5] Department of Physics and Materials, Photonics Research Institute, Research Institute for Advanced Manufacturing, The Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong, China

[6] Shenzhen Research Institute, The Hong Kong Polytechnic University, Shenzhen 518057, China

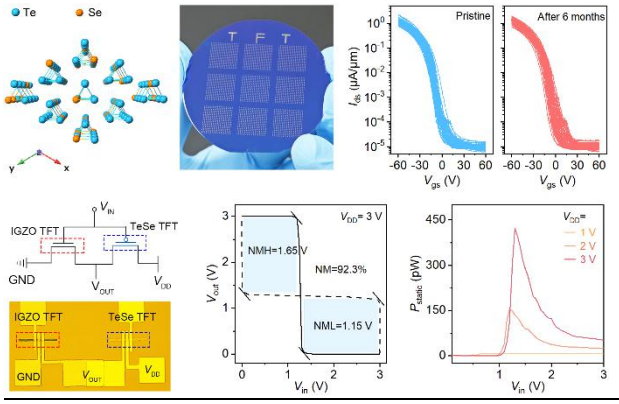
Nano Res., **Just Accepted Manuscript** • https://doi.org/10.26599/NR.2026.94909305
https://www.sciopen.com/journal/1998-0124 on Nov. 2, 2026

© The Authors(s)

Just Accepted

This is a "Just Accepted" manuscript, which has been examined by the peer-review process and has been accepted for publication. A "Just Accepted" manuscript is published online shortly after its acceptance,which is prior to technical editing and formatting and author proofing. Tsinghua University Press (TUP) provides "Just Accepted" as an optional and free service which allows authors to make their results available to the research community as soon as possible after acceptance. After a manuscript has been technically edited and formatted, and the page proofs have been corrected, it will be removed from the "Just Accepted" web site and published officially with volume and article number (e.g., *Nano Research*, **2025**, *18*, 94906990). Please note that technical editing may introduce minor changes to the manuscript text and/or graphics which may affect the content, and all legal disclaimers that apply to the journal pertain. In no event shall TUP be held responsible for errors or consequences arising from the use of any information contained in these "Just Accepted" manuscripts. To cite this anuscript please use its Digital Object Identifier (DOI®),which is identical for all formats of publication.

TABLE OF CONTENTS (TOC)



Leveraging precise stoichiometric control and thickness engineering, we report scalable *p*-$Te_{1-x}Se_x$ TFTs with exceptional ambient stability, enabling their integration into complementary logic gates that exhibit pW-level static power consumption.

Just Accepted

Research Article

Scalable p-type $Te_{1-x}Se_x$ thin-film transistors and low-power complementary logic gates

Yu Wang [1], Yubo Hao [1], Junli Du [2], Zhenjia Xie [3], Zhiwen Zhou [4] ✉, Quanyang Tao [1], Canjun Ke [1], Di Wu [1], Longhui Zeng [1], Yuen Hong Tsang [5,6] ✉, Pei Lin [1] ✉

[1] Henan Key Laboratory of Advanced Optoelectronic Materials and Devices, Key Laboratory of Materials Physics of Ministry of Education, School of Physics, Zhengzhou University, Zhengzhou 450052, China
[2] Academy for Advanced Interdisciplinary Science and Technology, University of Science and Technology Beijing, Beijing 100083, China
[3] State Key Laboratory for Advanced Metals and Materials, University of Science and Technology Beijing, Beijing 100083, China
[4] School of Materials Science and Engineering, Harbin Institute of Technology, Harbin 150001, China
[5] Department of Physics and Materials, Photonics Research Institute, Research Institute for Advanced Manufacturing, The Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong, China
[6] Shenzhen Research Institute, The Hong Kong Polytechnic University, Shenzhen 518057, China

Received: 30 June 2026; **Revised: 2 October 2026**; **Accepted: 2 November 2026**

✉Address correspondence to Zhiwen Zhou, zwzhou@connect.hku.hk; Yuen Hong Tsang, yuen.tsang@polyu.edu.hk; Pei Lin, linpei@zzu.edu.cn

Cite this article: *Nano Research*, 2027, 20, 94909305 https://doi.org/10.26599/NR.2026.94909305

ABSTRACT: Despite the promise of Te as a p-type channel material, realizing Te-based thin-film transistors (TFTs) with low off-state current and high on/off ratio is challenging due to its small bandgap and high background carrier density. Se-alloying offers a potential solution to mitigate these limitations, yet the device performance has remained suboptimal. In this work, through the synergy of stoichiometric control and thickness engineering, we achieve an optimal trade-off between charge transport and switching characteristics in $Te_{1-x}Se_x$ TFTs. The resulting devices exhibit an average field-effect mobility of 16.8 $cm^2 V^{-1} s^{-1}$, I_{on}/I_{off} ratio of 1.3×10^5 and an ultralow off-state current of 10 pA μm^{-1}. The fabrication process is fully compatible with established low-temperature TFT technologies, enabling high-yield production of transistor arrays with favorable electrical uniformity. Notably, the devices demonstrate exceptional environmental stability, retaining critical performance metrics after six months of storage without encapsulation. Complementary logic gates (NOT, NAND, and NOR) are fabricated by integrating p-$Te_{0.63}Se_{0.37}$ and n-IGZO TFTs. The inverter achieves a high voltage gain of 28, a noise margin of 92.3%, and a low static power consumption of 420 pW at 3 V supply voltage. This study highlights the potential of $Te_{1-x}Se_x$ as a scalable p-type channel material, advancing the development of TFT-based logic circuits.

KEYWORDS: thin-film transistor, p-type semiconductor, complementary logic gate, Te-Se alloy, wafer-scale

Just Accepted

1 Introduction

Thin-film transistors (TFTs) represent a foundational technology in modern electronics, driving innovations across both established and emerging applications such as flat-panel displays, image sensors, memory devices, and digital circuits [1, 2]. While n-type TFTs based on amorphous silicon (Si), low-temperature polycrystalline Si, and indium gallium zinc oxide (IGZO) have reached technological maturity through extensive development and commercial deployment, the realization of p-type TFTs remains a persistent challenge due to the scarcity of compatible semiconductor materials and controllable doping techniques. Particularly, these intrinsic limitations are further exacerbated by the stringent requirements for scalable, low-temperature, and cost-effective fabrication processes. The absence of high-performance p-type TFTs and thus the complementary logic gates impose higher structural complexity for achieving robust and low-power circuits [3]. In response, significant research efforts have been devoted to develop p-type transistors using metal oxides [4-6], two-dimensional (2D) transition metal dichalcogenides [7-11], and metal-halide perovskites [12, 13]. Nevertheless, metal oxide-based p-type TFTs typically suffer from low carrier mobility, while the susceptibility of metal-halide perovskites to moisture and organic molecules brings long-term stability issues.

Recent years have witnessed a resurgence of interest in tellurium (Te), an elemental non-layered 2D material for advanced electronics, owing to its intrinsic p-type conductivity and small effective hole mass [11, 14-18]. Notably, large-area Te films with high crystalline quality can be readily synthesized via industry-compatible thermal evaporation [19], magnetron sputtering [20], and atomic layer deposition methods [21-23]. Recent advances in p-type Te field-effect transistors have demonstrated remarkable

hole mobility exceeding 10^3 cm^2 V^{-1} s^{-1} [24, 25]. However, this exceptional charge transport capability always comes at the expense of compromised switching characteristics, typically exhibiting limited room-temperature on/off ratio (< 10^4) and elevated off-state leakage current (> 10^{-9} A μm^{-1}) that fall short of the basic requirement for low-power logic circuit operation. These limitations fundamentally originate from the inherent properties of bulk Te, including its narrow bandgap (~0.35 eV) and high background carrier concentration (~10^{18} cm^{-3}) at room temperature [16, 26, 27]. A common approach to mitigate this issue involves thinning Te down to quantum limit to induce bandgap enlargement, which generally necessitates a material thickness less than ~6 nm [20, 28-33]. However, depositing continuous Te films with a few nanometers thickness on common dielectric substrates (e.g., SiO_2, Al_2O_3) is technically challenging because of its preferential island growth mode during the early nucleation stage [21, 34-36]. Furthermore, spontaneous surface oxidation intensifies at reduced thickness, significantly degrading the charge transport properties of ultrathin Te [20]. Consequently, the devices must be elaborately encapsulated with atomic layer deposited Al_2O_3 passivation layer, introducing additional fabrication complexity.

Se-alloying provides a viable strategy to circumvent the limitations associated with Te, as critical properties such as alloy bandgap and carrier density can be precisely controlled through atomic ratio modulation [37-39]. While early studies on $Te_{1-x}Se_x$ alloys primarily focus on short-wave infrared optoelectronics [40-43], their applications in p-type TFTs have only emerged in the past two years. For example, Liu et al. reported the thermal deposition of Se-alloyed Te-TeO_x films for amorphous p-channel TFTs, achieving a field-effect hole mobility of approximately 15 cm^2 V^{-1} s^{-1} [44]. Meng et al. implemented oxygen implantation in evaporated Te-Se alloy films to synthesize TeSeO with different compositions. The optimized $Te_{0.8}Se_{0.2}O_{0.8}$ exhibits a high hole mobility of 48.5 cm^2 V^{-1} s^{-1} while maintaining on/off current ratio of ~10^5 [45]. Choi et al. synthesized 60 nm-thick $Te_{0.5}Se_{0.5}$ film using pulsed laser deposition method, resulting in a field-effect mobility of 3 cm^2 V^{-1} s^{-1} [34]. Despite these achievements, $Te_{1-x}Se_x$ TFTs still face challenges of high off-state currents that typically lead to nW-level static power consumption in inverters. Moreover, wafer-scale fabrication of $Te_{1-x}Se_x$ TFTs-based low-power complementary logic gates and their corresponding demo applications remain largely unexplored.

In this work, we demonstrate scalable p-type $Te_{1-x}Se_x$ thin-film transistors and their implementation in low-power complementary logic circuits. The effect of composition and channel thickness on the transport properties of $Te_{1-x}Se_x$ TFTs was systematically investigated. Optimized $Te_{0.63}Se_{0.37}$ TFT with a channel thickness of ~22 nm exhibits favorable trade-off between charge transport and switching characteristics, exhibiting an average field-effect mobility of 16.8 cm^2 V^{-1} s^{-1} and a current on/off ratio of 1.3×10^5, while maintaining a low off-state current of 10 pA μm^{-1}. Notably, the fabrication process reveals full compatibility with low-temperature TFT technologies, enabling wafer-scale production of transistor arrays with favorable electrical uniformity. Furthermore, the devices exhibit remarkable environmental stability, key performance metrics of TFTs can be well retained after six months of ambient storage without encapsulation. Complementary logic gates including inverter (NOT), NAND, and NOR are further demonstrated using p-$Te_{0.63}Se_{0.37}$ and n-IGZO TFTs. The resulting inverters show favorable performance metrics, including a voltage gain of 28, a noise margin of 92.3%, and a low static power consumption of 420 pW at the supply voltage of 3 V. This study highlights the potential of $Te_{1-x}Se_x$ as scalable and cost-effective p-type channel materials, paving the way for broader applications of complementary TFTs logic circuits.

2 Experimental

2.1 Deposition of $Te_{1-x}Se_x$ film and TFTs fabrication

$Te_{1-x}Se_x$ thin films were deposited via thermal evaporation as described in our prior work [42]. First, bulk $Te_{1-x}Se_x$ alloy ingot was synthesized by vacuum-sealing stoichiometric mixture of high-purity Te and Se powders at various Te: Se mass ratios (19:1, 18:2, 17:3, 15: 5, and 14: 6 g) in a quartz tube, followed by heating at 560 °C for 12 hours in a muffle furnace and subsequently furnace-cooled to room temperature. The resulting ingot was crushed into small pieces and utilized as the source material for thermal evaporation. Prior to film deposition, the chamber was evacuated to a base pressure below 5×10^{-4} Pa, and the substrate was maintained at the room temperature. The deposition rate was controlled at around 2-10 Å s^{-1}. SiO_2/p^{++}-Si substrates with an oxide thickness of 300 nm were used for bottom-gate TFTs fabrication. The patterned channels were defined through maskless UV lithography (UV Litho-ACA, TuoTuo Technology). The $Te_{1-x}Se_x$ films were deposited on the SiO_2 surface following the aforementioned procedure and annealed on hot plate in a N_2 glove box at 100 °C for 10 min. Finally, 70 nm-thick Au source and drain electrodes were deposited via magnetron sputtering.

2.2 Fabrication of complementary logic gates

All the complementary logic gates were fabricated via standard microfabrication processes. For the inverters, a heavily-doped p^{++}-Si substrate was used as the bottom-gate electrode with a 30 nm-thick atomic-layer-deposited HfO_2 as the dielectric layer. Specifically, the HfO_2 deposition was carried out at 150 °C with H_2O and tetrakis(dimethylamino)hafnium as precursors. Subsequently, an 80-nm-thick n-type IGZO channel (In: Ga: Zn: O atomic ratio=1:1:1:4) was deposited by magnetron sputtering. Prior to deposition, the chamber was evacuated to a base pressure below 8×10^{-8} mbar. Sputtering was performed at a working pressure of 5×10^{-3} mbar with Ar and O_2 flow rates of 10 and 1.1 sccm, respectively, yielding a deposition rate of 0.6 Å s^{-1}. The as-deposited samples were then annealed in ambient air at 290 °C for 10 min. Source and drain contacts were defined using 70-nm-thick Mo. Finally, a p-type $Te_{0.63}Se_{0.37}$ TFT with a 16-nm-thick channel was fabricated as described above. The NAND and NOR logic gates were constructed on SiO_2/p^{++}-Si substrate with pre-patterned 70 nm Au serving as the local gate electrode. The other fabrication processes followed the same methodology as the inverters except for different circuit architectures.

Just Accepted

2.3 Material and device performance characterizations

The channel material thickness in TFTs is measured by atomic force microscope (AFM). The crystal structure and chemical states of the deposited $Te_{1-x}Se_x$ film were characterized by X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS). Because the vapor pressures of Se and Te differ substantially [37], the composition of deposited films can deviate from the nominal stoichiometry and is further affected by the alloying process, thermal deposition rate, and annealing conditions. Therefore, the actual Te: Se atomic ratios were determined by energy-dispersive X-ray spectroscopy (EDX) coupled with scanning electron microscopy (SEM) (Fig. S1 in the Electronic Supplementary Material (ESM)). Raman spectra of the $Te_{1-x}Se_x$ film were obtained using the 532 nm excitation laser. It is noted that thick films were used for these characterization analyses to ensure signal quality. The electrical characteristics of TFTs and inverters were measured using Keithley 4200 coupled with probe station, while the input and output waveforms for NAND and NOR logic gates were evaluated with Keysight B1500 semiconductor parameter analyzer. All the electrical measurements were conducted at room temperature under ambient conditions.

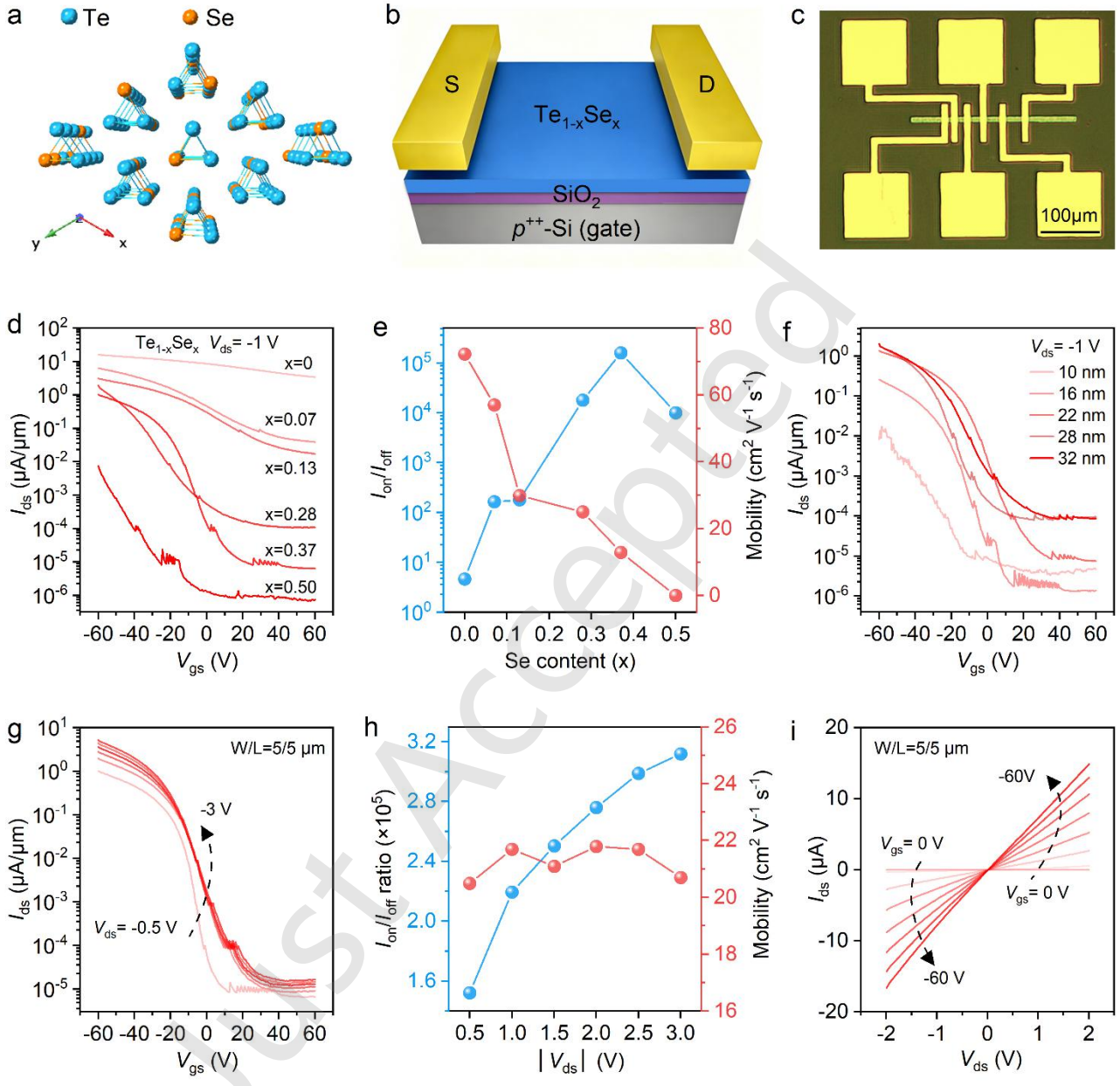


Figure 1 Electrical characterizations of $Te_{1-x}Se_x$ TFTs fabricated on SiO_2/p^{++}-Si substrate. (a) Schematic crystal structure of $Te_{1-x}Se_x$ alloy. (b) Cross-sectional schematic of the $Te_{1-x}Se_x$ TFT. (c) Optical microscopy image of a $Te_{1-x}Se_x$ TFT. (d) Transfer characteristics of $Te_{1-x}Se_x$ TFTs with different stoichiometric ratios. (e) I_{on}/I_{off} ratio and carrier mobility extracted from the curves in (d). (f) Thickness-dependent transfer characteristics of $Te_{0.63}Se_{0.37}$ TFTs. (g) Representative transfer characteristics of a $Te_{0.63}Se_{0.37}$ TFT with a channel thickness of ~22 nm. (h) I_{on}/I_{off} ratio and carrier mobility extracted from (g). (i) Output characteristics of the $Te_{0.63}Se_{0.37}$ TFT.

3 Results and discussion

Both Te and Se crystallize in an isomorphic hexagonal lattice characterized by one-dimensional helical chains oriented along the crystallographic *c*-axis (Fig. 1(a)). Their complete

Just Accepted

miscibility across the entire compositional range enables the synthesis of $Te_{1-x}Se_x$ alloys with continuously tunable physicochemical properties. In this study, $Te_{1-x}Se_x$ thin films with Se atomic fractions (x) varying from 0 to 0.50 were fabricated and characterized using Raman spectroscopy (Fig. S2 in the ESM). The spectrum of pure Te exhibits characteristic peaks at 93.6 cm^{-1} (E_1-TO), 122.8 cm^{-1} (A_1), and 142.3 cm^{-1} (E_2). Upon increasing the Se molar fraction, the Te-like A_1 and E_2 modes exhibit a progressive blue-shift and

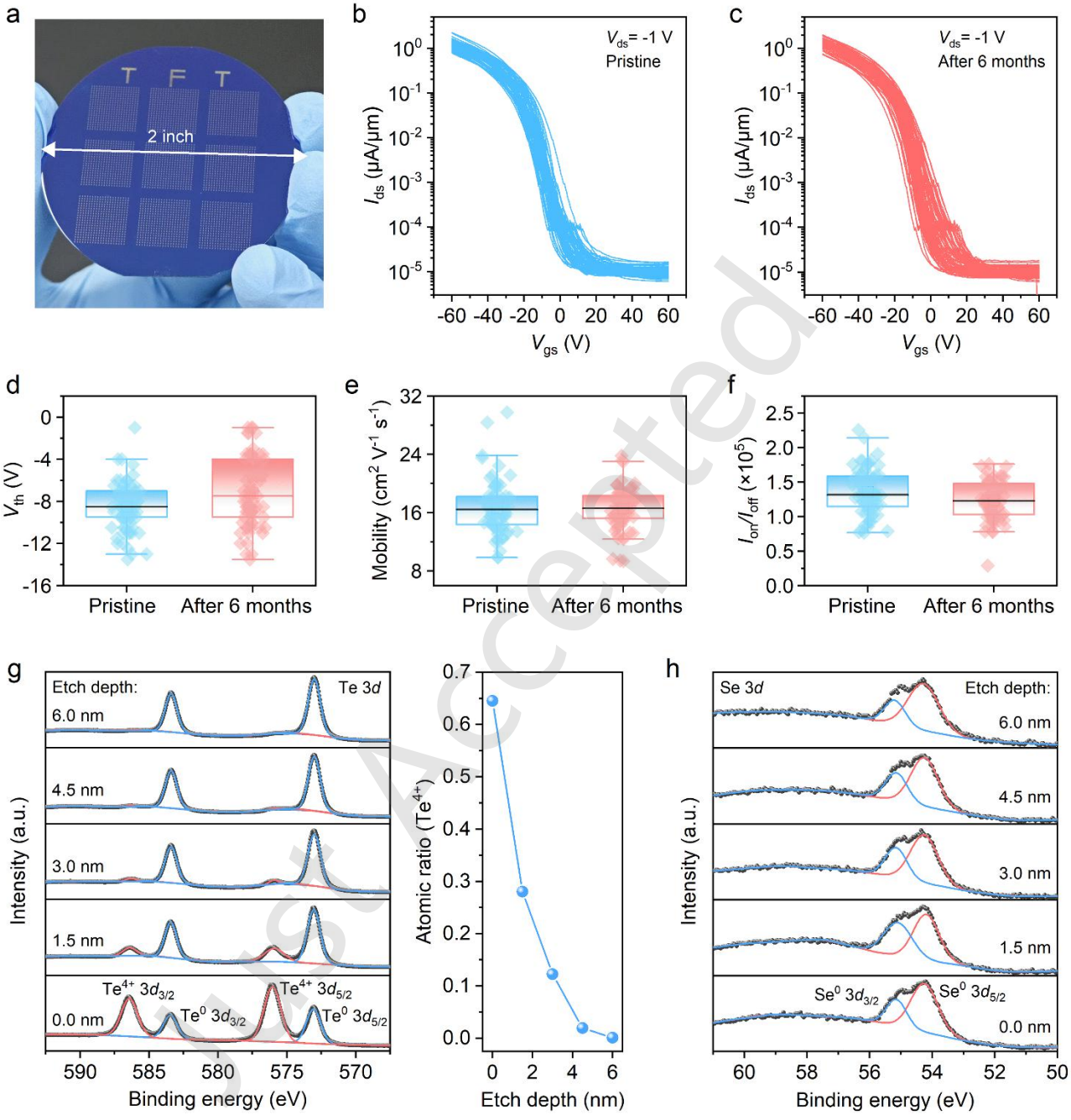


Figure 2 Wafer-scale $Te_{0.63}Se_{0.37}$ TFTs and environmental stability. (a) 22 nm-thick $Te_{0.63}Se_{0.37}$ TFT arrays fabricated on a 2-inch SiO_2/p^{++}-Si wafer. W/L=5 μm/5 μm. (b) Statistical transfer characteristics of 70 randomly selected transistors. (c) Transfer characteristics of the devices after six months of storage without encapsulation. (d-f) Statistical distribution of key performance metrics, including V_{th}, μ_{eff}, and I_{on}/I_{off} ratio. Depth-profiling XPS spectra of the $Te_{0.63}Se_{0.37}$ film for the (g) Te 3*d* and (h) Se 3*d* core levels.

eventually merge into a single broadened peak. Concurrently, a Se-like E_2 mode emerges with its intensity increases monotonically with Se concentration. Notably, no characteristic peaks of pure Te or Se phases are observed in the $Te_{1-x}Se_x$ spectra, indicating the formation of a homogeneous alloy composed of covalent Te-Se chains rather than a physical mixture of elemental Te and Se. To evaluate macroscopic uniformity, Raman mapping was performed across a $Te_{0.63}Se_{0.37}$ film deposited on a 2-inch SiO_2/p^{++} Si wafer (Fig. S3 in the ESM). Statistical analysis of the Se-like E_2 mode (175.4 cm^{-1}) from 100 stochastic measurements reveals minimal intensity fluctuations, indicating favorable compositional homogeneity requisite for large-scale TFT arrays integration.

The as-deposited $Te_{1-x}Se_x$ thin films typically exist in a quasi-amorphous structure, especially at high Se contents,

Just Accepted

which is primarily attributed to the superior room-temperature crystallization kinetics of Te relative to Se [38]. Consequently, post-thermal annealing is imperative to induce recrystallization and enhance film quality. As demonstrated by the XRD patterns of $Te_{0.63}Se_{0.37}$ film, distinct diffraction peaks corresponding to the (100) and (101) lattice planes emerge at a mild annealing temperature of 100 °C. Maintaining this low annealing temperature is critical, as higher thermal budgets trigger pinhole formation in the ultrathin FET channel layer and cause the film to become discontinuous at 150 °C (Fig. S4 in the ESM). Complementary SEM and AFM characterizations (Fig. S5 in the ESM) reveal a well-defined polycrystalline morphology with an average lateral grain size of ~1.0 μm and a root-mean-square roughness (S_q) of ~5.1 nm.

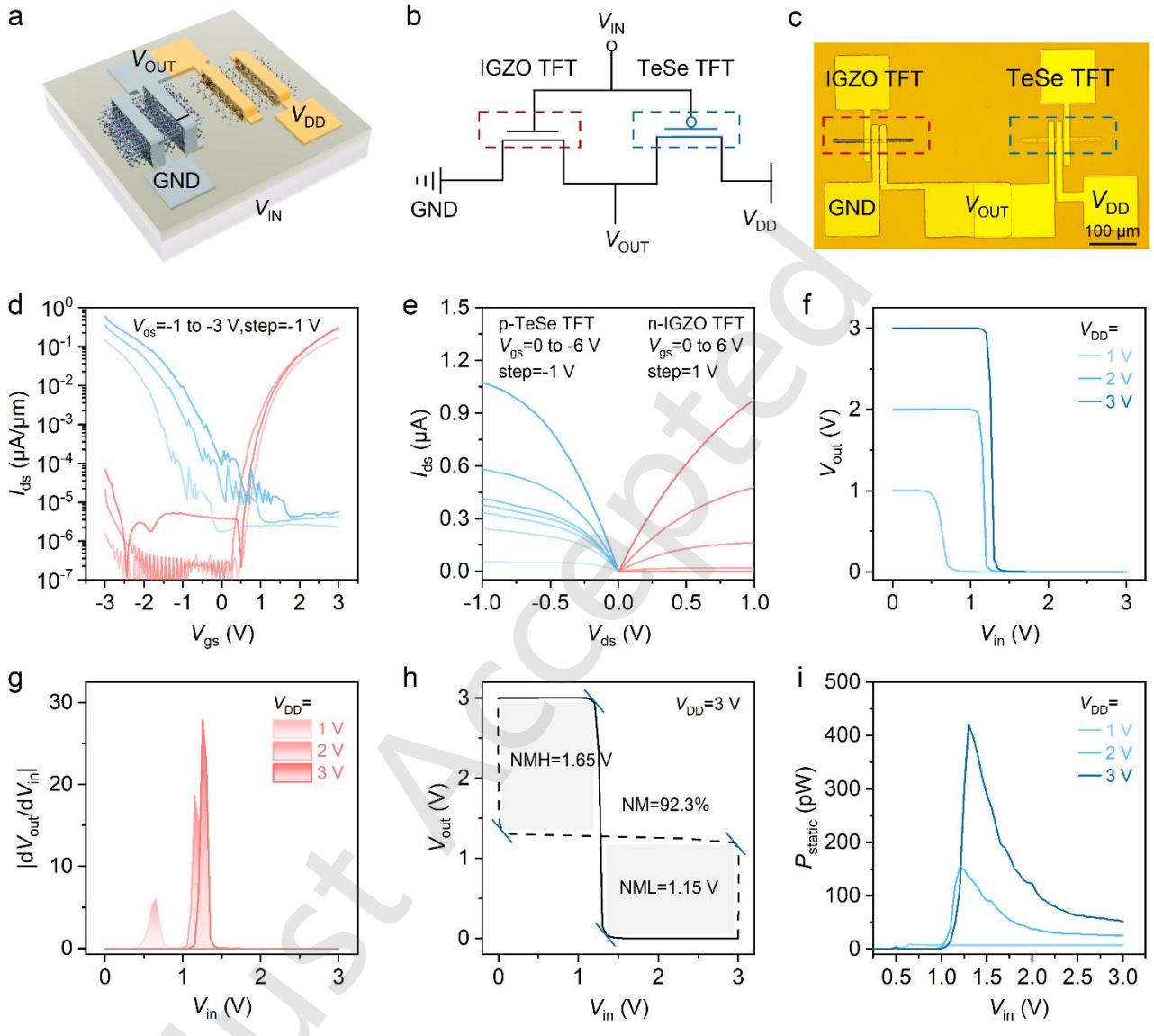


Figure 3 Performance of complementary inverter based on p-$Te_{0.63}Se_{0.37}$ and n-IGZO TFTs. (a) Schematic device structure. (b) Circuit diagram and (c) optical image of the inverter fabricated on a p^{++}-Si substrate with ALD-deposited HfO_2 as dielectric layer. (d) Transfer and (e) output characteristics of the constituent p-$Te_{0.63}Se_{0.37}$ and n-IGZO transistors. (f) The voltage transfer characteristics and (g) corresponding gain plots of the logic NOT at supply voltages V_{DD} of 1, 2, and 3 V. (h) Noise margin of the inverter at a V_{DD} of 3 V. (i) Static power consumption at V_{DD} values of 1, 2, and 3 V.

A schematic illustration of the bottom-gate $Te_{1-x}Se_x$ TFT architecture and a representative optical microscopy image are presented in Figs. 1(b) and 1(c). Figure 1(d) displays the transfer characteristics of $Te_{1-x}Se_x$ TFTs as a function of Se concentration, with all devices exhibiting typical p-type transport behavior. Notably, compared to the pristine Te counterparts, Se alloying significantly enhances the gate controllability of the TFTs, accompanied by a systematic negative shift in the threshold voltage (V_{th}) with increasing Se content. This modulation is consistent with the Se-induced widening of energy bandgap and the concurrent suppression of native acceptor state densities within the alloyed $Te_{1-x}Se_x$ channels (Fig. S6 in the ESM) [41, 42]. A comprehensive analysis of the current I_{on}/I_{off} ratio and carrier mobility is summarized in Fig. 1(e). Among the investigated compositions, $Te_{0.63}Se_{0.37}$ TFTs deliver a favorable balance between charge transport and switching characteristics. Specifically, lowering the Se content enhances both the I_{on} and mobility. However, the overall transistor performance is severely compromised by an associated increase in the I_{off} current to nA regime, rendering

Just Accepted

these low-Se compositions unsuitable for low-power electronics. Conversely, increasing the Se content effectively suppresses the off-state current but at the cost of a marked reduction in carrier mobility.

The thickness-dependent performance of $Te_{0.63}Se_{0.37}$ TFTs was further investigated, as shown in Fig. 1(f). Analogous to behavior reported in other low-dimensional semiconductors, devices featuring thicker channel (> 28 nm) exhibit a simultaneous increase in both I_{on} and I_{off}, yielding a current switching ratio of approximately 10^4. On the other hand, for ultrathin channel devices (< 10 nm), a pronounced degradation in I_{on} is observed. This performance degradation could be attributed to the higher relative surface roughness of ultrathin films compared to their thicker counterparts, alongside the spontaneous formation of an amorphous, poorly conducting native TeO_2 layer on the channel surface. This oxide layer reduces the effective conductive channel thickness, as validated in the subsequent section. Balanced electrical characteristics alongside a high current on/off ratio of over 10^5 are achieved in $Te_{0.63}Se_{0.37}$ TFTs with a channel thickness of approximately 16-22 nm.

Representative transfer characteristics of a 22-nm-thick $Te_{0.63}Se_{0.37}$ TFT (W/L=5 μm/5 μm) are presented in Fig. 1(g). Across source-drain voltage (V_{ds}) ranging from -0.5 V to -3 V, the device consistently maintains a high on/off current ratio of approximately (2.2±0.8) ×10^5. Notably, at V_{ds} =-0.5 V, the width-normalized I_{off} is as low as ~6.6 pA μm^{-1}, with an effective field-effect hole mobility (μ_{eff}) of approximately 20.5 $cm^2 V^{-1} s^{-1}$. Remarkably, a robust μ_{eff} exceeding 20 $cm^2 V^{-1} s^{-1}$ is sustained across the entire V_{ds} bias range (Fig. 1(h)). A thinner 16-nm-thick $Te_{0.63}Se_{0.37}$ TFT was also evaluated (Fig. S7 in the ESM), which similarly exhibits a high I_{on}/I_{off} of over 10^5 and a fair μ_{eff} of ~17 $cm^2 V^{-1} s^{-1}$. The output characteristics of the 22-nm-thick $Te_{0.63}Se_{0.37}$ TFT are presented in Fig. 1(i), displaying a strong gate-voltage dependence of the drain current. However, at V_{gs} = 0 V, the output curves exhibit pronounced nonlinearity in the low V_{ds} region (Fig. S8 in the ESM), which is attributed to the substantial Schottky barrier at the Au/$Te_{0.63}Se_{0.37}$ interface. Additionally, the high solubility of Te in Au and the easy formation of Te-Au alloy may also deteriorate the interfacial contact properties [46]. Transmission line method (TLM) measurements reveal a contact resistance of approximately 94 kΩ at V_{gs}=-60 V (Fig. S9 in the ESM). To further investigate this Au/$Te_{0.63}Se_{0.37}$ interface, temperature-dependent transfer curves of the transistor were characterized, revealing a large barrier height of ~50 mV (Fig. S10 in the ESM). Consequently, minimizing contact barrier height is a critical strategy for optimizing the charge transport properties of $Te_{1-x}Se_x$ TFTs. Although it is beyond the scope of this work, employing a transferred high work function electrode technique may offer an effective pathway to mitigate this issue [47].

Furthermore, the scalability and environmental stability of the $Te_{0.63}Se_{0.37}$-based TFTs were evaluated. The devices are readily fabricated via standard photolithography, thermal deposition, and lift-off processes, highlighting their full compatibility with mature TFT manufacturing technologies. Figure 2(a) presents an optical photograph of wafer-scale $Te_{0.63}Se_{0.37}$ TFT arrays fabricated on a 2-inch SiO_2/p^{++}-Si substrate. Transfer characteristics of 70 randomly selected transistors were measured, demonstrating favorable device-to-device uniformity, alongside an average field-effect mobility of 16.8 $cm^2 V^{-1} s^{-1}$, I_{on}/I_{off} ratio of 1.3×10^5 and a low off-state current of 10 pA μm^{-1}. (Fig. 2(b)). Crucially, as illustrated in Fig. 2(c), these unencapsulated TFTs exhibit exceptional environmental stability, displaying negligible degradation even after six months of desiccator storage under ambient conditions (25 ℃, 30% relative humidity). Figs. 2(d)-(f) show the statistical distribution and comparison of key TFT electrical metrics (V_{th}, μ_{eff}, and I_{on}/I_{off} ratio) between pristine and aged devices. All the critical parameters remain tightly distributed with minimal performance fluctuations over time.

To elucidate the origin of the favorable ambient stability observed in these TFTs, depth-resolved XPS spectra of the $Te_{0.63}Se_{0.37}$ film were acquired, as shown in Figs. 2(g)-(h). The Te 3*d* spectrum of as-deposited film exhibits coexisting Te^{4+} and Te^0 peaks, confirming partial oxidation of Te element [20]. Conversely, owing to the higher oxophilicity of Te relative to Se, no Se^{4+} oxidation peaks (~60 eV) are observed in the Se 3*d* spectra [39, 45]. It is supposed that the resulting amorphous TeO_2 on the channel surface could function as a native, self-limiting passivation layer that suppresses inward oxygen diffusion, which plays a critical role in sustaining the robust environmental stability of $Te_{0.63}Se_{0.37}$ TFTs. A pronounced attenuation in both the Te^{4+} signal intensity and its corresponding atomic fraction was observed with increasing Ar^+ etching depth, with the oxide feature vanishing almost completely beyond an etch depth of ~6.0 nm (Fig. 2(g)). This reveals that the oxidation is preferentially confined to the surface, consistent with the cross-sectional transmission electron microscopy analysis (Fig. S11 in the ESM). This surface-localized oxidation model also elucidates the severely degraded electrical transport properties observed in the ultrathin-channel $Te_{0.63}Se_{0.37}$ TFT shown in Fig. 1(f).

To evaluate the application feasibility of p-$Te_{0.63}Se_{0.37}$ TFTs for scalable logic gates, complementary inverters by integrating them with well-established n-IGZO TFTs were constructed (Fig. 3(a)). The fabrication processes for both p- and n-channel devices exhibit full compatibility, enabling the monolithic integration of inverter arrays on a centimeter-scale p^{++}-Si substrate via standard photolithography, thin-film deposition, and lift-off techniques (Fig. S12 in the ESM). The p^{++}-Si serves as the common bottom-gate electrode and ALD-grown 30 nm HfO_2 as dielectric layer (Fig. 3(b) and Fig. 3(c)). To ensure optimal complementary logic operation, the electrical characteristics of the constituent p- and n-type TFTs were carefully matched by optimizing the channel thickness and device geometry. As evidenced by the transfer and output characteristics in Figs. 3(d)-(e), the p-$Te_{0.63}Se_{0.37}$ and n-IGZO TFTs exhibit well-balanced on-state and off-state current, comparable switching ratios (10^5-10^6), and almost symmetric transfer profiles centered near 0.5 V gate bias. Figure 3(f) presents the voltage transfer characteristics (VTCs) of the inverter operating at supply voltages (V_{DD}) of 1, 2, and 3 V, demonstrating sharp rail-to-rail switching behavior.

Taking the operation at V_{DD}=3 V as an example, the output voltage (V_{out}) is maintained at 3.0005±0.0005 V under a low input voltage (V_{in}) bias, which is exceptionally close to the

Just Accepted

ideal V_{DD}. Once the V_{in} exceeds the switching threshold voltage, the V_{out} undergoes an abrupt transition to an ultralow off-state voltage of ~0.2 mV (close to the ground potential V_{GND}). This sharp voltage transition yields a high gain ($|dV_{out}/dV_{in}|$) of 28 at V_{DD}=3 V (Fig. 3(g)). Furthermore, a high-state noise margin (NMH) of ~1.62 V and a low-state noise margin (NML) of ~1.15 V are extracted, accounting for a total noise margin (NM) of 92.3% relative to V_{DD} (Fig. 3(h)). This outstanding noise tolerance ensures reliable operation in electrically noisy environments. Another key advantage of this complementary inverter is its minimized static power dissipation. Because both the p-$Te_{0.63}Se_{0.37}$ and n-IGZO transistors exhibit suppressed off-state currents on the order of pA μm^{-1}, only a negligible static current (I_{static}) flows from V_{DD} to the ground across all input states. As illustrated in Fig. 3(i), the peak static power consumption of the inverter is ~420 pW at V_{DD}=3 V, which is much lower than previously reported Te-based inverters (Table S1 in the ESM), highlighting the potential of $Te_{1-x}Se_x$ for low-power logic circuitry [20, 30, 33].

In addition to basic inverters, two other fundamental logic gates (NAND and NOR) were also implemented by combining p-

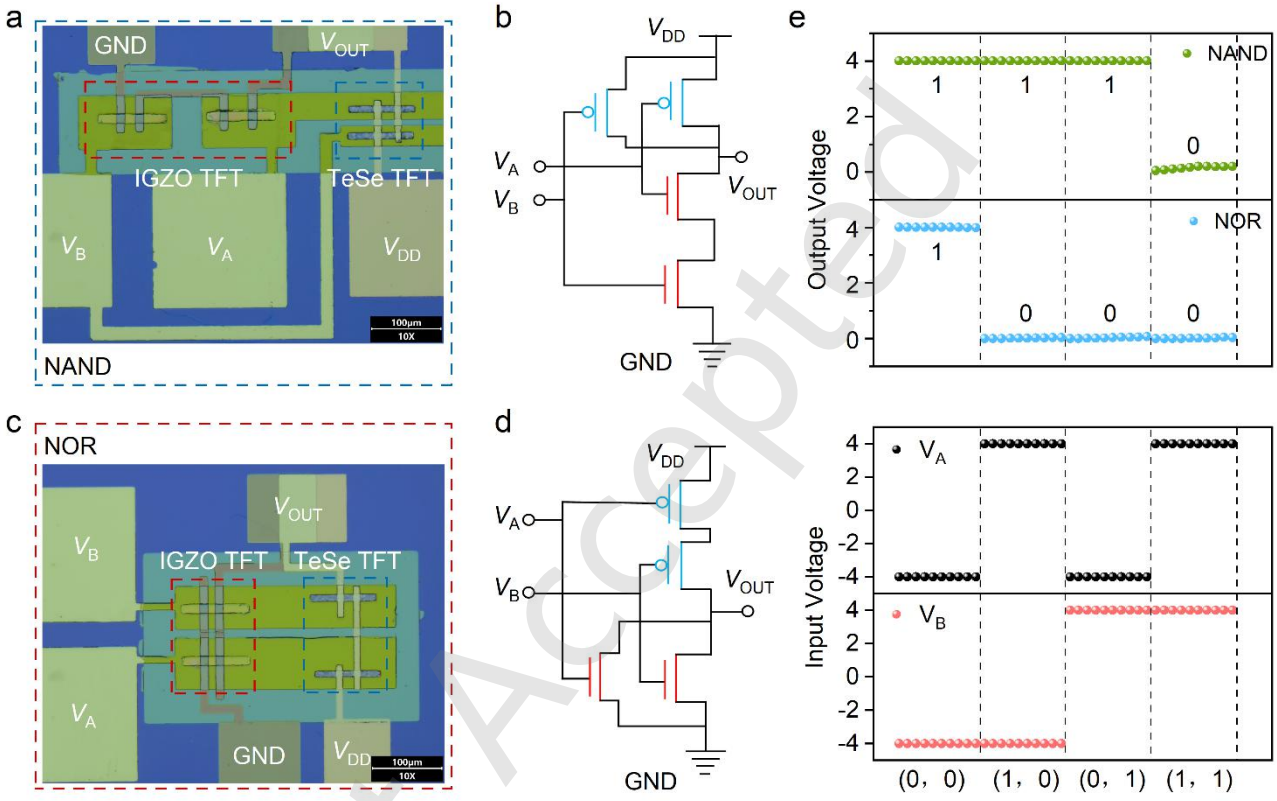


Figure 4 Complementary NAND and NOR logic gates with monolithically integrated p-$Te_{0.63}Se_{0.37}$ and n-IGZO TFTs. (a) Optical microscopy image and (b) schematic circuit diagram of the NAND logic gate. (c) Optical microscopy image and (d) schematic circuit diagram of the NOR logic gate. (e) Input voltage signals (bottom) and corresponding output voltage waveforms (top) of NAND and NOR logic gates.

$Te_{0.63}Se_{0.37}$ and n-IGZO TFTs. The fabrication process for these multi-input logic gates similarly follows that of the complementary inverters except that utilizing a common SiO_2/p^{++}-Si substrate, pre-patterned Au as local bottom gate electrodes, and an ALD-deposited 30 nm-thick HfO_2 as gate dielectric layer. As illustrated in Figs. 4(a)-(b), The NAND gate integrates two series-connected n-IGZO and two parallel-connected p-$Te_{0.63}Se_{0.37}$ transistors. This configuration executes the following logic operation: the output switches to a logic-low state "0" only when both input signals V_A (gate voltage of n-IGZO TFT) and V_B (gate voltage of p-$Te_{0.63}Se_{0.37}$ TFT) are simultaneously biased to the logic-high state "1". For all other permuted input combinations ("00", "01", "10"), the output remains at the logic-high state "1". Conversely, the NOR gate comprises two parallel-connected n-IGZO TFTs and two series-connected p-$Te_{0.63}Se_{0.37}$ TFTs (Figs. 4(c)-(d)). Its logic operation is defined such that the output reaches a logic-high state "1" exclusively when both inputs V_A and V_B are at the logic-low state "0". For all other input conditions ("01", "10", "11"), the output is maintained at the logic-low state "0". Figure 4(e) (bottom) displays the applied two square-wave input voltage signals (V_A and V_B) with amplitudes of -4 V (low) and 4 V (high), which correspond to logic "0" and "1", respectively. The resulting output voltage waveforms at a V_{DD} of
4 V are shown in Fig. 4(e) (top), which exhibit well-defined logic-level separation with negligible voltage degradation. Both the NAND and NOR gates consistently produce the expected output logic states that align precisely with their theoretical Boolean truth tables. The successful implementation of fully functional complementary logic gates forms the essential foundation for building more complex digital circuits, such as adders, shift registers, and even microprocessors.

4 Conclusions

Just Accepted

In summary, we demonstrate scalable p-$Te_{1-x}Se_x$ TFTs featuring electrical uniformity and their successful integration into low-power complementary logic gates. Through systematic investigation of alloy composition and channel thickness, we achieve an optimal balance between charge transport and switching characteristics, yielding TFTs with an average field-effect mobility of 16.8 $cm^2\ V^{-1}\ s^{-1}$, a current on/off ratio of 1.3×10^5 and a suppressed off-state current of 10 pA/μm. Remarkably, the unencapsulated devices exhibit favorable environmental stability, retaining critical performance metrics after six months of ambient exposure. This robust ambient tolerance is credited to the spontaneous formation of a self-limiting TeO_2 layer on the $Te_{0.63}Se_{0.37}$ channel surface, which acts as a passivating barrier against further atmospheric degradation. Leveraging this platform, fully functional complementary logic gates NOT, NAND, and NOR are implemented by integrating p-$Te_{0.63}Se_{0.37}$ with n-IGZO TFTs. At a V_{DD} of 3 V, the inverter exhibits a high voltage gain of 28, a noise margin of 92.3%, and a low static power consumption of 420 pW. This study underscores the potential of $Te_{1-x}Se_x$ as a scalable and cost-effective p-type channel material, advancing the development of TFT-based low-power logic circuits.

Electronic Supplementary Material: Supplementary material (Figures S1–S12 and Table S1) is available in the online version of this article at https://doi.org/10.26599/NR.2026.94909305.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and/or the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

Acknowledgements

This work is financially supported by the Henan Provincial Key Science and Technology Research Projects (Grant No. 252102211102), State Key Laboratory for Advanced Metals and Materials (Grant No. 2025-Z11), National Natural Science Foundation of China (52302162, U22A20138, 62561160157, 62374149, 12504496), Natural Science Foundation of Henan Province (252300421059, 252300421292), Shenzhen Science and Technology Innovation Commission, Shenzhen Fundamental Research (Project No.: JCYJ20241202130542054), NSFC/RGC Joint Research Scheme (N_PolyU533/25), Photonics Research Institute, PolyU (Project No.: CD9W).

Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

P. L.: Conceptualization, methodology, funding acquisition, writing - original draft. Y. W.: Investigation, data curation, formal analysis, visualization. Y. B. H.: Investigation, validation, formal analysis. J. L. D.: Writing - review & editing, funding acquisition. Z. J. X.: Formal analysis. Z. W. Z.: Writing - review & editing, formal analysis. Q. Y. T.: Writing - review & editing. C. J. K.: Investigation, formal analysis. D. W., L. H. Z. and Y. H. T.: Funding acquisition, writing - review & editing. Y. W. and Y. B. H. contributed equally to this work. All authors have reviewed and approved the final manuscript.

Use of AI statement

None.

References

[1] Geng, D.; Wang, K.; Li, L.; Myny, K.; Nathan, A.; Jang, J.; Kuo, Y.; Liu, M. Thin-film transistors for large-area electronics. *Nat. Electron.* **2023**, *6*, 963-972.

[2] Çeliker, H.; Dehaene, W.; Myny, K. Multi-project wafers for flexible thin-film electronics by independent foundries. *Nature* **2024**, *629*, 335-340.

[3] Myny, K. The development of flexible integrated circuits based on thin-film transistors. *Nat. Electron.* **2018**, *1*, 30-39.

[4] Mude, N.; Lee, J.; Cho, S. Recent advancements in p-type inorganic semiconductor thin-film transistors: A Review. *Crystals* **2025**, *15*, 341.

[5] Ouyang, Z.; Wang, W.; Dai, M.; Zhang, B.; Gong, J.; Li, M.; Qin, L.; Sun, H. Research progress of p-type oxide thin-film transistors. *Materials* **2022**, *15*, 4781.

[6] Xiong, Y.; Xu, D.; Zou, Y.; Xu, L.; Yan, Y.; Wu, J.; Qian, C.; Song, X.; Qu, K.; Zhao, T.; Gao, J.; Yang, J.; Zhang, K.; Zhang, S.; Wang, P.; Chen, X.; Zeng, H. Vapour-liquid-solid-solid growth of two-dimensional non-layered β-Bi_2O_3 crystals with high hole mobility. *Nat. Mater.* **2025**, *24*, 688-697.

[7] Xiong, Y.; Xu, D.; Feng, Y.; Zhang, G.; Lin, P.; Chen, X. P-type 2D semiconductors for future electronics. *Adv. Mater.* **2023**, *35*, 2206939.

[8] Wang, Y.; Kim, J. C.; Li, Y.; Ma, K. Y.; Hong, S.; Kim, M.; Shin, H. S.; Jeong, H. Y.; Chhowalla, M. P-type electrical contacts for 2D transition-metal dichalcogenides. *Nature* **2022**, *610*, 61-66.

[9] Wu, J.; Zhuge, F.; Li, H.; Zhai, T. Recent advances in two-dimensional p-type metal chalcogenides: synthesis, doping strategies and applications. *J. Phys. D: Appl. Phys.* **2023**, *56*, 023001.

[10] Zou, T.; Reo, Y.; Heo, S.; Jung, H.; Kim, S.; Liu, A.; Noh, Y.-Y. Monolithic three-dimensional integration with 2D material-based p-type transistors. *Mater. Sci. Eng.: R: Rep.* **2025**, *163*, 100893.

[11] Qu, K.; Zhang, Z.; Dai, Y.; Wang, X.; Lei, S.; Wang, X.; Li, J.; Zhang, K.; Duan, X.; Chen, X.; Zeng, H. Opportunities and challenges of 2D p-type semiconductors: from material systems to electronic and optoelectronic device applications. *Adv. Funct. Mater.* **2026**, *36*, e31994.

[12] Zhu, H.; Liu, A.; Shim, K. I.; Jung, H.; Zou, T.; Reo, Y.; Kim, H.; Han, J. W.; Chen, Y.; Chu, H. Y.; Lim, J. H.; Kim, H.-J.; Bai, S.; Noh, Y.-Y. High-performance hysteresis-free perovskite transistors through anion engineering. *Nat. Commun.* **2022**, **13**, 1741.

[13] Liu, A.; Zhu, H.; Bai, S.; Reo, Y.; Zou, T.; Kim, M.-G.; Noh, Y.-Y. High-performance inorganic metal halide perovskite transistors. *Nat. Electron.* **2022**, *5*, 78-83.

[14] Zha, J.; Dong, D.; Huang, H.; Xia, Y.; Tong, J.; Liu, H.; Chan, H. P.; Ho, J. C.; Zhao, C.; Chai, Y.; Tan, C. Electronics and optoelectronics based on tellurium. *Adv. Mater.* **2024**, *36*, 2408969.

[15] Zha, J.; Tong, J.; Huang, H.; Xia, Y.; Dong, D.; Tan, C. A Perspective on tellurium-based optoelectronics. *Appl. Phys. Lett.* **2024**, *125*, 070504.

[16] Wang, Y.; Qiu, G.; Wang, R.; Huang, S.; Wang, Q.; Liu, Y.; Du, Y.; Goddard, W. A.; Kim, M. J.; Xu, X.; Ye, P. D.; Wu, W. Field-effect transistors made from solution-grown two-dimensional tellurene. *Nat. Electron.* **2018**, *1*, 228-236.

[17] Liao, J.; Lai, Z.; Meng, Y.; Ho, J. C. Recent progress on elemental tellurium and its devices. *J. Semicond.* **2025**, *46*, 011605.

[18] Niu, C.; Long, L.; Zhang, Y.; Lin, Z.; Tan, P.; Lin, J.-Y.; Wu, W.; Wang, H.; Ye, P. D. Ultralow voltage operation of p- and n-FETs enabled by self-formed gate dielectric and metal contacts on 2D tellurium. *Adv. Mater.* **2025**, *37*, 2418142.

[19] Zhao, C.; Tan, C.; Lien, D.-H.; Song, X.; Amani, M.; Hettick, M.; Nyein, H. Y. Y.; Yuan, Z.; Li, L.; Scott, M. C.; Javey, A. Evaporated tellurium thin films for p-type field-effect transistors and circuits. *Nat. Nanotechnol.* **2020**, *15*, 53-58.

Not Accepted

[20] Kim, T.; Choi, C. H.; Byeon, P.; Lee, M.; Song, A.; Chung, K.-B.; Han, S.; Chung, S.-Y.; Park, K.-S.; Jeong, J. K. Growth of high-quality semiconducting tellurium films for high-performance p-channel field-effect transistors with wafer-scale uniformity. *npj 2D Mater. Appl.* **2022**, *6*, 4.

[21] Tran, D. C.; Pham, G. H.; Huong Chu, T. T.; Kim, J.; Jeong, J. K.; Im, S.; Lee, B. H.; Sung, M. M. Layer-by-layer growth of two-dimensional tellurium thin films via ultrahigh-pressure atomic layer deposition for p-type semiconductors. *Nano Lett.* **2024**, *24*, 16276-16282.

[22] Kim, M.; Lee, Y.; Kim, K.; Pham, G.-H.; Kim, K.; Jun, J. H.; Lee, H.-w.; Yoon, S.; Hwang, H. J.; Sung, M. M.; Lee, B. H. Processes to enable hysteresis-free operation of ultrathin ALD Te p-channel field-effect transistors. *Nanoscale Horiz.* **2024**, *9*, 1990-1998.

[23] Tan, P.; Niu, C.; Lin, Z.; Lin, J.-Y.; Long, L.; Zhang, Y.; Wilk, G.; Wang, H.; Ye, P. D. Wafer-scale atomic layer-deposited TeO_x/Te heterostructure p-type thin-film transistors. *Nano Lett.* **2024**, *24*, 12433-12441.

[24] Yang, P.; Zha, J.; Gao, G.; Zheng, L.; Huang, H.; Xia, Y.; Xu, S.; Xiong, T.; Zhang, Z.; Yang, Z.; Chen, Y.; Ki, D.-K.; Liou, J. J.; Liao, W.; Tan, C. Growth of tellurium nanobelts on h-BN for p-type transistors with ultrahigh hole mobility. *Nano-Micro Lett.* **2022**, *14*, 109.

[25] Zhang, X.; Yu, H.; Tang, W.; Wei, X.; Gao, L.; Hong, M.; Liao, Q.; Kang, Z.; Zhang, Z.; Zhang, Y. All-van-der-Waals barrier-free contacts for high-mobility transistors. *Adv. Mater.* **2022**, *34*, 2109521.

[26] Liu, A.; Zhu, H.; Zou, T.; Reo, Y.; Ryu, G.-S.; Noh, Y.-Y. Evaporated nanometer chalcogenide films for scalable high-performance complementary electronics. *Nat. Commun.* **2022**, *13*, 6372.

[27] Chen, F.; Cao, D.; Li, J.; Yan, Y.; Wu, D.; Zhang, C.; Gao, L.; Guo, Z.; Ma, S.; Yu, H.; Lin, P. Solution-processed thickness engineering of tellurene for field-effect transistors and polarized infrared photodetectors. *Front. Chem.* **2022**, *10*, 1046010.

[28] Lim, S.-H.; Kim, T. I.; Park, I.-J.; Kwon, H.-I. Synthesis of a tellurium semiconductor with an organic-inorganic hybrid passivation layer for high-performance p-type thin film transistors. *ACS Appl. Electron. Mater.* **2023**, *5*, 4816-4825.

[29] Kim, T.; Choi, C. H.; Kim, S. E.; Kim, J. K.; Jang, J.; Choi, S.; Noh, J.; Park, K. S.; Kim, J.; Yoon, S.; Jeong, J. K. High-performance hexagonal tellurium thin-film transistor using tellurium oxide as a crystallization retarder. *IEEE Electron Device Lett.* **2023**, *44*, 269-272.

[30] Lee, J.-Y.; Kim, T. I.; Kwon, H.-I.; Park, I.-J. Surface crystallization effects on tellurium oxide thin films for low-power complementary logic circuit applications. *Appl. Surf. Sci.* **2024**, *669*, 160536.

[31] Jeong, U.; Rho, H. Y.; Oh, J. o.; Daw, D.; Lee, Y.; Chung, K.-B.; Sen, A.; Kim, S. Plasma-engineered high-performance tellurium field-effect phototransistors. *Adv. Funct. Mater.* **2025**, *35*, 2421140.

[32] Jung, C.; Lee, J.; Heo, S. H.; Yoon, S. H.; Kim, T.; Sung, M. M.; Jeong, J. K. Scalable ternary logic device based on TeO_x/IGTO heterojunction transistor. *Adv. Funct. Mater.* **2025**, *35*, 2501834.

[33] Tang, Y.; Song, Y.; Zeng, L.; Lo, Y.-h.; Nomura, K. Wafer-scale high mobility 2D tellurium thin-film transistor for heterogeneous integrated 3D-CFET logic circuits. *Small* **2025**, *35*, 2504908.

[34] Choi, K.; Nam, S.; Kim, Y.-H.; Oh, H.; Kim, I.; Lee, K.; Cho, S. H. Promotion of processability in a p-type thin-film transistor using a Se-Te alloying channel layer. *ACS Appl. Mater. Interfaces* **2024**, *16*, 23459-23466.

[35] Zhao, C.; Batiz, H.; Yasar, B.; Ji, W.; Scott, M. C.; Chrzan, D. C.; Javey, A. Orientated growth of ultrathin tellurium by van der Waals epitaxy. *Adv. Mater. Interfaces* **2022**, *9*, 2101540.

[36] Ryu, S. H.; Kim, S.; Kim, T.; Jeon, J.; Park, G. M.; Yoo, H.; Kim, S.-C.; Won, S. O.; Kim, J.-Y.; Kim, S. K. Reductive transformation of ALD TeO_2 into continuous and impurity-free tellurium films. *Small* **2026**, *32*, e73470.

[37] Tan, C.; Amani, M.; Zhao, C.; Hettick, M.; Song, X.; Lien, D.-H.; Li, H.; Yeh, M.; Shrestha, V. R.; Crozier, K. B.; Scott, M. C.; Javey, A. Evaporated Se_xTe_{1-x} thin films with tunable bandgaps for short-wave infrared photodetectors. *Adv. Mater.* **2020**, *32*, 2001329.

[38] Geoffrion, L. D.; Guisbiers, G. Physico-chemical properties of selenium-tellurium alloys across the scales. *Nanoscale Adv.* **2021**, *3*, 4254-4270.

[39] Huang, H.; Zha, J.; Xu, S.; Yang, P.; Xia, Y.; Wang, H.; Dong, D.; Zheng, L.; Yao, Y.; Zhang, Y.; Chen, Y.; Ho, J. C.; Chan, H. P.; Zhao, C.; Tan, C. Precursor-confined chemical vapor deposition of 2D single-crystalline Se_xTe_{1-x} nanosheets for p-type transistors and inverters. *ACS Nano* **2024**, *18*, 17293-17303.

[40] Fu, L.; He, Y.; Zheng, J.; Hu, Y.; Xue, J.; Li, S.; Ge, C.; Yang, X.; Peng, M.; Li, K.; Zeng, X.; Wei, J.; Xue, D.-j.; Song, H.; Chen, C.; Tang, J. Te_xSe_{1-x} photodiode shortwave infrared detection and imaging. *Adv. Mater.* **2023**, *35*, 2211522.

[41] Li, R.; Yao, F.; Xu, Y.; Bai, S.; Jia, Z.; Lin, Q. Optimizing the charge carrier dynamics of thermal evaporated Te_xSe_{1-x} films for high-performance short-wavelength infrared photodetection. *Adv. Funct. Mater.* **2024**, *34*, 2307005.

[42] Guo, Z.; Wang, J.; Du, J.; Wu, D.; Zeng, L.; Tsang, Y. H.; Wu, D.; Wang, Y.; Ding, Y.; Lin, P. Self-driven $Te_{0.65}Se_{0.35}$/GaAs SWIR photodiode with spectral response to 1.55 μm for broadband imaging and optical communication. *Nano Energy* **2025**, *133*, 110452.

[43] Hu, M.; Duan, Y.; Li, S.; Yang, L.; Dong, W.; Dang, W.; Zhang, Z.; Liu, J.; Li, Z. Molecular engineering of hole-selective layer of Te_xSe_{1-x} for high-performance short-wave infrared photodetectors. *ACS Photonics* **2025**, *12*, 932-943.

[44] Liu, A.; Kim, Y.-S.; Kim, M. G.; Reo, Y.; Zou, T.; Choi, T.; Bai, S.; Zhu, H.; Noh, Y.-Y. Selenium-alloyed tellurium oxide for amorphous p-channel transistors. *Nature* **2024**, *629*, 798-802.

[45] Meng, Y.; Wang, W.; Fan, R.; Lai, Z.; Wang, W.; Li, D.; Li, X.; Quan, Q.; Xie, P.; Chen, D.; Shao, H.; Li, B.; Wu, Z.; Yang, Z.; Yip, S.; Wong, C.-Y.; Lu, Y.; Ho, J. C. An inorganic-blended p-type semiconductor with robust electrical and mechanical properties. *Nat. Commun.* **2024**, *15*, 4440.

[46] Rahman, I. K. M. R.; Kim, T.; Kim, I.; Higashitarumizu, N.; Wang, S.; Wang, S.; Kim, H. M.; Bullock, J.; Altoe, V.; Ager, J. W., III; Chrzan, D. C.; Javey, A. Thermally stable ruthenium contact for robust p-type tellurium transistors. *Nano Lett.* **2025**, *25*, 3956-3963.

[47] Ma, L.; Wang, Y.; Liu, Y. van der Waals contact for two-dimensional transition metal dichalcogenides. *Chem. Rev.* **2024**, *124*, 2583-2616.

© The Author(s) 20xx. *Nano Research* published by Tsinghua University Press. The articles published in this open access journal are distributed under the terms of the Creative Commons Attribution 4.0 International License (http://creativecommons.org/licenses/by/4.0/), which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

Just Accepted

Electronic Supplementary Material

Scalable p-type $Te_{1-x}Se_x$ thin-film transistors and low-power complementary logic gates

Yu Wang [1], Yubo Hao [1], Junli Du [2], Zhenjia Xie [3], Zhiwen Zhou [4] ✉, Quanyang Tao [1], Canjun Ke [1], Di Wu [1], Longhui Zeng [1], Yuen Hong Tsang [5,6] ✉, Pei Lin [1] ✉

[1] Henan Key Laboratory of Advanced Optoelectronic Materials and Devices, Key Laboratory of Materials Physics of Ministry of Education, School of Physics, Zhengzhou University, Zhengzhou 450052, China
[2] Academy for Advanced Interdisciplinary Science and Technology, University of Science and Technology Beijing, Beijing 100083, China
[3] State Key Laboratory for Advanced Metals and Materials, University of Science and Technology Beijing, Beijing 100083, China
[4] School of Materials Science and Engineering, Harbin Institute of Technology, Harbin 150001, China
[5] Department of Physics and Materials, Photonics Research Institute, Research Institute for Advanced Manufacturing, The Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong, China
[6] Shenzhen Research Institute, The Hong Kong Polytechnic University, Shenzhen 518057, China

Supporting information to https://doi.org/10.26599/NR.2026.94909305

Just Accepted

Address correspondence to Zhiwen Zhou, zwzhou@connect.hku.hk; Yuen Hong Tsang, yuen.tsang@polyu.edu.hk; Pei Lin, linpei@zzu.edu.cn

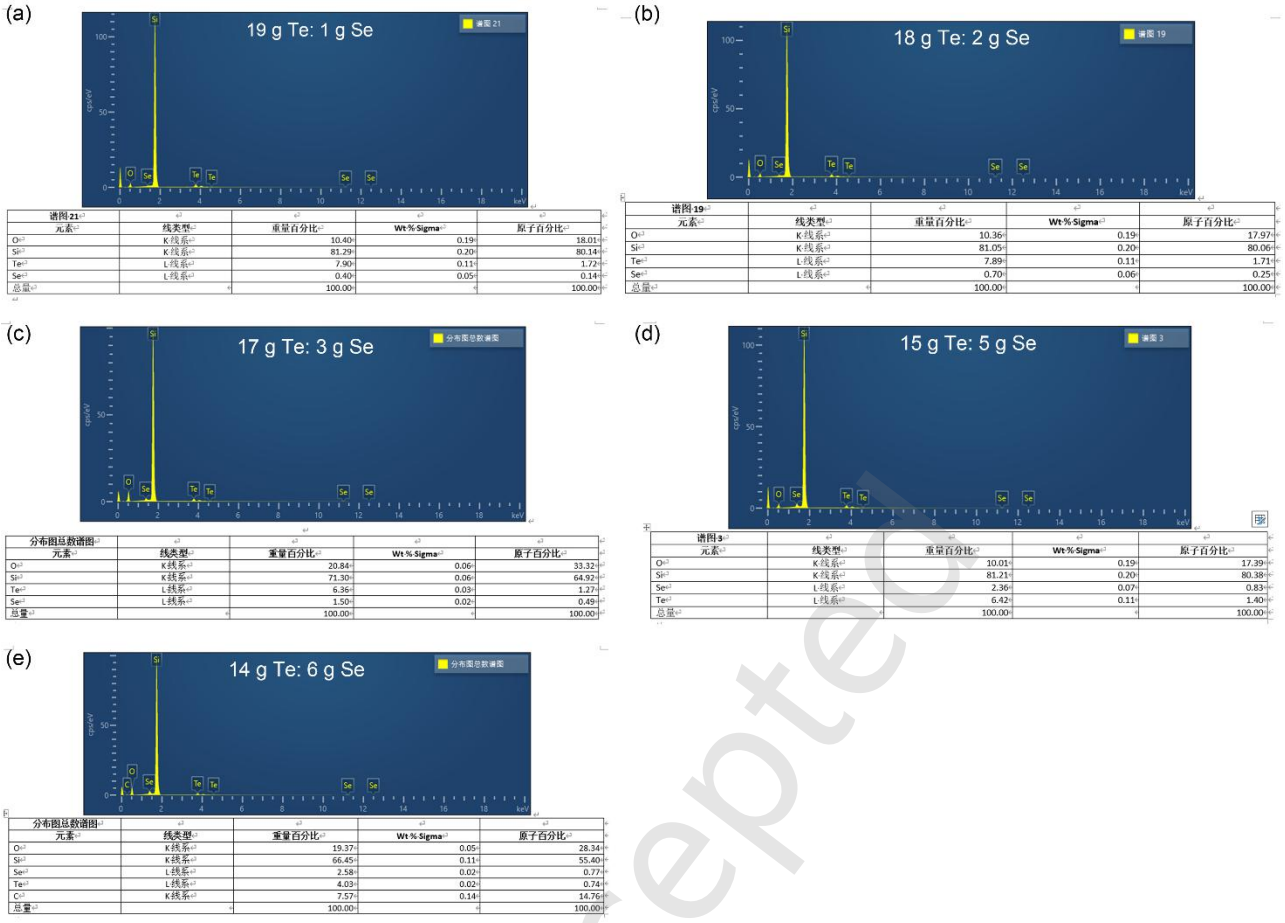


Figure S1 SEM-EDX results of $Te_{1-x}Se_x$ alloy films synthesized with various Te: Se precursor mass ratios of 19:1, 18:2, 17:3, 15:5, and 14:6 g. The calculated Se fractions ([Se]/[Se]+[Te]) are approximately 0.07, 0.13, 0.28, 0.37, and 0.50, respectively.

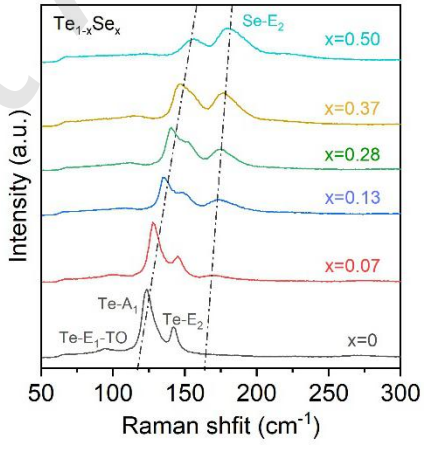


Figure S2 Raman spectra of $Te_{1-x}Se_x$ alloy with increasing Se content from x=0 to 0.5.

Just Accepted

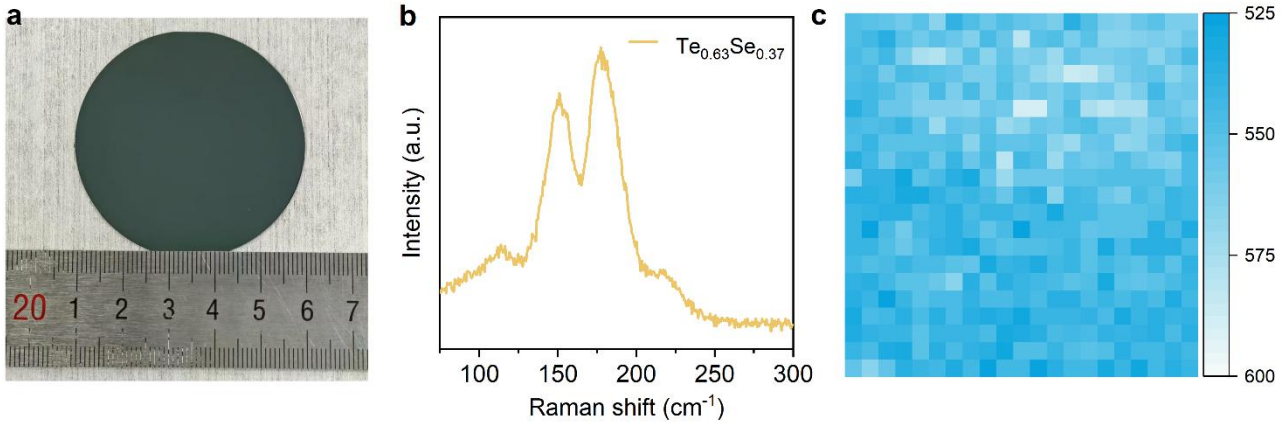


Figure S3 (a) Optical photograph of a 2- inch $Te_{0.63}Se_{0.37}$ film. (b) Typical Raman spectrum of the $Te_{0.63}Se_{0.37}$. (c) Raman mapping spectra of $Te_{0.63}Se_{0.37}$ film deposited on a 2-inch SiO_2/Si substrate, collected from 100 randomly selected locations across the wafer.

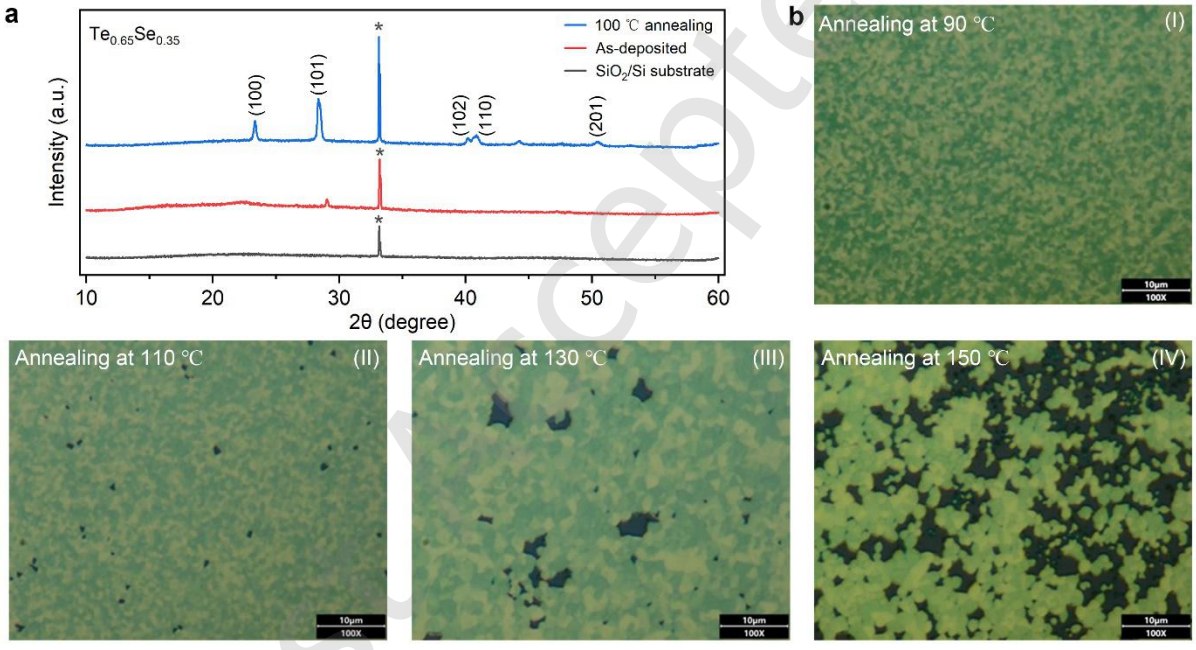


Figure S4 (a) X-ray diffraction patterns of as-deposited and annealed $Te_{0.63}Se_{0.37}$ films. (b) Polarized optical microscopy images of a thin $Te_{0.63}Se_{0.37}$ film (~20 nm) annealed at (I) 90 ℃, (II) 110 ℃, (III) 130 ℃, and (IV) 150 ℃.

As shown, the film exhibits polycrystalline characteristics even after thermal annealing at a low temperature of 90 ℃. However, pinhole formation initiates at ~110 ℃, and the film becomes completely discontinuous at 150 ℃. Our prior and ongoing studies reveal that higher annealing temperatures (e.g., > 130 ℃) can be safely adopted for thicker $Te_{0.63}Se_{0.37}$ films (e.g., > 80 nm). In addition, our experimental observations indicate that $Te_{1-x}Se_x$ films deposited on Si substrates can generally withstand higher annealing temperatures than those on SiO_2/Si substrates.

Just Accepted

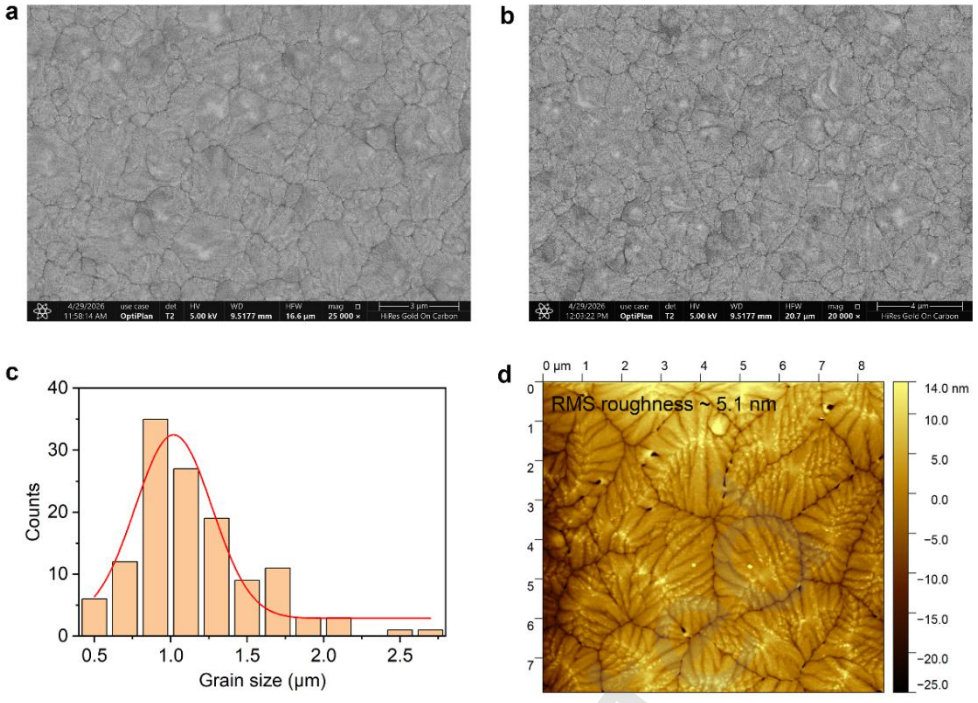


Figure S5 Morphological characterization of the annealed $Te_{0.63}Se_{0.37}$ thin film. (a-b) Top-view scanning electron microscopy (SEM) images. (c) Grain size distribution analysis showing an average lateral grain size of ~1.0 μm. (d) Atomic force microscopy (AFM) topography image of the film, exhibiting a root-mean-square surface roughness of ~5.1 nm (scan area: 8.5 μm × 7.8 μm).

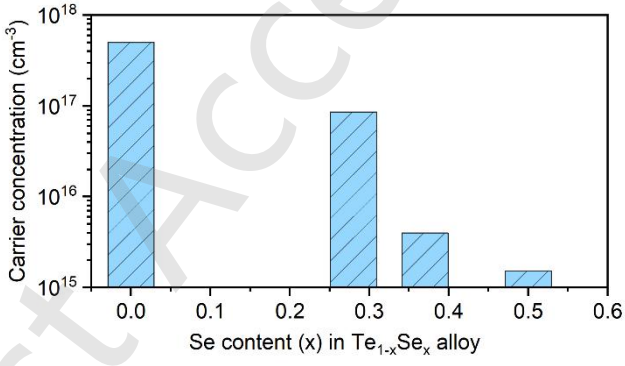


Figure S6 Carrier concentration of $Te_{1-x}Se_x$ alloy films as a function of Se content, determined from Hall effect measurements.

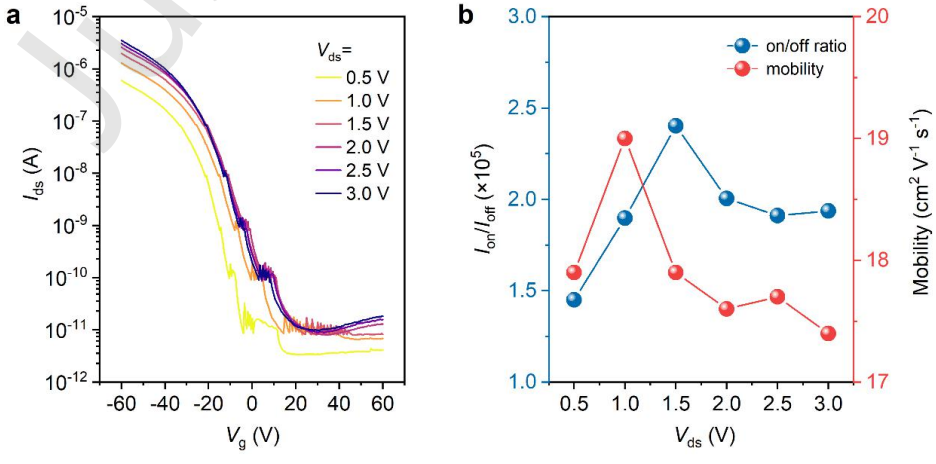


Figure S7 Electrical performance of a 16-nm-thick $Te_{0.63}Se_{0.37}$ TFT. (a) Transfer characteristics. (b) V_{ds}-dependent statistics of the on/off current ratio and effective field-effect mobility.

Just Accepted

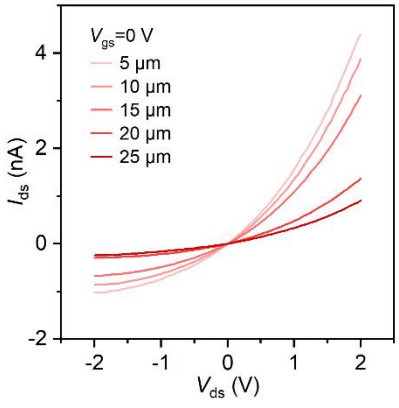


Figure S8 Output characteristics of $Te_{0.63}Se_{0.37}$ TFTs with different channel lengths at V_{gs}=0 V.

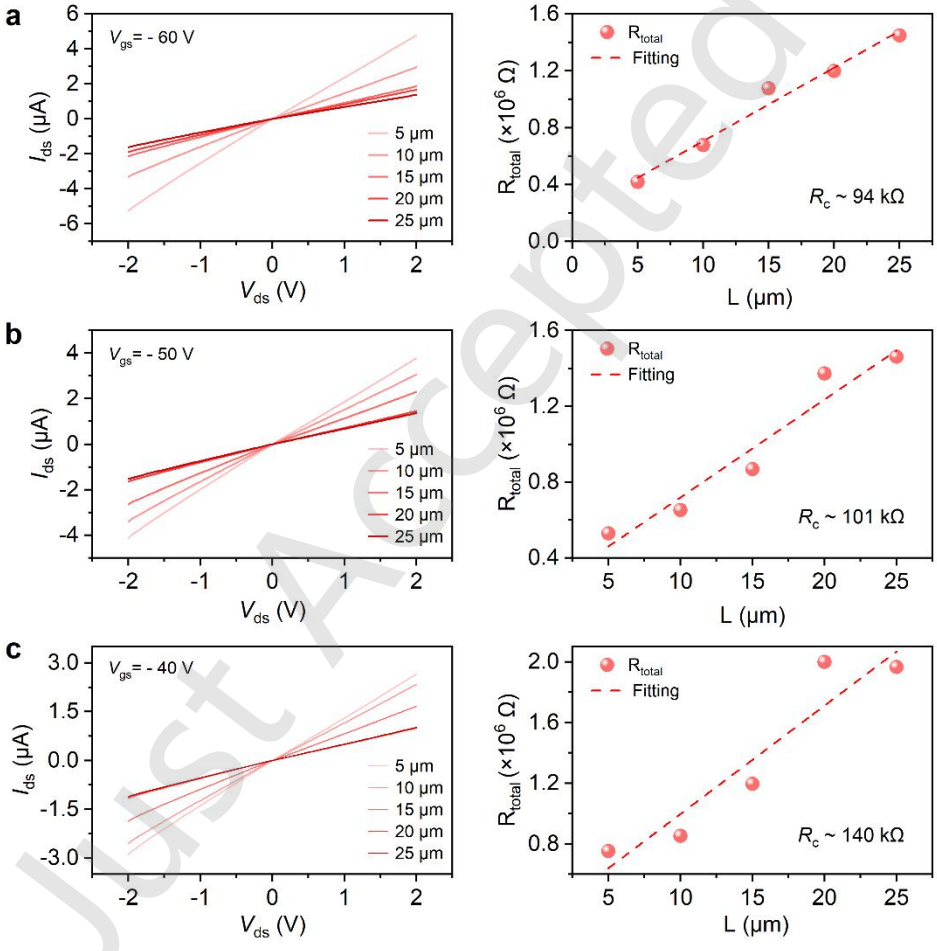


Figure S9 Output characteristics of $Te_{0.63}Se_{0.37}$ FETs (W/L=5/5 μm) with various channel lengths, measured at V_{gs} values of (a) -60 V, (b) -50 V, and -40 V, alongside the corresponding calculated contact resistances (R_c).

Just Accepted

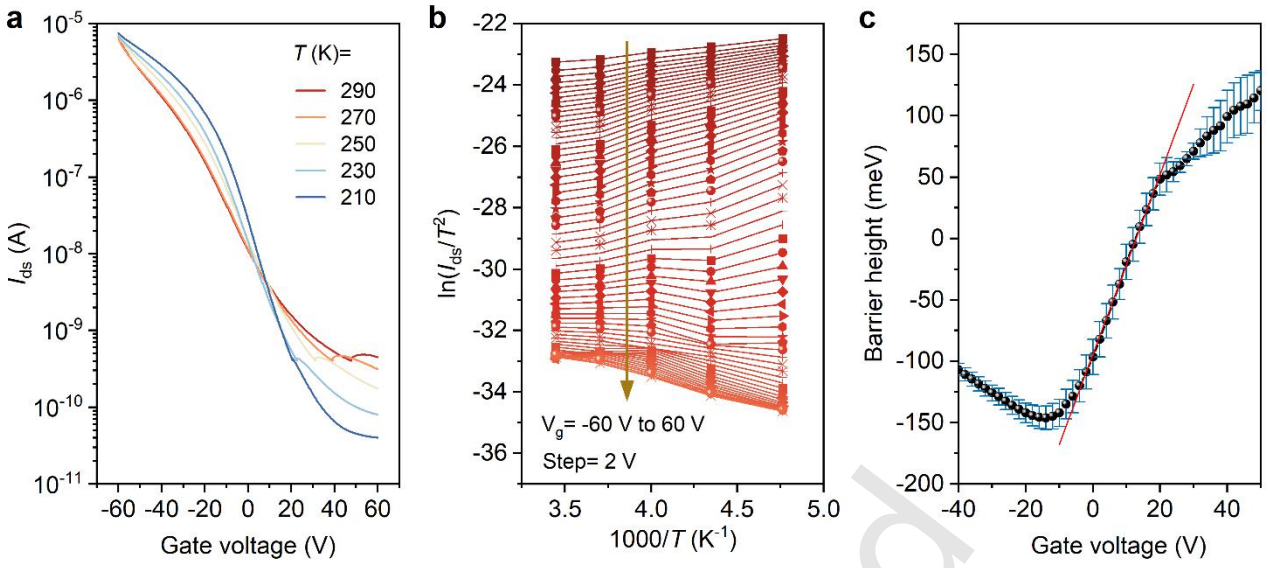


Figure S10 Schottky barrier characterizations of the Au/$Te_{0.63}Se_{0.37}$ contacts. (a) Temperature-dependent transfer curves of the $Te_{0.63}Se_{0.37}$ TFTs. (b) Gate-dependent ln (I_{ds}/T^2) versus 1000/T plots. (c) Gate-dependent barrier heights of the Au/$Te_{0.63}Se_{0.37}$ junctions extracted from (b).

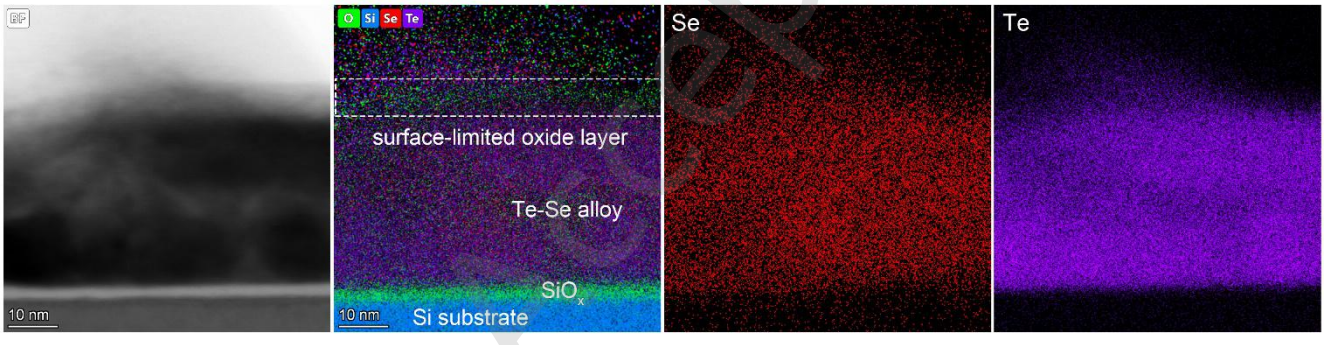


Figure S11 Cross-sectional TEM-EDX characterization results of $Te_{0.63}Se_{0.37}$ film.

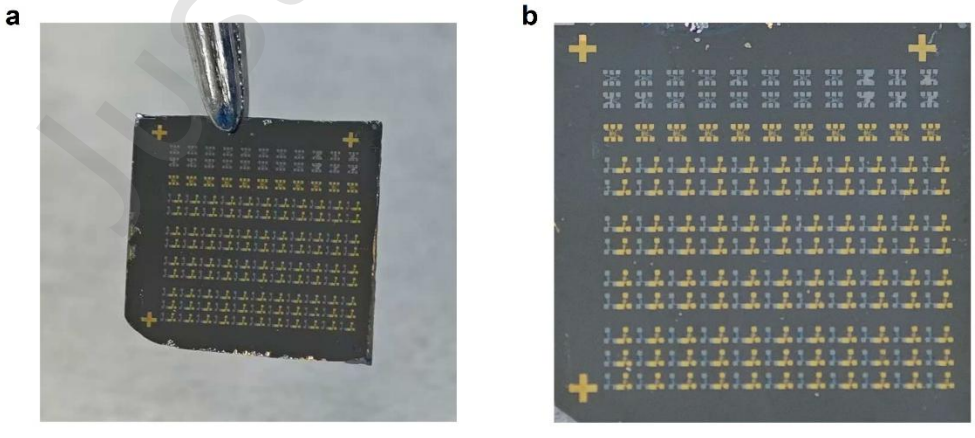


Figure S12 CMOS inverter array fabricated with p-$Te_{0.63}Se_{0.37}$ and n-IGZO TFTs on centimeter-scale p^{++}-Si substrate.

Table S1. Comparison of reported Te and $Te_{1-x}Se_x$-based inverters.

Just Accepted

Material (p-type)	Material (n-type)	V_{DD}（V）	Gain	P_{static}（nW）	Reference
Te-TeO_x	In_2O_3	10	8.5	-	[1]
nc-Te	IGZO	10	49.04	95.87	[2]
Te NW	-	2	70	-	[3]
Te	Bi_2S_3	10	200	-	[4]
Te	IGZO	7	16.7	-	[5]
$Se_{0.5}Te_{0.5}$	InZnSnO	5	12	17	[6]
Se-alloyed-Te-TeO_x	In_2O_3	20	1300	-	[7]
Te-TeO_x	-	7	130	-	[8]
$Te_{0.65}Se_{0.35}$	**IGZO**	**3**	**28**	**0.42**	**This work**

References

[1] Zhang, Y. X.; Wang, J. W.; Xie, P. S.; Meng, Y.; Shao, H.; Jin, C. X.; Gao, B. X.; Shen, Y.; Quan, Q.; Li, Y. Z.; Wang, W. J.; Li, D. J.; Wu, Z. H.; Li, B. W.; Yip, S.; Sun, J.; Ho, J. C. Molecular reconfiguration of disordered tellurium oxide transistors with biomimetic spectral selectivity. *Adv. Mater*. **2024**, *36*, 2412210.

[2] Kim, G. H.; Kang, S. H.; Lee, J. M.; Son, M.; Lee, J.; Lee, H.; Chung, I.; Kim, J.; Kim, Y. H.; Ahn, K.; Park, S. K.; Kim, M. G. Room temperature-grown highly oriented p-type nanocrystalline tellurium thin-films transistors for large-scale CMOS circuits. *Appl. Surf. Sci.* **2023**, *636*, 157801.

[3] Zhao, Y. T.; Zhao, S. C.; Pang, X. X.; Zhang, A. N.; Li, C. N.; Lin, Y. X.; Du, X. M.; Cui, L.; Yang, Z. H.; Hao, T. L.; Wang, C. P.; Yin, J.; Xie, W.; Zhu, J. Biomimetic wafer-scale alignment of tellurium nanowires for high-mobility flexible and stretchable electronics. *Sci. Adv.* **2024**, *10*, eadm9322.

[4] Liu, A.; Zhu, H.; Zou, T.; Reo, Y.; Ryu, G. S.; Noh, Y. Y. Evaporated nanometer chalcogenide films for scalable high-performance complementary electronics. *Nat. Commun.* **2022**, *13*, 6372.

[5] Im, H.; Oh, J. O.; Lee, Y.; Jung, E. K.; Kim, E.; Lee, J.; Kim, J.; Naqi, M.; Kim, Y. S.; Kim, S. Heterogeneous integration of complementary field-effect transistors for high-performance Micro LED displays. *Adv. Mater.* **2025**, *37*, 2408034.

[6] Choi, K.; Nam, S.; Kim, Y. H.; Oh, H.; Kim, I.; Lee, K.; Cho, S. H. Promotion of processability in a p-type thin-film transistor using a Se-Te alloying channel layer. *ACS Appl. Mater. Interfaces* **2024**, *16*, 23459-23466.

[7] Liu, A.; Kim, Y. S.; Kim, M. G.; Reo, Y.; Zou, T.; Choi, T.; Bai, S.; Zhu, H.; Noh, Y. Y. Selenium-alloyed tellurium oxide for amorphous p-channel transistors. *Nature* **2024**, *629*, 798-802.

[8] He, M. F.; Choi, H.; Le, Z. K.; Yang, X. M.; Huang, Y. L.; Reo, Y. J.; Bai, S.; Wang, M. Y.; Zhu, H. H.; Noh, Y. Y.; Liu, A. In-situ p-doping of nanometer tellurium-based oxide for room-temperature CMOS circuits. *Adv. Mater.* **2026**, *38*, e72813.

Just Accepted