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Research Article

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Abstract

Oscillator-inspired neural computing offers a promising route toward energy-efficient information processing, yet its practical implementation is constrained by the lack of compact hardware platforms capable of generating programmable temporal signals. Here, we present a two-dimensional MoS_2/hBN/few-layer graphene floating-gate transistor as a programmable optoelectronic waveform generator. The temporal waveforms emerge from the dynamic competition between gate-induced charge injection and ultraviolet-assisted charge erasure in the floating gate, which drives periodic modulation of the channel conductance. The output frequency can be adjusted from 1 Hz to 10 kHz, while the waveform profile is regulated through gate-voltage programming, illumination intensity, and drain bias. Two coupled devices further demonstrate externally programmable in-phase and anti-phase temporal signal generation, and the experimentally measured dynamics are incorporated into numerical simulations of associative memory recall and graph-coloring tasks. By enabling programmable temporal signal generation in floating-gate transistors, this work establishes a compact hardware building block for oscillator-inspired neuromorphic computing and multifunctional temporal information processing.

Keywords: optoelectronics, floating-gate transistor, two-dimensional semiconductor, neuromorphic computing

1. Introduction

Oscillator-inspired computing has emerged as a promising framework for neuromorphic information processing, in which information is encoded and manipulated through the collective temporal dynamics of nonlinear oscillatory elements[1-3]. By exploiting phase evolution, synchronization, and attractor dynamics, oscillator-based systems have been explored for optimization, pattern recognition, associative memory, and constraint-satisfaction tasks[4-7]. Compared with conventional digital architectures based on sequential Boolean operations, such approaches offer potential advantages in energy efficiency, parallelism, and fault tolerance[8,9]. Realizing these opportunities, however, requires compact and scalable hardware platforms capable of generating programmable temporal dynamics[10,11].

Conventional oscillatory hardware, such as ring oscillators, relaxation oscillators, and phase-transition oscillators, generally relies on dedicated nonlinear elements or feedback circuits to generate periodic dynamics[12-15]. Although these approaches have demonstrated impressive computational capabilities, the resulting hardware complexity and limited programmability remain significant challenges for scalable neuromorphic systems[16,17]. An attractive alternative is to exploit dynamic internal state variables whose continuous evolution directly encodes temporal information, thereby enabling programmable temporal signal generation within compact device platforms[18-20].

Two-dimensional floating-gate transistors provide a unique platform in which the floating-gate charge continuously determines the channel conductance through electrostatic coupling[21-24]. While previous studies have primarily exploited this charge as a nonvolatile memory state[25-27], its dynamic evolution under nonequilibrium electrical and optical excitation remains largely unexplored. When continuously driven out of equilibrium, floating-gate charge can function as a programmable temporal-state variable, enabling dynamic signal generation beyond conventional information storage and offering a compact physical basis for oscillator-inspired neuromorphic computing.

Here, we demonstrate a MoS_2/hBN/few-layer graphene (FLG) floating-gate transistor as a programmable optoelectronic oscillatory element capable of generating tunable temporal signals. Under the combined action of electrical programming and ultraviolet-assisted charge erasure, the floating-gate charge undergoes continuous dynamic evolution, giving rise to periodic conductance modulation and oscillatory output waveforms. The temporal characteristics of the waveform, including frequency, amplitude, baseline, and profile, can be

systematically programmed through electrical and optical control. We further demonstrate phase-programmed operation in two-device circuits and evaluate associative memory and graph-coloring tasks through device-informed numerical simulations. These results establish floating-gate charge dynamics as a programmable temporal-state variable for oscillator-inspired neuromorphic computing.

2. Results and Discussion

I. Floating-Gate Charge Storage and Optical Erasure

The floating-gate transistor was fabricated using a dry transfer technique based on two-dimensional materials (see Methods). Few-layer MoS_2 served as the semiconducting channel[28-31], few-layer graphene (FLG) was employed as the floating gate (FG)[32-35], and few-layer hexagonal boron nitride (hBN) functioned as the dielectric layer[36-40]. The resulting heterostructure was assembled on a silicon substrate with a 285 nm SiO_2 layer, which also acted as the control gate of the floating-gate transistor. A schematic illustration of the device structure is presented in **Figure 1a**. The optical microscopy image and atomic force microscopy (AFM) characterization of the device are provided in Figure S1, Supporting Information. The thicknesses of the MoS_2, hBN and FLG layers are approximately 4 nm, 12 nm, and 10 nm, respectively.

The conductance state of the MoS_2 channel can be controlled by injecting carriers into or removing stored carriers from the FG layer by applying backgate voltage (V_{bg}) on the silicon substrate. As shown in **Figure 1b**, the device exhibits a low-resistance-state (LRS) while applying positive V_{bg}, and it recovers to the high-resistance-state (HRS) after the positive V_{bg} pulse[41]. Conversely, the device switches to HRS under a negative V_{bg}, and reverts to LRS once the negative V_{bg} pulse is removed. The current ratio between the LRS and HRS reaches as high as 10^7 under bias voltage (V_{ds}) of 0.1 V. The transfer characteristics under varying V_{bg} sweep ranges and the retention performance demonstrating stable HRS and LRS states over 10,000 s are provided in Figure S2, Supporting Information. Simultaneously, the electrical potential of the FG layer (V_{fg}), a key factor in understanding the resistance switching behavior, was monitored via the FG electrode under a zero-current condition, thereby preventing charge loss from the FG to the probe during the measurement[42,43]. The V_{fg} showed clear modulation in response to V_{bg} pulses due to capacitance coupling, switching between +8 V and -5 V, which correspond to the LRS and HRS of the MoS_2 channel, respectively.

The underlying mechanism of this resistance regulation is illustrated in the band diagrams in **Figure 1c**. When a V_{bg} of +12 V is applied to the silicon substrate, V_{fg} rises to +8

V through capacitive coupling, driving the MoS_2 channel into LRS. During the pulse, the electric field across the hBN barrier enables electron to be injected into and stored in the floating gate. After removal of the positive V_{bg} pulse, the stored electrons remain in FG layer, resulting in the negative V_{fg} of -5 V. Consequently, the MoS_2 channel switches to the HRS. This switching process can be repeated by applying subsequent positive V_{bg} pulse. In contrast, when a V_{bg} of -12 V is applied, V_{fg} decreases to approximately -5 V through capacitance coupling, driving the channel into the HRS. During the pulse, holes are injected into and stored in the floating gate. After removal of the negative V_{bg} pulse, the stored holes result in a positive V_{fg} of +8 V, returning the MoS_2 channel to the LRS. The direct modulation of V_{fg} as a function of V_{bg} has been demonstrated in Figure S3, Supporting Information.

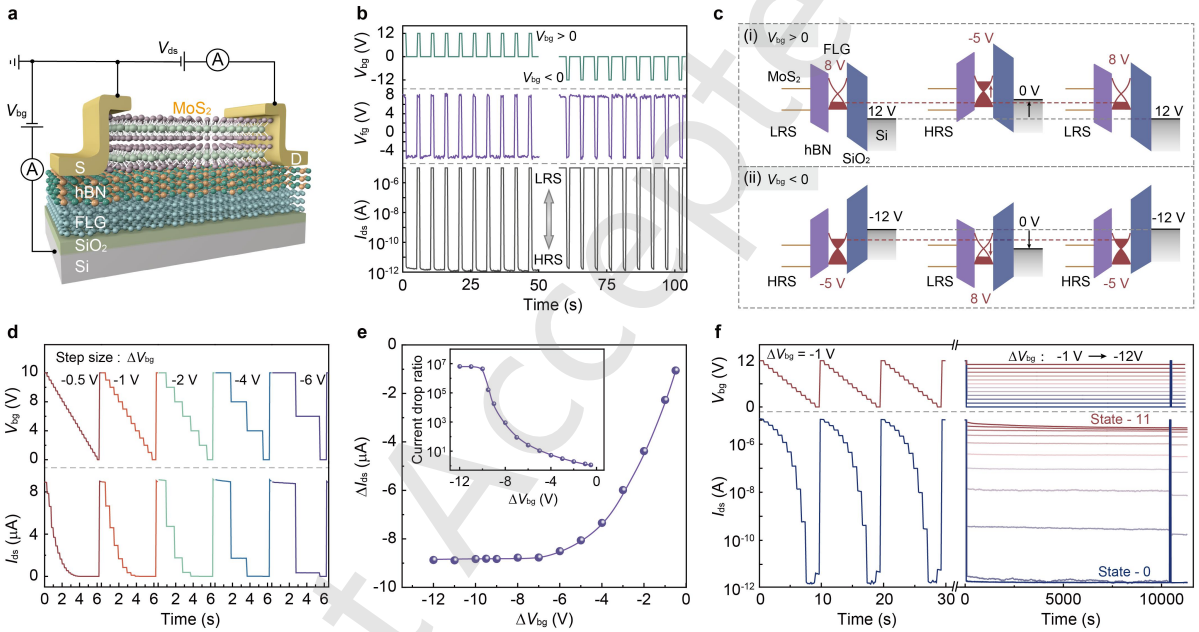

Figure 1. Gate-voltage modulation of the MoS_2/hBN/FLG floating-gate transistor. (a) Schematic structure of the floating-gate transistor based on MoS_2/hBN/FLG heterostructure fabricated on a Si/SiO_2 substrate. (b) Reversible switching of channel resistance and FG layer potential between the high-resistance-state (HRS) and low-resistance-state (LRS) using backgate voltage (V_{bg}) pulses with a duration of 1 s. (c) Band diagram evolution of the heterostructure under (i) positive and (ii) negative V_{bg}, showing dynamical change of the band diagram. (d) Stepwise modulation of resistance by decreasing V_{bg} with different step sizes of -0.5 V, -1 V, -2 V, -4 V, and -6 V. Channel current (I_{ds}) was measured at V_{ds} = 0.1 V. (e) Relationship between the variation of I_{ds} and the applied V_{bg}. The inset shows the current-reduction ratio after each V_{bg} step. (f) Multilevel conductance modulation via stepwise V_{bg} reduction with a fixed step size of -1 V, along with the retention of distinct current states as the V_{bg} decreased from 12 V to 0 V.

These results show that capacitance coupling between the control backgate and FG layer

plays a critical role in the resistance regulation of the MoS_2 channel[42,44]. This suggests that more precise resistance control can be achieved by controlling the variation of the V_{bg}. As demonstrated in **Figure 1d**, a stepwise decrease of V_{bg} enables gradual modulation of I_{ds}. The resistance switching occurs at the falling edge of the V_{bg} pulse, when the capacitive-coupling contribution vanishes and the stored charge state determines the channel conductance. By decreasing the V_{bg} from +10 V to 0 V using step sizes of -0.5 V, -1 V, -2 V, -4 V and -6 V, distinct current plateaus are observed, corresponding to the intermediate resistance states. Further analysis shows that the variation in I_{ds} becomes more pronounced as the amplitude of the V_{bg} step increases, as shown in **Figure 1e**. The drop ratio of I_{ds} increases from 1 to 10^7 when the V_{bg} step size (ΔV_{bg}) increases from -0.5 V to -10 V, demonstrating a wide dynamic range in the tunable channel resistance. Moreover, the resistance state modulation via the voltage sweeping matches well with the transfer curve of the device (Figure S4, Supporting Information), confirming the reproducibility of the resistance modulation. More importantly, the intermediate current states exhibit long-term stability. As shown in **Figure 1f**, when V_{bg} is gradually decreased from 12 V to 0 V with a step size of -1 V, a total of 12 distinct resistance states are established. Each state remains stable over a monitoring period of 10,000 s, showing negligible variation in the I_{ds}, thereby demonstrating excellent retention capability of the device.

UV illumination provides a second, polarity-dependent pathway for controlling the FG charge. The optical modulation originates from photon-assisted transfer of stored carriers in the FLG as previously reported[25,26]. After positive electrical programming, electrons stored in the FLG establish a negative V_{fg} and deplete the n-type MoS_2 channel. When photons with sufficient photon energy are absorbed through the FLG layer, the stored electrons can overcome the effective FLG/hBN interface barrier and transfer across hBN, driving V_{fg} toward 0 V (**Figure 2a**), the resulting capacitive coupling increases the electron density and conductance of MoS_2, giving positive photoresponse PPR. The PPR of the device under 365 nm and 254 nm are illustrated in **Figure 2b**. Conversely, negative electrical programming stores holes in the FLG and establishes a positive V_{fg}. UV-assisted hole escape lowers V_{fg} toward 0 V (**Figure 2c**), and reduces the MoS_2 conductance, producing the negative photoresponse (NPR). The NPR of the device under 365 nm and 254 nm are illustrated in **Figure 2d**. Time-resolved V_{fg} measurements further confirm that the conductivity change is accompanied by the V_{fg} variation under UV illumination[25]. The previous tunneling measurements on the same heterostructure yielded electron and hole barrier heights of

approximately 2.8 and 3.3 eV, corresponding to PPR and NPR cutoff wavelengths of approximately 440 and 375 nm, respectively. Therefore, other wavelengths within these barrier-defined response ranges can also drive optical erasure.

The intensity-dependent optical response further provides a kinetic control parameter for waveform generation. As shown in **Figure 2e**, the time required for the channel current to reach saturation decreases with increasing intensity of the 254 nm incident light. This is because stronger illumination enhances the removal rate of stored electrons in the FG layer, thereby accelerating the change in I_{ds}. In other words, under a fixed illumination duration, distinct resistance states can be achieved by tuning the light intensity, as indicated by the vertical dashed line at t = 60 s in **Figure 2e**. Furthermore, we evaluated the retention characteristics of these resistance states. The results show that, like the excellent stability observed under electrical modulation, the optically induced resistance states also exhibit outstanding retention behavior. During a prolonged test period of up to 10^4 s, no noticeable degradation in resistance states was observed, confirming their robust stability (**Figure 2f**).

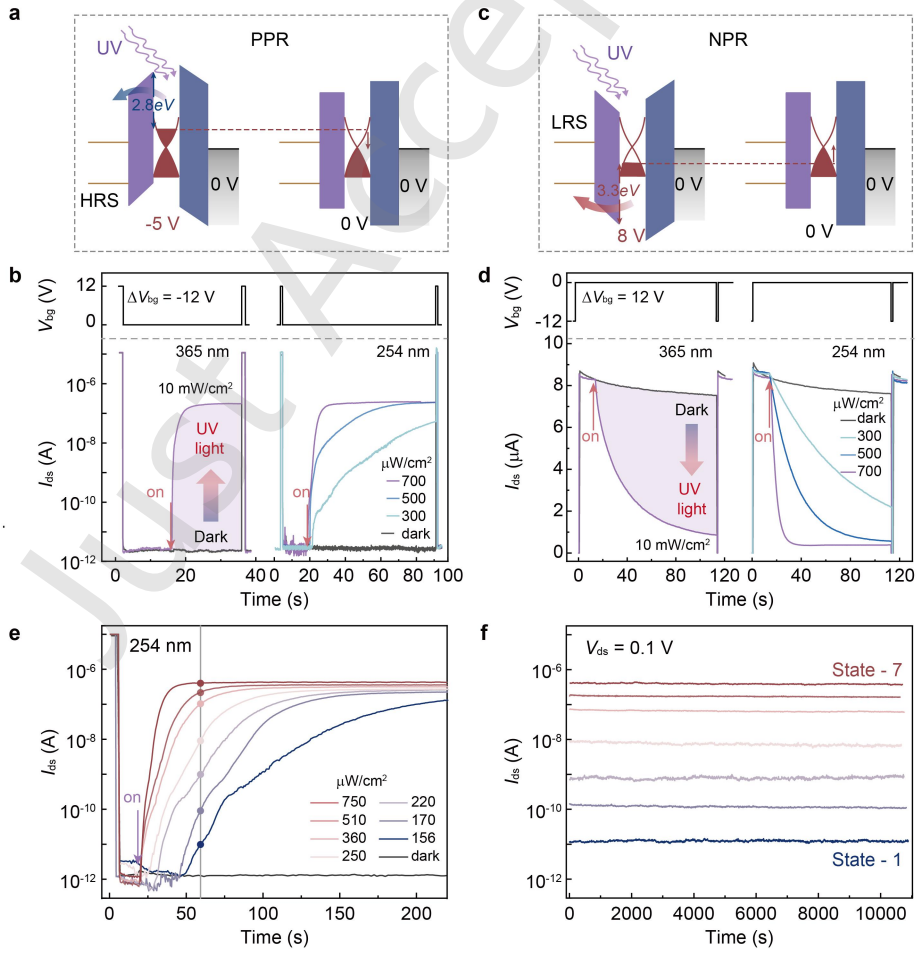

Figure 2. Ultraviolet modulation of charge states in MoS_2/hBN/FLG floating-gate transistor. (a) Schematic band diagram of the device under negative V_{fg}: UV illumination

promotes photoexcited electrons to escape from the FG layer, restoring V_{fg} to 0 V. (b) Positive photoresponse (PPR) to 365 nm and 254 nm UV light, when the device is in HRS; +12 V V_{bg} pulse is used for reset. (c) Schematic band diagram of the device under positive V_{fg}: photoexcited holes escape from the FG layer under UV light, resetting V_{fg} to 0 V. (d) Negative photoresponse (NPR) to 365 nm and 254 nm UV light, when the device is in LRS. -12 V V_{bg} pulse is used to reset the device to LRS after NPR. (e) Time-resolved PPR under 254 nm UV light with varying intensities, illuminations begin at t = 20 s. (f) Long-term retention test of the resistance states set by 254 nm UV light with different intensities.

II. Oscillatory Waveform Generation through Combined Gate Programming and UV Illumination

The preceding results demonstrate that distinct resistance states in the floating-gate transistor can be regulated through both gate-controlled floating-gate charge modulation and UV-induced charge erasure. When stepwise gate-voltage modulation is applied simultaneously with continuous UV illumination, the competition between these two processes gives rise to dynamic conductance evolution, resulting in periodic resistance oscillations. This behavior converts a programmed gate-voltage sequence into a periodic optoelectronic output waveform. **Figure 3a** illustrates the measurement circuit consisting of the floating-gate transistor and a load resistor. Under a time-dependent gate bias and continuous UV illumination, the channel conductance is periodically modulated, producing oscillatory current and load-voltage outputs.

In this configuration, we explored two distinct schemes for realizing resistance oscillation through optoelectronic coupling. In the first case, a stepwise decreasing V_{bg} is combined with UV-induced positive photoresponse, as illustrated in **Figure 3b**. As previously discussed, electrons are accumulated in the floating gate under the higher V_{bg} states. When V_{bg} is decreased stepwise, the contribution of capacitive coupling is progressively reduced, allowing the stored electrons in the floating gate to increasingly dominate the channel conductance. As a result, V_{fg} decreases and the channel current Ids is suppressed. During the plateau regions between voltage steps, continuous UV illumination gradually removes the stored electrons from the FG layer, increasing V_{fg} and restoring Ids through the PPR process. The repeated alternation between gate-induced conductance suppression and UV-assisted current recovery generates periodic oscillations in Ids, as shown in **Figure 3b**. This behavior is further confirmed by the corresponding voltage oscillations measured across the series load resistor. Notably, the output voltage amplitude is determined by the load resistance and can therefore be tuned by employing different load resistors.

In the second case (**Figure 3c**), a stepwise increasing V_{bg} is combined with UV-induced NPR. The increase in V_{bg} drives the floating-gate state toward hole accumulation, resulting in an increase in V_{fg}, and a corresponding change in channel conductance. During the subsequent voltage-holding periods, continuous UV illumination gradually removes the stored holes from the floating gate, reducing V_{fg} and decreasing the channel current through the NPR process. The repeated alternation between gate-driven conductance modulation and UV-assisted charge erasure results in periodic oscillations of the channel current and output voltage. In both operation modes, the oscillation period is determined by the externally programmed gate-step interval, whereas the waveform evolution within each cycle is governed by the competition between gate-controlled floating-gate charge modulation and UV-assisted charge erasure.

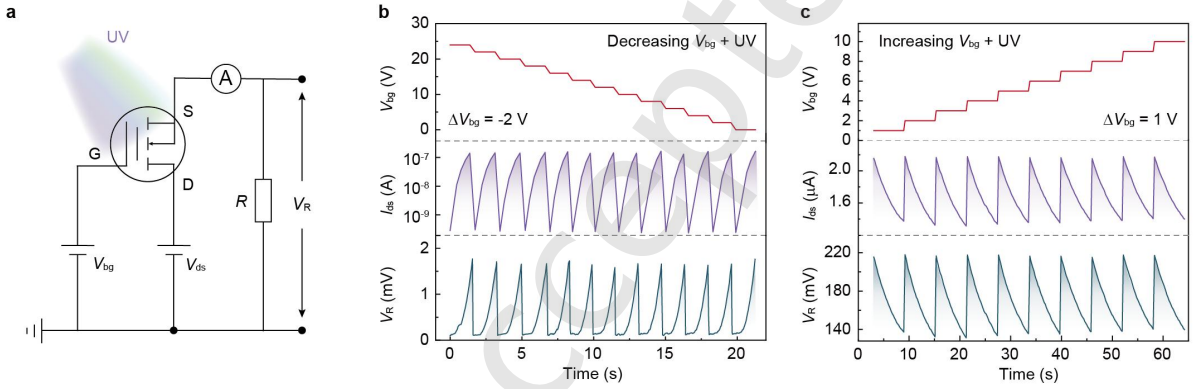

Figure 3. Gate-paced optoelectronic oscillation controlled by coupled gate-driven charge modulation and optical erasure. (a) Schematic of the oscillation circuit based on the floating-gate transistor and load resistor. (b) Oscillation waveforms generated under 254 nm UV illumination by combining a decreasing stepwise V_{bg} with PPR. (c) Oscillation waveforms generated under 254 nm UV illumination by combining an increasing stepwise V_{bg} with NPR. The load resistance was fixed at 10 kΩ for both operating modes.

III. Frequency and Amplitude Programming of Gate-Paced Optoelectronic Waveforms

For neuromorphic hardware, programmable control of frequency, amplitude, and phase is essential for temporal encoding and circuit-level operation. In the present device, the oscillation period is directly programmed by the gate-step interval, enabling straightforward frequency control over several orders of magnitude. The floating-gate transistor defines the waveform shape, recovery or decay kinetics, baseline shift, amplitude, and maximum resolvable operating frequency under a given optical-erasure condition. In **Figure 4**, the applied V_{bg} waveform consists of finite transition and holding periods. During each transition, gate-driven charge modulation produces an abrupt current change. During the holding period,

continuous UV illumination drives floating-gate charge erasure and gives rise to current recovery or decay.

For instance, when the interval was 1 s (**Figure 4a)**, the oscillation period was also 1 s, corresponding to a frequency of 1 Hz. The dominant frequencies were extracted via Fourier transformation analysis of the oscillation waveforms (Figure S5, Supporting Information). Moreover, reducing the voltage step interval increases the oscillation frequency, reaching 100 Hz at 10 ms (Figure S6, Supporting Information) and 1 kHz at 1 ms (**Figure 4b**) under 254 nm UV illumination. Concurrently, the increase in photon energy facilitated more efficient electron removal in PPR, due to the increased quantum efficiency[45], which could enable the oscillation under even higher frequency. As illustrated in **Figure 4c**, under 222 nm illumination, a distinct 10 kHz oscillation frequency is observed even at a voltage interval as short as 0.1 ms. Oscillatory outputs at other frequencies under 222 nm illumination are shown in Figure S7, Supporting Information. These results clearly demonstrate the tunability of the oscillation frequency, demonstrating programmable operation across four orders of magnitude in frequency.

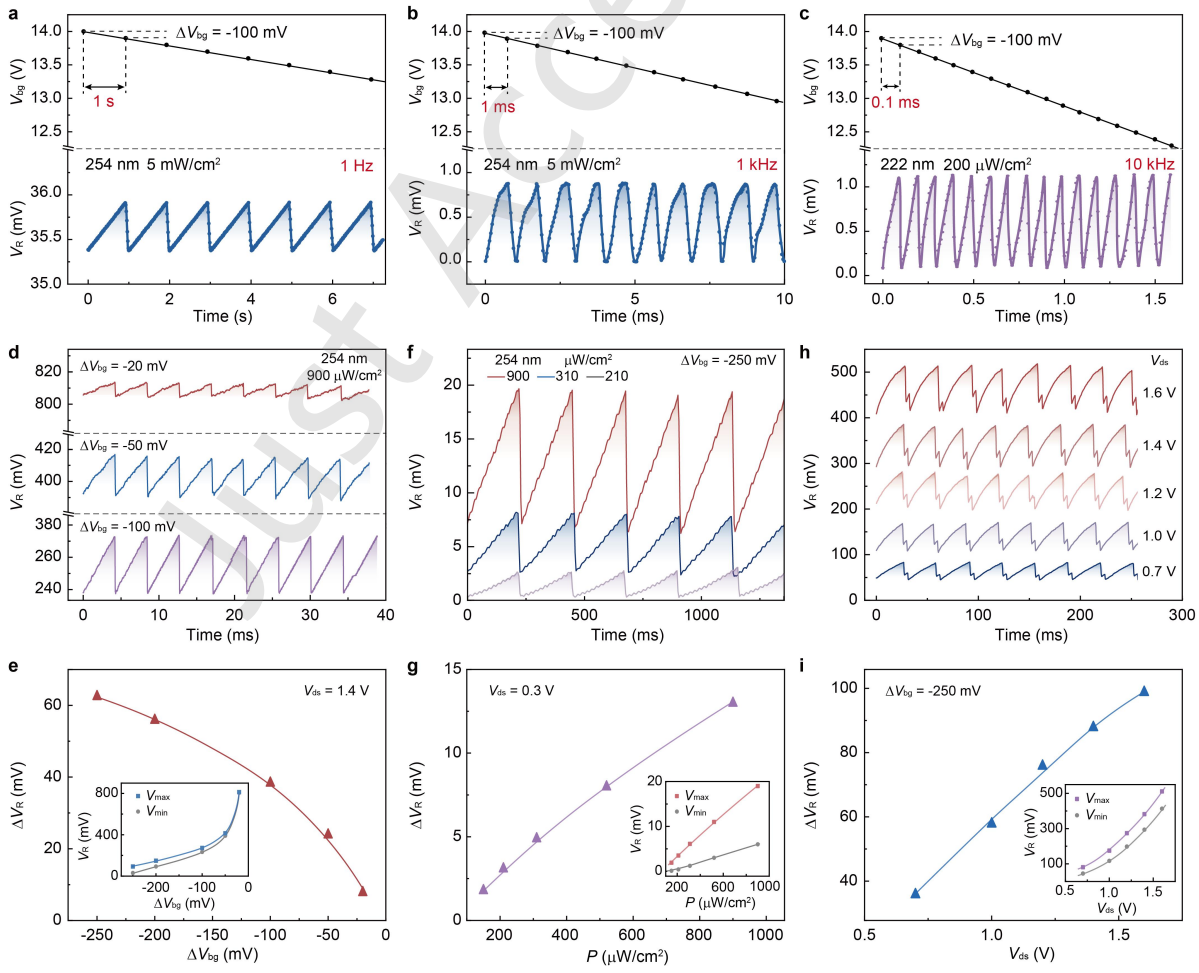

Figure 4. Frequency and amplitude control of gate-paced optoelectronic waveforms. (a)

Output oscillation at 1 Hz, generated using a 1 s interval for the decreasing voltage step combined with PPR under 254 nm UV illumination (5 mW/cm^2). (b) Oscillation at 1 kHz with a 1 ms interval under 254 nm UV illumination (5 mW/cm^2). (c) Oscillation at 10 kHz under 222 nm illumination (200 μW/cm^2) with a 0.1 ms interval. For all waveforms, the voltage step amplitude is -100 mV and V_{ds} is fixed at 0.1 V. (d) Oscillation waveforms as a function of ΔV_{bg}, varied from -20 mV to -100 mV under 254 nm illumination (900 μW/cm^2) at V_{ds} = 1.4 V. (e) Oscillation amplitude (ΔV_R) as a function of ΔV_{bg}, showing an increase from -20 mV to -250 mV. Inset: variation of V_{max} and V_{min} with ΔV_{bg}. (f) Oscillation waveforms under different illumination intensities (P) ranging from 210 μW/cm^2 to 900 μW/cm^2, with ΔV_{bg} = -250 mV and V_{ds} = 0.3 V. (g) Dependence of ΔV_R on P, showing monotonic increase. Inset: variation of V_{max} and V_{min} with P. (h) Oscillation waveforms at different drain biases (V_{ds}) from 0.7 V to 1.6 V under 254 nm UV illumination (20 mW/cm^2). (i) Dependence of ΔV_R on V_{ds}, showing a monotonically increases. Inset: variation of V_{max} and V_{min} with V_{ds}. For all waveforms, the load resistor is 1 MΩ.

Additionally, the amplitude of the oscillation can be modulated by varying the step size of V_{bg}. As illustrated in **Figure 1e**, the variation in I_{ds} is strongly correlated to the magnitude of the V_{bg} step. Within each oscillation cycle, the increment of I_{ds} is governed by UV-induced electron depletion, whereas the decrease is primarily determined by the change in V_{bg}. Consequently, under constant UV illumination, the oscillation amplitude ΔV_R—defined as the difference between maximum (V_{max}) and minimum (V_{min}) output voltage—increases with larger ΔV_{bg}. As shown in **Figure 4d**, the amplitude of the output voltage oscillation becomes more pronounced as ΔV_{bg} increases from -20 mV to -100 mV. Notably, the baseline level of the output voltage also shifts downward with increasing ΔV_{bg}. This shift arises from the need to maintain a dynamic equilibrium between UV-induced charge erasure and voltage-induced charge injection in FG layer, which is essential for sustaining stable oscillatory behavior. The charge injection rate is predominantly affected by the magnitude of ΔV_{bg}, while the charge erasure rate depends on both the illumination condition and the instantaneous V_{fg}. To compensate for the enhanced injection efficiency at larger ΔV_{bg}, the V_{fg} must be reduced to boost the erasure rate under the same illumination condition. As a result, the baseline of output voltage, which is proportional to the I_{ds}, decreases accordingly. **Figure 4e** extracts the variation of ΔV_R with ΔV_{bg}, showing an increasing trend as the ΔV_{bg} increases from -20 mV to -250 mV. Correspondingly, V_{max} and V_{min} exhibit a downward trend, which is presented in the inset of **Figure 4e**.

Moreover, the oscillation amplitude can also be modulated by the intensity of the UV illumination by tuning the charge erasure rate in FG layer. As shown in **Figure 4f**, the oscillation amplitude increases with the light intensity of 254 nm UV illumination, while the

step size of V_{bg} was fixed. The variation of the ΔV_R as a function of the light intensity was summarized in **Figure 4g**, which shows a monotonically increasing trend with the light intensity. The V_{max} and V_{min} of the output voltage under varying light intensities are also depicted in the inset of **Figure 4g**. Furthermore, it is worth noting that stronger illumination not only enhances the oscillation amplitude but also increases the maximum achievable oscillation frequency (Figure S8, Supporting Information). Finally, the oscillation amplitude can also be modulated through the drain bias voltage (V_{ds}). **Figure 4h** shows the output oscillation curves at varying V_{ds}. V_{max}, V_{min} and ΔV_R all increase with the applied V_{ds}, while keeping the ΔV_{bg} and load resistance constant. As summarized in **Figure 4i**, the oscillation amplitude increases from 36 mV to 100 mV, as V_{ds} increases from 0.7 V to 1.6 V. Furthermore, by modulating the duration of the plateau regions between voltage steps, we can enhance the UV-induced charge erasure from the floating gate, thereby prolonging the rising edge of the oscillation waveform and enabling additional control over the waveform shape, as demonstrated in Figure S9, Supporting Information.

IV. Phase-Programmed Circuit Operation and Device-Informed Oscillator-Network Simulations

The programmable oscillatory response of the floating-gate device provides a temporal signal that can be used for phase-coded circuit operation and oscillator-network simulations. As a circuit-level demonstration, two devices were connected in parallel, as schematically shown in **Figure 5a**. The circuit consists of two parallel branches-Device 1 connected through with R_1 and Device 2 connected through with R_2-that share a common load resistor R_3. Independent gate voltage inputs (V_{bg1} and V_{bg2}) are applied to the two devices to externally program their relative phase.

Figure 5b shows the in-phase operating state. When in-phase gate voltage inputs are applied, both V_1 and V_2 exhibit identical oscillation periods of 2 ms with coincident peaks, indicating coincident phase evolution under identical gate-voltage programming. The output signal V_3 oscillates at the same frequency, with an amplitude approximately equal to the sum of the individual contributions, reflecting current summation through R_3. In contrast, **Figure 5c** presents the anti-phase operating state. When out-of-phase gate voltage inputs with a half-period offset are applied, V_1 and V_2 maintain the same oscillation period (2 ms) but exhibit a phase difference of π (1 ms). This phase opposition leads to partial cancellation of the total current through R_3, resulting in an output signal V_3 with a reduced amplitude and an

effective oscillation period of 1 ms. These results demonstrate that the two-device circuit can access distinct phase configurations, including in-phase and anti-phase states, through external modulation. Such controllable phase relationships constitute fundamental building blocks for encoding and processing information in oscillator-based computing architectures.

Building on the experimentally demonstrated oscillatory dynamics, we further evaluated their computational relevance through device-informed numerical simulations, in which a network of coupled oscillators was configured to perform associative memory recall and constraint-satisfaction tasks. In this framework, each oscillator represents a network node, while the coupling matrix encodes the interaction weights between oscillators. The experimentally measured oscillatory waveform was introduced as the temporal template for oscillator nodes, and task dependent network interactions were constructed to guide the evolution of the simulated states. Through this framework, programmable device level oscillations can be connected with attractor formation and phase state organization, enabling representative functions including associative memory recall and graph coloring.

For associative memory, four 12×12 command patterns, including 'Right', 'Left', 'Forward', and 'Stop', were encoded as stored binary phase state patterns in the device informed ONN simulation. Each pixel was mapped to an oscillator state represented by 0 or π phase shifts of the experimentally measured waveform template, and the stored patterns were embedded into a numerical interaction matrix using a Hebbian Hopfield rule. Starting from erased inputs with missing strokes, the simulated dynamics evolved toward lower-energy states and converged to the nearest stored attractor. Consequently, the corrupted patterns were progressively reconstructed and converged to the corresponding complete stored patterns, demonstrating pattern completion from partially erased inputs, as shown in **Figure 5d**.

To further evaluate the computational capability, a graph-coloring task was implemented through device informed numerical simulations. Graph coloring is a representative constraint satisfaction problem in which adjacent nodes are required to have different colors. In the simulated oscillator network, each oscillator represents a graph node, while graph edges are mapped to phase separation constraints between connected oscillators. In this framework, assigning different colors corresponds to grouping oscillators into distinct phase clusters. The graph coloring problem is therefore transformed into a phase-separation process, where the network evolves toward a phase configuration that minimizes the number of violated pairwise constraints. The steady-state solution is obtained through phase clustering, in which oscillators converging to the same phase are assigned the same color. As shown in **Figure 5e**,

the simulated network converges to three distinct phase clusters containing 4, 3, and 2 nodes (highlighted in orange, blue, and green, respectively), corresponding to a valid 3-coloring solution for the graph shown in **Figure 5f**. The requirement that adjacent nodes possess different colors is naturally satisfied through the resulting phase configuration.

These results demonstrate that the programmable oscillatory dynamics of the floating-gate device provide a device-level basis for oscillator-inspired neuromorphic computation. The experimentally measured waveform characteristics can be incorporated into numerical oscillator-network models, establishing a functional connection between programmable device dynamics, phase-state evolution, and computational behavior. The floating-gate architecture enables precise control of oscillatory waveforms through gate-voltage programming and optical modulation, allowing systematic tuning of frequency, amplitude, and waveform shape. Together with its compact single-device implementation, these characteristics highlight the potential of floating-gate optoelectronic oscillators as building blocks for future oscillator-based neuromorphic hardware.

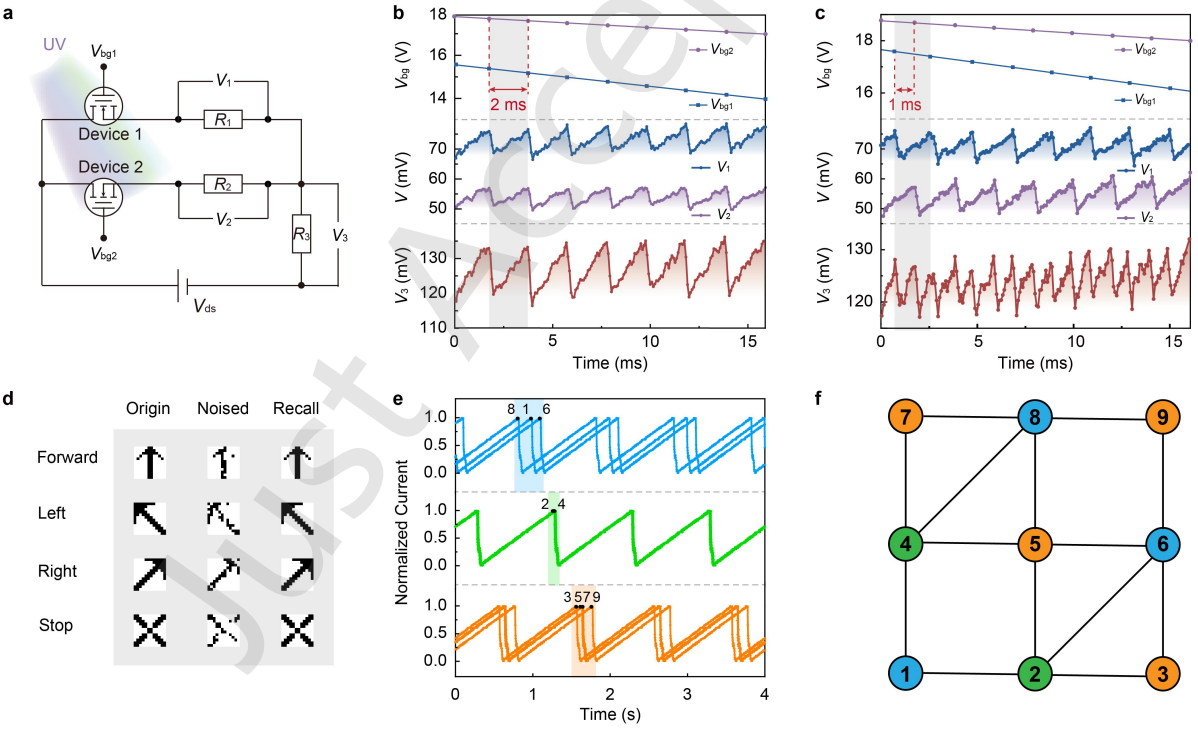

Figure 5. Oscillator networks for associative memory and computation. (a) Circuit schematic of two floating-gate transistors connected in parallel. (b) In-phase operation: in-phase gate voltage inputs (V_{bg1}, V_{bg2}) produce synchronized output oscillations across R_1, R_2, and R_3, all exhibiting identical periods of 2 ms. The output V_3 shows an amplitude approximately equal to the sum of V_1 and V_2, indicating constructive current summation. (c) Anti-phase operation: out-of-phase gate voltage inputs (half-period shift) lead to desynchronized output oscillations. V_1 and V_2 exhibit a phase difference of π (1 ms), resulting in an output V_3 with a reduced amplitude and effective period of 1 ms due to partial current

cancellation. (d) Associative memory simulation using four 12×12 command patterns, 'Right', 'Left', 'Forward', and 'Stop'. When presented with erased inputs containing missing strokes, the simulated network reconstructs the corresponding complete stored patterns. (e) Device-informed graph-coloring simulation. Three distinct phase clusters emerge, comprising 4, 3, and 2 oscillators (highlighted in orange, blue, and green, corresponding to nodes 3, 5, 7, and 9; 8, 1, and 6; and 2 and 4, respectively), corresponding to a valid 3-coloring solution. (f) Topology of the input graph used for the coloring problem. Nodes and edges define the constraint that connected nodes must have different colors.

3. Conclusion

In summary, we have demonstrated a programmable gate-paced optoelectronic waveform generator element based on a two-dimensional MoS_2/hBN/FLG floating-gate memory transistor. Under stepwise gate-voltage programming and continuous UV illumination, the dynamic competition between gate-induced floating-gate charging and photo-assisted charge erasure produces periodic modulation of the channel conductance. The output period is determined by the external gate-step interval, while the amplitude, recovery or decay dynamics, and maximum resolvable frequency are governed by the floating-gate charge dynamics and optical erasure kinetics. The output frequency can be programmed from 1 Hz to 10 kHz, and the amplitude can be tuned by gate-step size, light intensity, and drain bias. Two coupled devices further demonstrate externally programmable in-phase and anti-phase current summation, and experimentally measured device dynamics are incorporated into numerical simulations of associative memory recall and graph-coloring tasks. This work establishes a compact, optically addressable, and electrically programmable hardware platform for oscillator-inspired neuromorphic computing and multifunctional temporal information processing.

Methods

Multilayer 2D materials (few-layer graphene (FLG), hBN, and MoS_2) were mechanically exfoliated from bulk crystals purchased from HQ Graphene and transferred onto silicon substrates coated with 285 nm of SiO_2. The heterostructure was assembled using a dry transfer technique with a polydimethylsiloxane (PDMS) stamp under ambient conditions, maintaining precise temperature control (25 ± 1°C) to minimize flake wrinkling or damage. The assembly sequence involved transferring the FLG flake onto the SiO_2/Si substrate, aligning and stacking the hBN flake atop the FLG, and finally placing the MoS_2 flake onto the hBN/FLG stack to complete the heterostructure.

Cr/Au (10 nm/60 nm) electrodes were patterned via standard electron-beam lithography

(EBL, TESCAN X4), followed by thermal evaporation (JSD 500) and lift-off in acetone to remove excess metal. Electrical characterization employed three dedicated systems: a Keithley 4200A Semiconductor Analyzer to characterize the electrical and optoelectronic switching behavior under different illumination conditions ; a Keysight B2912B Semiconductor Analyzer to probe the influence of gate-voltage step size on conductance states; and an FS-Pro High-Speed Measurement System, coupled with a Tektronix MSO54B oscilloscope, to apply sub-millisecond-level gate-voltage pulses and capture high-frequency output oscillations, enabling analysis of dynamic response and high-speed performance. All measurements were conducted in a vacuum chamber to eliminate interference from ambient moisture and oxygen. For optoelectronic measurements, the UV beam was unfocused and covered the entire heterostructure. The effective area is measured to be 40 μm^2.

Experimentally measured oscillatory waveforms were used as temporal templates for device-informed ONN simulations. In the associative-memory task, four 12 × 12 command patterns were encoded as binary states and stored using a classical Hopfield network model. Specifically, a Hebbian interaction matrix (W) was constructed from the stored patterns, and the network state vector (s), containing the binary states of all pixels, was iteratively updated by the standard Hopfield rule. During recall from erased inputs with missing strokes, the Hopfield energy ($E = -\frac{1}{2}s^{T}Ws$) was monitored to evaluate convergence toward stored attractor states. In the graph-coloring task, a nine-node graph was represented by phase oscillators with graph-dependent coupling. The phase dynamics were numerically evolved using a Kuramoto-type update, and the final phases were decoded into three color groups centered at 0, 2π/3, and 4π/3. The number of conflicting edges, defined as connected nodes assigned to the same color, was used as the cost function, and a zero-conflict final state was regarded as a valid 3-coloring solution.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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