

Selector only memory: Mechanism, devices, industrial demonstrations, and challenges

Si-Bo Wang¹, Nian-Ke Chen¹(✉), Bai-Qian Wang¹, Huan-Ran Ding¹, Yu-Ting Huang¹(✉), Jia Sun¹, Yao-Jie Wang¹, Wen-Xiong Song², Ming Xu³, Xian-Bin Li¹(✉)

¹ State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, College of Integrated Circuits, Jilin University, Changchun 130012, China

² State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China

³ School of Integrated Circuits, Huazhong University of Science and Technology, Wuhan 430074, China

Nano Res., **Just Accepted Manuscript** • <https://doi.org/10.26599/NR.2026.94909157>

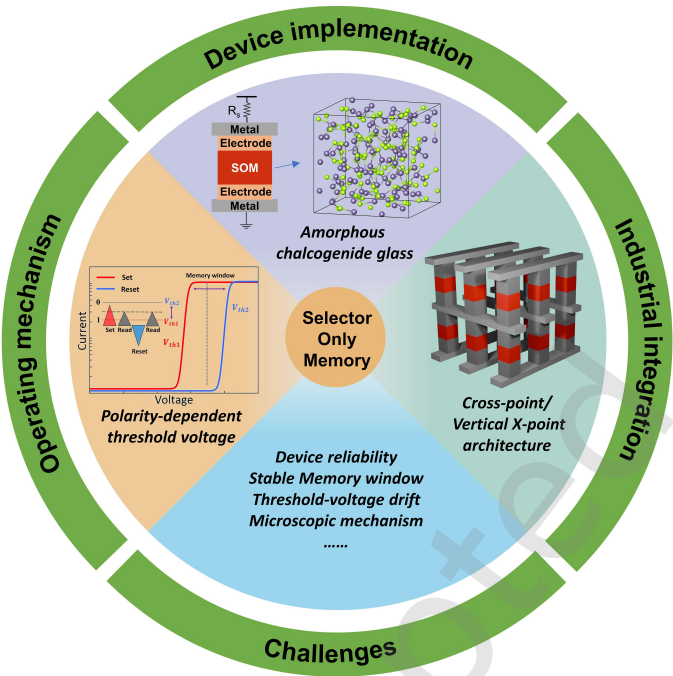
<https://www.sciopen.com/journal/1998-0124> on Aug. 31, 2026

© The Authors(s)

Just Accepted

This is a “Just Accepted” manuscript, which has been examined by the peer-review process and has been accepted for publication. A “Just Accepted” manuscript is published online shortly after its acceptance, which is prior to technical editing and formatting and author proofing. Tsinghua University Press (TUP) provides “Just Accepted” as an optional and free service which allows authors to make their results available to the research community as soon as possible after acceptance. After a manuscript has been technically edited and formatted, and the page proofs have been corrected, it will be removed from the “Just Accepted” web site and published officially with volume and article number (e.g., *Nano Research*, **2025**, *18*, 94906990). Please note that technical editing may introduce minor changes to the manuscript text and/or graphics which may affect the content, and all legal disclaimers that apply to the journal pertain. In no event shall TUP be held responsible for errors or consequences arising from the use of any information contained in these “Just Accepted” manuscripts. To cite this manuscript please use its Digital Object Identifier (DOI®), which is identical for all formats of publication.

TABLE OF CONTENTS (TOC)



Selector only memory stores information through polarity-dependent threshold voltage states in amorphous chalcogenide glass, enabling a compact 1S0R architecture for cross-point or vertical X-point memory. This review summarizes its mechanisms, device and industrial integration progress, and key challenges.

Selector only memory: Mechanism, devices, industrial demonstrations, and challenges

Si-Bo Wang¹, Nian-Ke Chen¹, Bai-Qian Wang¹, Huan-Ran Ding¹, Yu-Ting Huang¹, Jia Sun¹, Yao-Jie Wang¹, Wen-Xiong

Song², Ming Xu³, and Xian-Bin Li¹

¹ State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, College of Integrated Circuits, Jilin University, Changchun 130012, China

² State Key Laboratory of Materials for Integrated Circuits, Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China

³School of Integrated Circuits, Huazhong University of Science and Technology, Wuhan 430074, China

Received: 8 August 2026; Revised: 28 August 2026; Accepted: 31 August 2026

✉ Address correspondence to Nian-Ke Chen, chennianke@jlu.edu.cn; Yu-Ting Huang, huangyuting@jlu.edu.cn; Xian-Bin Li, lixianbin@jlu.edu.cn

🔗 Cite this article: Nano Research, 2026, 19, 94909157 <https://doi.org/10.26599/NR.2026.94909157>

ABSTRACT: Selector-only memory (SOM) has emerged as a promising memory concept for high-density cross-point and three-dimensional vertical X-point (VXP) architectures by integrating selector and storage functions within a nanoscale single active material. In contrast to conventional one-selector-one-resistor (1S1R) cross-point memories, SOM exploits polarity-dependent threshold-voltage (V_{th}) modulation in amorphous chalcogenide materials, enabling nonvolatile information storage while retaining volatile selector behavior. This review provides a systematic overview of recent advances in SOM. The threshold-switching behavior and microscopic mechanisms of polarity-dependent V_{th} shift that govern SOM operation are first discussed. Strategies for improving device performance and reliability are then summarized, followed by recent progress in SOM-oriented materials screening and device modeling. Advances in array-level integration and industrial demonstrations are subsequently highlighted. Finally, the key challenges limiting the further development of SOM are discussed, and possible routes toward their resolution are outlined.

KEYWORDS: selector only memory; ovonic threshold switching; phase-change memory; amorphous chalcogenide; nonvolatile memory

1 Introduction

Continuous advances in semiconductor technology have dramatically increased computational capability over the past several decades. However, the separation between processing and memory in conventional von Neumann architectures has created a fundamental bottleneck known as the “Memory Wall” [1]. This challenge has become particularly severe in modern artificial intelligence (AI) workloads, where massive data movement between processors and memory dominates both system latency and energy consumption. Consequently, the development of new memory architectures and technologies has become a critical requirement for next-generation computing [2–6]. To address this challenge, cross-point architectures based on emerging non-volatile memories have attracted particular interest [7, 8]. In such arrays, selectors or transistors are commonly used as access devices to suppress leakage currents, and avoid sneak-path crosstalk [9–11], forming architectures such as 1S1R (one-selector-one-resistor) and 1T1R (one-transistor-one-resistor). Within this framework, chalcogenide-based ovonic threshold switching (OTS) selectors have attracted

particular attention because they combine high drive current, nanosecond-speed operation, low leakage current, and excellent scalability, and have already demonstrated industrial viability in commercial 3D memory products such as Intel Optane [12].

However, practical studies suggest that OTS selectors can already satisfy the required selector performance, whereas the resistive memory element more often becomes the dominant bottleneck in 1S1R cells, particularly as scaling aggravates the phase-change memory (PCM) component’s limitations in write program margin, thermal disturbance, endurance, and structural complexity [13]. This observation has motivated efforts to simplify the cell architecture by integrating selector and memory functionalities into a single active element, giving rise to self-selecting concepts in which one device simultaneously provides access control and information storage. An early example of such a concept was reported by Macronix in 2003 [14], where programmable threshold-voltage (V_{th}) states were realized in amorphous chalcogenide-based memory. Within this context, selector only memory (SOM) was proposed as a promising concept for next-generation storage-class memory by IMEC [15, 16] and SK hynix [13, 17, 18].

Table 1. Comparison of emerging nonvolatile memory technologies. The endurance data were primarily collected from studies [19–32]. Abbreviations: 1S1R, one-selector-one-resistor; 1T1M, one-transistor-one-magnetic-tunnel-junction; 1T1C, one-transistor-one-

capacitor. The magnetic tunnel junction serves as the storage element in MRAM, whereas the capacitor refers to a ferroelectric capacitor in FeRAM.

Comparison	PCM	RRAM	MRAM	FeRAM	SOM
Storage state	Amorphous/ polycrystal phases	Resistance state	Magnetic state	Ferroelectric polarization	V_{th} state
Nonvolatility	Yes	Yes	Yes	Yes	Yes
Endurance	$\sim 10^7$	$\sim 10^{12}$	$\sim 10^{14}$	$\sim 10^{12}$	$\sim 10^8$
Cell structure	1S1R	1S1R	1T1M	1T1C	1S0R

SOM integrates both selector and memory functionalities within a simple single-layer structure, forming an OTS-only (1S0R) architecture. Unlike conventional cross-point memories that rely on separate selector and resistive elements, this approach significantly simplifies the device structure while offering potential advantages in scalability, energy efficiency, integration density and endurance (Table 1) [13]. The operation of SOM relies on the polarity-dependent modulation of the V_{th} in chalcogenide glass materials. By applying electrical programming pulses, distinct V_{th} are created, thereby generating a memory window that enables discrimination between logic states. Although the low resistance state is volatile, the programmed V_{th} state can be retained non-volatily, allowing SOM devices to simultaneously function as both memory cells and selectors within cross-point arrays. Beyond serving as a structurally simplified alternative to cross-point arrays, SOM is also particularly attractive for 3D vertical X-point (VXP) architectures [7, 13, 18, 33], because an SOM-based VXP cell

requires only a single selector-memory layer. This simpler stack allows a smaller hole size and a more streamlined deposition process, making SOM more suitable for VXP integration. As a recently emerging memory concept, SOM remains in a rapid stage of development. Despite the increasing attention from academic and industrial communities, several challenges remain, including achieving sufficiently large and stable memory window (MW), controlling V_{th} drift and variability, and enhancing write/read endurance, and understanding the microscopic mechanisms (Figure 1).

In this review, recent advances in SOM technology are summarized. The physical mechanisms responsible for threshold switching and polarity-dependent V_{th} shift in SOM devices are discussed. Strategies for improving device performance through experimental optimization and first-principles calculations are then reviewed. Finally, recent progress in array integration and industrial demonstrations is highlighted, followed by a discussion of current challenges and possible future development pathways for SOM technologies.

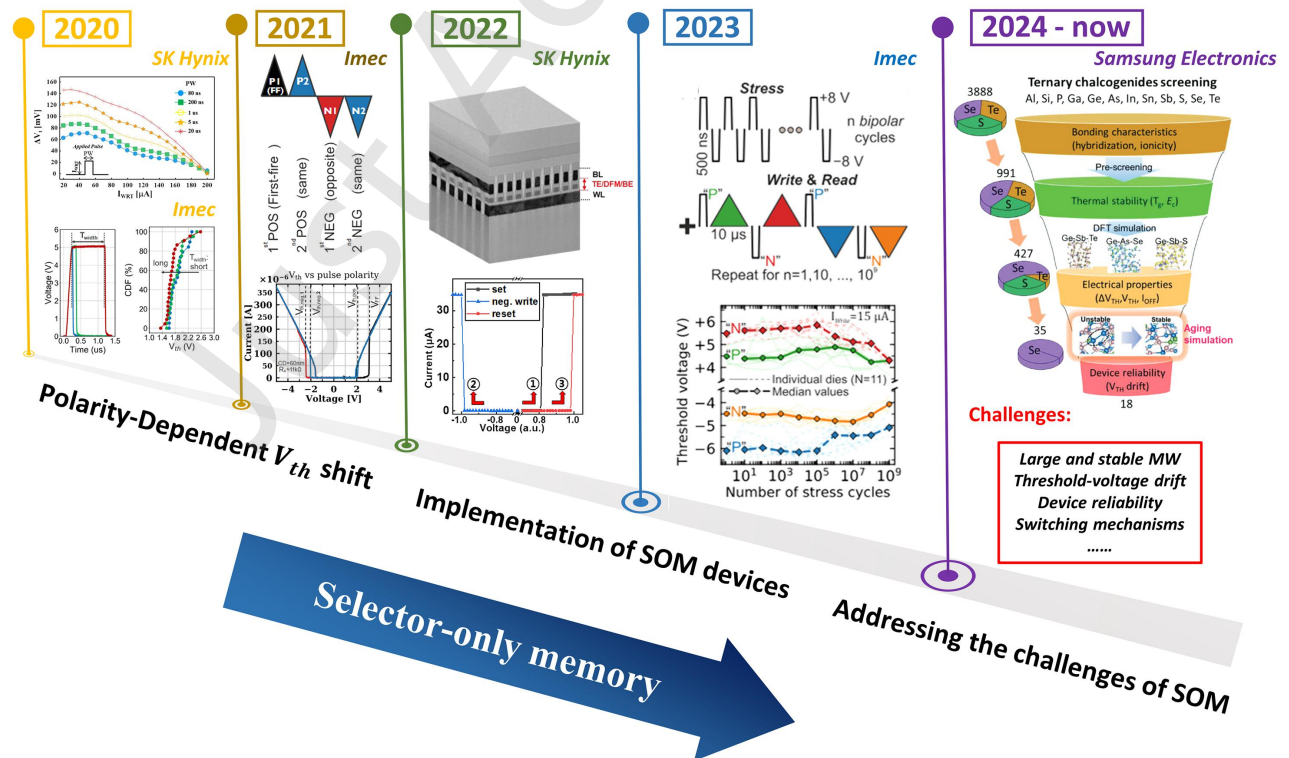


Figure 1. Timeline of some representative developments of SOM from 2020 to the present, showing the progression from polarity-dependent V_{th} shift to SOM device implementation and ongoing efforts to address key challenges for practical applications. Reproduced with permission from Ref. [15–18, 34, 35], © IEEE 2020, 2021, 2022, 2023, 2024.

2 Main mechanism of Selector Only Memory (SOM)

2.1 Threshold Switching Mechanisms

The operation of SOM is fundamentally built on the threshold-switching behavior of OTS materials. Therefore, before discussing the origin of polarity-dependent memory states in SOM, it is necessary to first consider the physical mechanisms underlying threshold-switching. Although OTS devices have been extensively studied, the microscopic origin of their abrupt transition from the high-resistance (OFF) state to the low-resistance (ON) state remains under active debate. Several models have been proposed to explain this process, as discussed below.

2.1.1 Electro-thermal models

The electro-thermal models were proposed to account for the switching phenomenon [36–40], as illustrated by the feedback loop of the thermal runaway model shown in **Figure 2a**. In this framework, Joule heating raises the local temperature of the OTS material, thereby enhancing its electrical conductivity and establishing a positive electrothermal feedback loop. This self-reinforcing process can drive an abrupt increase in conductivity and a transition to a ON state. However, although thermal models were successfully applied to describe the negative differential resistance observed in single-crystal Si-doped yttrium-iron garnet [41], they can't yield the snapback-like negative-resistance region characteristic of amorphous OTS materials [42, 43]. This limitation suggests that purely electrothermal effects are not adequate and that microscopic electronic processes must also be taken into account [44, 45]. By the early 1980s, the thermal model had largely been replaced by electric-field-driven OTS models based on electronic excitation mechanisms [46].

Although traditional purely thermal models exhibit inherent limitations, incorporating Joule-heating-induced modifications of the structure or electronic states highlights the significant contribution of thermal effects. At present, thermal effects are not regarded as an independent switching mechanism, but rather as a facilitating factor that cooperates with other mechanisms, manifesting as thermally assisted atomic/electronic structure transition [47–49]. For example, in our recent first-principles study [48], Joule-heating-induced structural transitions in OTS materials can strongly modify their electronic structure by narrowing or even closing the band gap and inducing delocalization of originally localized band-tail states in OTS+PCM devices. These changes jointly increase the carrier concentration and electronic conductivity, thereby helping to sustain the holding-ON state. These findings indicate that thermal effects still play a crucial role in the OTS devices.

2.1.2 Field-induced nucleation

The field-induced nucleation model, originally developed in the context of phase-change materials, has also been extended to explain OTS [50–53]. In this framework, a strong electric field lowers the nucleation barrier and promotes the formation of localized conductive nuclei within the amorphous chalcogenide matrix, thereby giving rise to filamentary switching behavior (**Figure 2b**). During the first firing, where a higher V_{th} is required, a metastable crystalline conductive filament forms within the initially amorphous matrix. After forming, the conductive filament does not fully revert to the initial amorphous state; some residual nuclei remain. Because these residual nucleation sites have a lower nucleation energy than the surrounding amorphous matrix, subsequent nucleation is more readily initiated at these locations. As a result, the later switching cycles exhibit faster ON switching and a smaller V_{th} . At the same time, these field-stabilized conductive nuclei are not all thermodynamically stable once the

electric field is removed, which accounts for the volatile nature of threshold switching. However, the field-induced nucleation model also faces limitations. Materials commonly used for OTS typically exhibit high crystallization temperatures, making ultrafast nucleation under electric field alone difficult to reconcile with the experimentally observed sub-nanosecond switching dynamics [7]. Therefore, field-induced nucleation processes may not act entirely independently, but may instead cooperate with electronic switching. For example, Li and Chen proposed a synergistic filamentary–electronic picture, in which carrier excitation from a seed filament induces electronic and structural changes in the surrounding amorphous material, which may in turn facilitate the formation of conductive filaments [54].

2.1.3 High-field Poole–Frenkel (PF) transport threshold switching

The high-field PF transport model proposed by Ielmini and Zhang describes threshold switching in chalcogenide-based OTS devices as a predominantly electronic process governed by field-enhanced trap-mediated transports [55, 56]. As schematically depicted in **Figure 2c**, in the low electric field, the band profile remains comparatively uniform across the amorphous film, under this condition, the electric field is distributed relatively uniformly throughout the amorphous layer, and no localized highly conductive region is formed, which describes the conduction as trap-limited PF emission conduction model. After threshold switching, however, the band diagram becomes nonuniform, and Fowler–Nordheim tunneling enables a large number of carriers to transfer from deep traps to shallow trap states, leading to an abrupt increase in current. This nonequilibrium model provides an effective explanation for several defining electrical features of OTS devices. It accounts for the abrupt snapback behavior and S-shaped current–voltage characteristic observed immediately after switching, as well as the existence of a finite holding voltage required to maintain the ON state. It also offers a natural explanation for the ultrafast switching speeds experimentally observed in OTS devices, often in the sub-nanosecond to nanosecond regime, without requiring a substantial thermal incubation time. While the model is formulated primarily as an electronic transport picture, the microscopic origin of the active shallow trap states is likely more complex. Recent studies suggest that these trap states may be associated with local structural rearrangement, compositional segregation, carrier-induced polaronic relaxation, and other field-induced microscopic processes [57–61].

2.1.4 Structural rearrangement

Beyond purely electronic descriptions, OTS in chalcogenide glasses has also been associated with structural rearrangement of the amorphous network. First-principles calculations by Guo et al. [62] showed that carrier excitation in amorphous GeSe induces additional Ge–Ge bonds and overcoordinated Ge sites, accompanied by bandgap narrowing and enhanced delocalization of the conduction states, suggesting that OTS cannot be fully described by a purely electronic transition within a fixed atomic network. Noé et al. [57], proposed a structural-rearrangement model in which OTS was described as a field-induced transformation between distinct local bonding configurations in the amorphous chalcogenide network. In this model, high electric fields and the associated electronic excitation promote local reordering of the glass, including bond alignment and the evolution of local structural motifs, leading to the formation of metastable metavalent bonds (MVBs) (i.e., locally reconfigured bonding states with enhanced electronic delocalization [63]). As illustrated in **Figure 2d** for amorphous GeSe, this structural reordering is accompanied by pronounced electronic changes: compared with the OFF state, the ON state exhibits a narrowed or even closed bandgap, an increased density of states near the Fermi level, a reduced inverse

participation ratio (IPR), and much stronger carrier delocalization. These results support a picture in which threshold switching is closely linked to dynamic local bonding rearrangement, which stabilizes a more conductive electronic state under high field. Similar structural–electronic coupling was also reported in amorphous GeS [64], where carrier excitation promoted the growth of Ge–Ge chains, increasing network connectivity and potentially facilitating the formation of conductive local paths.

2.1.5 Polaronic Effects

Polaronic effects provide another important perspective for understanding threshold switching in amorphous OTS materials. Emin [59] proposed a small polaron model to explain threshold switching in amorphous semiconductors, the threshold switching in amorphous semiconductors takes place when the small-polaron density rises to a critical steady-state level. Under this condition, adjacent polarons interfere with one another and partially cancel the lattice displacements induced by neighboring polarons, thereby suppressing carrier–phonon coupling and facilitating the emergence of high-mobility, quasi-free carriers. Although this model has faced challenge, as strong small-polaron interactions in amorphous materials are expected to occur only in rare and particular local bonding environments, thereby precluding polaron-like band

transport, it nevertheless emphasizes the important role of local atomic relaxation in modulating electronic conduction [65, 66].

Recent first-principles studies have further highlighted the role of polaron formation in OTS. Carrier excitation can induce local structural relaxation and generate midgap states, rather than merely activating a pre-existing static defect population [60, 67]. In our recent work [60], it was found that the excited state after structural relaxation exhibits newly emerged midgap states, as shown in **Figure 2e** for amorphous SiGeAsTe. Further analysis showed that these states originate primarily from carrier-induced electron–phonon coupling, rather than from purely electronic occupation changes. The spatial distribution of the midgap states also correlates closely with the regions of the largest atomic displacements, supporting their identification as polaron-related states. The same excitation-induced polaronic midgap-state formation was also found in GeSe and GeS, suggesting that this is a relatively general effect rather than a material-specific coincidence. These findings support a picture in which polaron-induced midgap states can provide positive feedback to conduction and thus promote the switch-on process. In this framework, the electric field promotes polaron formation indirectly by driving carrier excitation, while the midgap states are primarily associated with electron–phonon-like coupling rather than purely electron–electron interactions.

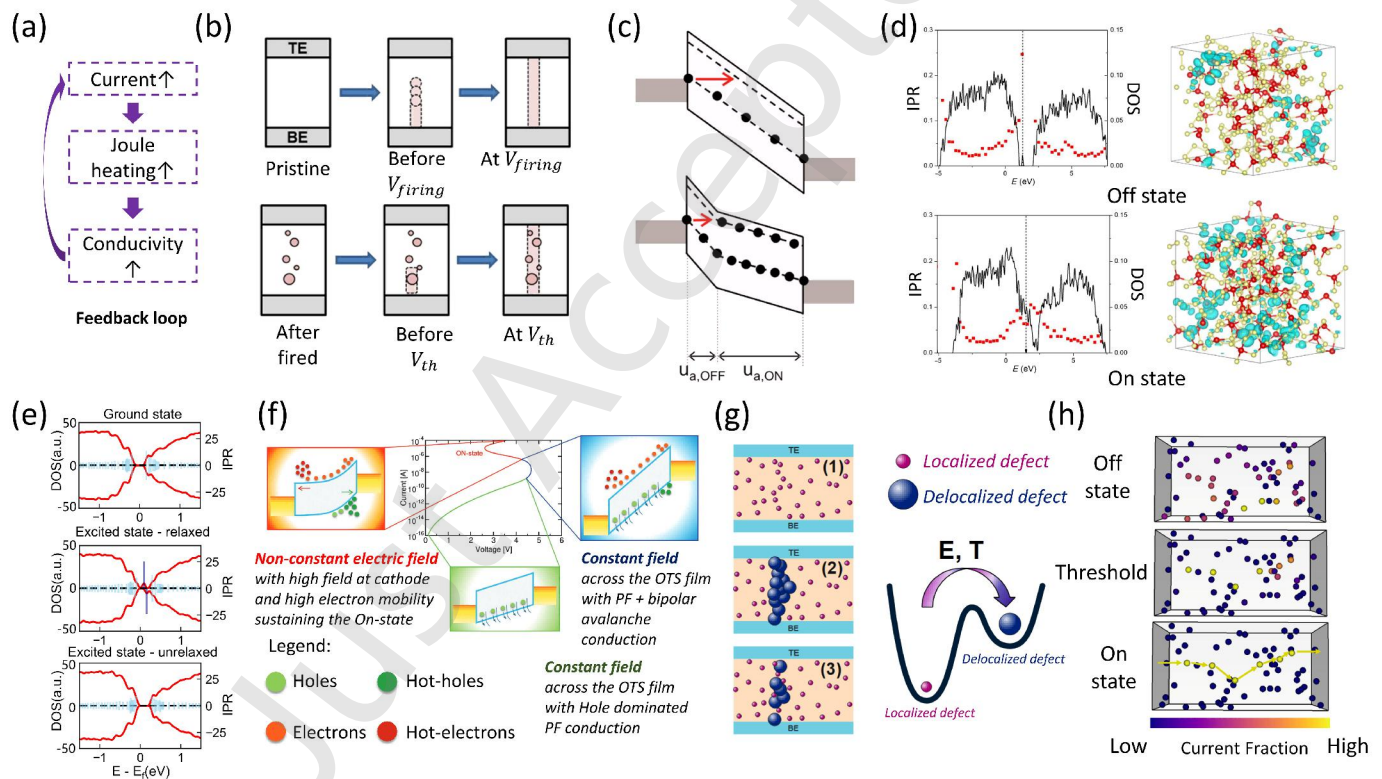


Figure 2. Schematics of threshold Switching Mechanisms. (a) Schematic of the feedback loop for thermal model. Reproduced with permission from Ref. [53], © AIP Publishing 2019. (b) Schematics of the field-induced nucleation process. Reproduced with permission from Ref. [57], © Noé P. et al. 2020. (c) Energy band schematic of High-field PF transport threshold switching model. Reproduced with permission from Ref. [55], © AIP Publishing 2019. (d) Calculated density of states (DOS) and inverse participation ratio (IPR) in off-state and on-state GeSe for Structural rearrangement. Reproduced with permission from Ref. [57], © Noé P. et al. 2020. (e) Spin-polarized DOS and IPR of ground state and excited state with/without structural relaxations. Reproduced with permission from Ref. [60], © American Chemical Society 2026. (f) Schematic band diagrams that correspond to each region in the I – V characteristics in avalanche multiplication model. Reproduced with permission from Ref. [68], © Fantini P. et al. 2023. (g) Schematic of the transition between localized and delocalized defects in OTS. Reproduced with permission from Ref. [34], © IEEE 2021. (h) Current sustained by defects for off-state, threshold and on-state. Reproduced with permission from Ref. [58], © IEEE 2023.

2.1.6 Avalanche Multiplication

Early electronic models such as the double-injection model suggested that carrier accumulation near the electrodes can strongly reshape the internal field distribution [69, 70]. In this framework, electrons and holes injected from opposite contacts recombine in the bulk, giving rise to space-charge buildup near the electrodes. As

the applied voltage increases, the space-charge regions expand and eventually overlap, leading to field collapse in the device interior and the formation of narrow barriers near the interfaces. These thin barriers facilitate carrier tunneling into the bulk, resulting in a high charge density and a quasi-metallic conductive state. Adler et al. [46] provided an electronic interpretation of OTS behavior, showing that, when the field-induced carrier generation is assumed

to proceed via impact ionization, S-shaped negative differential conductance can arise from its interplay with Shockley–Read–Hall recombination. Subsequent studies further improved this description by adding avalanche-like multiplication as a carrier-generation mechanism [71–74]. Fantini et al. [68] proposed a bipolar avalanche multiplication model (**Figure 2f**). Subthreshold conduction at low electric fields is governed by majority-carrier-dominated PF transport, whereas increasing electric field drives a transition toward bipolar impact ionization. The resulting electron–hole pair generation and cooperative transport contribute to carrier accumulation, abrupt conductivity enhancement, and the onset of snapback. They further supported this model experimentally in the subthreshold regime by extracting carrier multiplication factors from I–V characteristics, consistent with avalanche multiplication. These results support the relevance of avalanche processes in OTS switching, although their relative contribution may depend on material composition, device structure, and operating conditions. More recently, Sun et al. [75] proposed a charge-triggered switching mechanism in amorphous Se selectors, where high-density trap pairs pin the Fermi level in the OFF state, while near threshold the electrical excitation of trapped carriers, together with avalanche multiplication, triggers abrupt turn-on and high on-current. Overall, these studies indicate that avalanche multiplication can serve as an important electronic contribution to OTS switching.

2.1.7 Percolation cluster model

In the percolation cluster model, cluster formation is based on reversible transitions between localized and delocalized defect states [76, 77]. In this framework, each defect is treated as a two-state entity within a double-well potential, and the transition rates are governed by the local electric field and temperature. Because the delocalized state has a larger spatial extent than the localized state, electrical turn-on can occur when a sufficient number of neighboring defects become delocalized and overlap, thereby forming a percolative conductive cluster across the amorphous layer. As illustrated in **Figure 2g**, the OFF state corresponds to a configuration in which most defects remain localized, whereas threshold switching occurs when defect delocalization becomes sufficiently extensive to establish a spanning conductive cluster. The subsequent recovery of defects toward localized states disrupts the cluster and restores the OFF state, thereby accounting for the volatile character of OTS switching. This model provides a phenomenological framework for rationalizing several characteristic OTS behaviors, including ON-current increase, V_{th} drift and switching-induced V_{th} variation [15, 76]. Although several experimental observations are not fully reconciled within this framework, including the much stronger dependence of switching speed on applied voltage than on temperature, and the excellent cycle-to-cycle (C2C) uniformity reported in some devices, which may be difficult to fully reconcile with repeated cluster formation and rupture processes [78–80], the percolation cluster model offers an effective intuitive phenomenological picture.

Recently, Buscemi et al. [58] introduced a hydrodynamic multiphonon Trap-Assisted Tunneling (TAT) model for describing electrical transport and threshold switching in chalcogenide OTS devices. In this framework, charge transport proceeds through multiphonon TAT between localized defect states, resulting in the occurrence of temporary and progressive localization-delocalization of the trap states, creating conductive channels inside the insulating matrix, as given in **Figure 2h**. The model successfully reproduces the characteristic I–V features of OTS devices, including the abrupt turn-on at threshold, the subsequent snapback associated with negative differential resistance, and the holding condition that governs the stability of the ON state. Nevertheless, its description of switching remains partly phenomenological, as the microscopic origin and dynamics of the localized-to-delocalized transition are not yet fully resolved.

2.2 Mechanisms of Polarity-Dependent V_{th} Shift

Polarity-dependent V_{th} shift is the key physical basis of SOM, enabling reversible programming between low- V_{th} and high- V_{th} states with polarity voltage pulses, to achieve data storage function. The microscopic origin of this behavior remains not clear. This section discusses representative mechanisms proposed for polarity-dependent V_{th} shift in SOM.

2.2.1 Polarity-Dependent Traps

One plausible explanation for the polarity-dependent V_{th} shift in SOM is trap-mediated electronic reconfiguration. The essential idea is that polarity-dependent switching originates from an asymmetric evolution of the trap landscape after programming, which subsequently alters the threshold-switching condition under the following read pulse. Earlier studies on chalcogenide glasses suggested that valence-alternation-pair (VAP) related defect centers can undergo excitation-induced charge transfer, accompanied by local structural rearrangement and micro-anisotropy [81]. Consistent with this general defect-based perspective, Ravsher et al. [82] proposed that switching of field-sensitive defects should be one possible origin of the polarity effect in Se-based SOM devices, based on their earlier two-state model for OTS materials [76] in which defects are described as anisotropic structural units (ASUs) that can undergo localization–delocalization transitions in a double-well potential. Because the transition probability depends on the orientation of the ASU relative to the applied electric field, opposite programming polarities can selectively favor different defect subpopulations. As a result, the retained defect configuration after programming becomes either more or less favorable for subsequent switch-on, leading to different V_{th} states and thus a memory window (**Figure 3a**).

Lee et al. [49] showed that the activation energy for carrier transport exhibits a strong dependence on the programmed state, whereas the effective inter-trap spacing remains nearly unchanged. Based on thermally assisted hopping analysis [83], they extracted both the trap spacing (Δz) and activation energy (E_a) for different memory states and found that the state dependence is dominated by changes in E_a but not Δz (**Figure 3b**). These results suggest that opposite write polarities primarily alter trap condition or energetic alignment. Sung et al. [84] suggested that polarity-dependent V_{th} shifts in amorphous chalcogenide SOM originate from the redistribution of charged defects, with VAPs and dimer-type defects serving as trap centers. Under opposite programming polarities, charged defects near the electrode interfaces are redistributed into distinct configurations, leading to different transport barriers (**Figure 3c**).

2.2.2 Segregation

Ravsher et al. [82] proposed atomic segregation as one possible mechanism underlying the polarity effect in Se-based SOM devices. In this picture, the field-assisted atomic motion within the amorphous chalcogenide layer, leading to polarity-dependent compositional redistribution in the bulk or near the electrode interfaces. Such structural and chemical asymmetry can modify key transport parameters, including the trap distribution, and charge-injection barriers, thereby producing distinct threshold-switching conditions after opposite programming polarities. First-principles calculations further support this interpretation, showing that compositional segregation can induce different electronic structures at the two sides of the device and thereby modulate the mobility gap and charge-injection barriers [85]. More recently, in Sb_2Se_3 -based SOM, an applied electric field drives controllable migration of Sb and Se atoms, observed by in situ transmission electron microscopy (TEM), further supporting a migration-related contribution to SOM operation [86].

However, some experimental evidence suggests that this mechanism may become important mainly under relatively strong electrical and thermal stress. In GeSe-based SOM device [87], pronounced elemental segregation was observed only at high operating current (I_{op}), indicating that large-scale atomic migration is more likely to occur under high-current conditions. Consistently, studies on SiGeAsSe devices showed no major compositional difference between states programmed with opposite polarities [82]. Although a slight Se enrichment near the positively biased interface was detected, the variation was small and remained within the uncertainty of Energy-dispersive X-ray spectroscopy (EDS) analysis (**Figure 3d**). Nevertheless, it is still plausible that some atomic migration is happening on a local scale below the sensitivity of EDS. These results suggest that atomic segregation is a plausible contributor to the polarity effect, but its role under low-current SOM operation may be limited or secondary.

2.2.3 Avalanche-Based Models

Based on the bipolar avalanche framework [68], Ha-Jun Sung et al. [35] described the memory window of SOM using a space-charge-region (SCR) model. In this model, charged defects generated during the first-firing process and retained after RESET induce band bending near the electrode interfaces, thereby increasing the activation energy for carrier emission during subsequent read operations. By modulating the extent of the SCR under a nonuniform electric field, the spatial distribution of charged defects gives rise to polarity-dependent barrier modulation and thus a measurable memory window.

Fantini et al. [67] proposed a graded band gap (GBG) model as a microscopic explanation for polarity-dependent V_{th} shifts in SOM, building on their bipolar avalanche threshold-switching description. In this mechanism, the programming pulse establishes an asymmetric injection landscape across the chalcogenide film. Near the anode, strong electron injection induces local defect-state relaxation that lowers the activation energy for hole injection and enhances subthreshold conduction. Near the cathode, the strong electric field suppresses or removes part of the in-gap localized states, thereby increasing the corresponding hole-injection barrier. As a result, when the subsequent read pulse has the same polarity as

the programming pulse, holes are injected from the low-barrier side and V_{th} is lower; under the opposite polarity, holes are injected from the high-barrier side and V_{th} becomes higher, thereby forming the memory window (**Figure 3e**). Density Functional Theory (DFT) calculations provide atomistic support for this process, which show that electron injection into amorphous chalcogenide models can induce localized electronic states together with local structural relaxation. Importantly, the resulting downward shift of in-gap states toward the valence band persists even after the injected electrons are removed (**Figure 3f**). The resulting asymmetric distribution of in-gap states across the film thickness modifies carrier-injection barriers under opposite read polarities and thus gives rise to polarity-dependent V_{th} . A notable strength of the GBG model is that it can be directly implemented in Technology Computer Aided Design (TCAD), enabling quantitative reproduction of experimentally observed polarity-window trends.

Overall, each proposed mechanism captures part of the polarity effect in SOM, yet none has been fully established as a universal picture. Trap-based models are attractive because E_a and Δz can be extracted experimentally from trap assisted hopping analyses. However, the microscopic origin, spatial distribution, and long-term stability of the asymmetric defect configurations responsible for the programmed V_{th} states remain insufficiently understood. Segregation-related mechanisms have been supported by direct experimental observations, but in uniform materials their influence may be confined mainly to the near-electrode regions, and excessive field- or heat-assisted migration may eventually accelerate device degradation. The SCR model provides an intuitive description of polarity-dependent barrier modulation, but still requires more direct experimental validation of the proposed charged-defect distribution and interfacial band bending. The GBG model can quantitatively reproduce several key experimental trends, including the dependence of memory window on temperature, thickness, and alloy composition, yet its microscopic assumptions also await more direct experimental confirmation. Taken together, these results suggest that the physical origin of SOM operation is still at an early stage of development, and further combined experimental, theoretical, and multiscale modeling studies are needed to establish a more complete and predictive understanding.

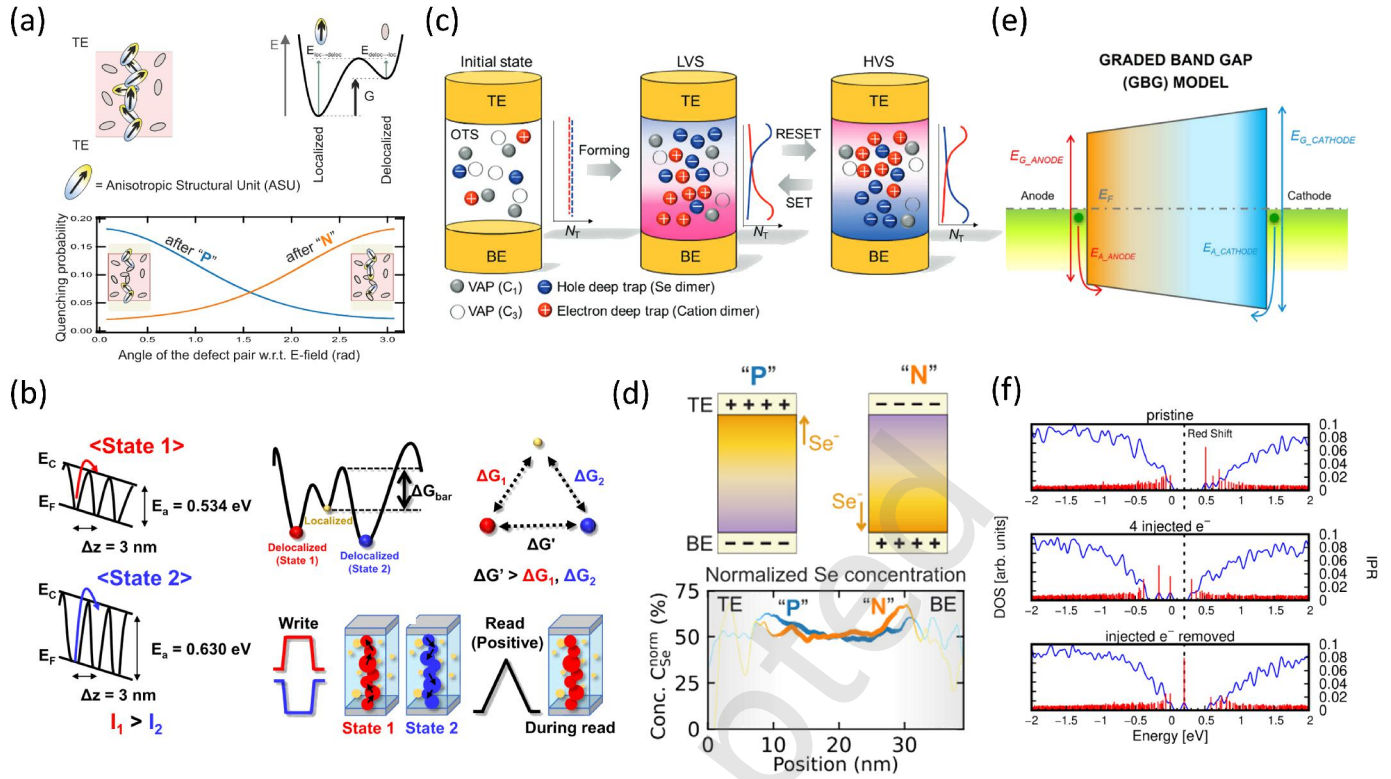


Figure 3. Mechanisms of Polarity-Dependent V_{th} Shift in SOM. (a) Schematic of Anisotropic structural units (ASUs) that can undergo localization–delocalization transitions in a double-well potential. Reproduced with permission from Ref. [82], © IEEE 2024. (b) Schematic illustration of the SOM mechanism, in which 2 delocalized defect-state energetics and their field-driven transitions govern threshold switching and memory window formation. Reproduced with permission from Ref. [49], © IEEE 2024. (c) Polarity-dependent evolution of charged-defect distribution into low- V_{th} and high- V_{th} states (LVS/HVS). Reproduced from Ref. [84] under the terms of the CC BY 4.0 license, © Sung H. et al. 2024. (d) Schematic illustration of field-induced elemental segregation and the comparison of relative Se concentration between the two samples, showing only minor compositional differences between the two states. Reproduced with permission from Ref. [82], © IEEE 2024. (e) Schematic illustration of the Graded Band Gap (GBG) model with the two different activation energies (E_a) for hole injection at the anode and cathode. (f) Amorphous $Ge_{25}As_{30}Se_{45}$ electronic density of states with and without injected electrons. (e-f) Reproduced with permission from Ref. [88], © Fantini P. et al. 2026, Springer Nature.

Table 2. Summary of some representative works of SOM devices and their performances. *The specific material composition was not reported. Abbreviations: HUST, Huazhong University of Science and Technology; POSTECH, Pohang University of Science and Technology; SIMIT, Shanghai Institute of Microsystem and Information Technology.

Year	Main affiliation	Material	Memory window	Retention	Write Endurance	Read Endurance	I_{write} (μ A)	T_{write} (ns)	Ref
2022	SK Hynix	OTS*	~ 0.2 V	85 °C/1 d	10^7		< 30	20	[18]
2023	KU Leuven/IMEC	SiGeAsSe*	~ 0.9 V	> 1 month	$> 10^8$	$> 10^6$	< 15	~ 10	[16]
2023	POSTECH	$Se_{0.5}(Si_{15}Te_{34}As_{42}Ge_9)_{0.5}$	> 1.2 V	> 10 years at RT	$> 10^8$		< 100	~ 10	[89]
2023	Samsung	Se based OTS*	> 0.5 V		10^8	10^9	40	56	[32]
2024	IBM/Macronix	Cu-doped GeSe	1.5 V	85 °C/1 d	$> 10^8$		10	25	[90]
2024	SK Hynix	OTS*	> 0.75 V	> 10 years at 125 °C	10^8	10^9	20	30	[31]
2024	IBM/Macronix	$Ge_{56}Se_{44}$	1.5 V	85 °C/1 d	$> 10^5$		100/393 (Reset/Set)	$10^3/50$	[91]
2024	POSTECH	$Se_{55}(Si_{14}Te_{38}As_{39}Ge_9)_{45}$	> 1 V		10^8			40	[92]
2025	Yonsei University	In-doped GeSbSeTe	1.5 V	> 2 hours at 85 °C	$> 10^8$			500	[93]
2025	HUST	In-doped GeSe	1.3 V	> 1000 s	10^6	10^9		100	[94]
2025	SK Hynix	OTS*			$> 10^7$		≤ 20	35	[95]
2025	Samsung	OTS*	> 0.75 V	> 10 years at 85 °C	$> 10^7$	$> 10^9$	20	50	[96]
2025	POSTECH	Multi-Stack InTe	1.15 V		$\sim 10^{10}$	10^8	10	1000	[97]
2025	HUST	Ga-doped GeSe	1.83 V		10^9			50	[98]
2025	POSTECH	Sb-InTe Hybrid stacked	> 1.3 V	> 10 years at RT	$\sim 10^{10}$	10^{10}	10	10	[99]
2026	Korea University	Si-doped GeS	~ 2.3 V	$> 10^7$ s	2×10^8				[100]
2026	SIMIT	Sb_2Se_3	~ 2 V	$> 10^8$ s at 85 °C	$> 10^7$			20	[86]

3 Strategies for Performance and Reliability Engineering of SOM

The dual-functional nature of SOM, in which a single active material must serve as both selector and memory, imposes stringent requirements on device operation and state stability. For practical operation, SOM devices must not only exhibit reliable threshold switching, but also generate and preserve distinguishable polarity-dependent V_{th} states for information storage. These requirements are reflected in several key device metrics, including memory window, V_{th} variability, retention, endurance, programming current, and speed. Some representative advances in SOM based on amorphous chalcogenide materials are summarized in **Table 2**, and the main strategies for performance and reliability enhancement are discussed below.

3.1 Performance Enhancement Strategies for SOM Devices

3.1.1 Compositional Optimization

Compositional optimization is important for improving SOM performance as the elemental composition directly affect the bonding configuration, trap landscape, and polarity-dependent switching behavior of the active layer. In Ge–Se-based SOM devices, tuning the Ge/Se ratio has been shown to systematically modify the threshold-switching characteristics, memory window magnitude, and device reliability [91]. Three GeSe compositions were compared, $Ge_{61}Se_{39}$ (Ge-rich), $Ge_{56}Se_{44}$ (middle), and $Ge_{35}Se_{65}$ (Se-rich) as shown in **Figure 4a–c**. The V_{th} increases progressively with increasing Se content, while the intermediate composition, $Ge_{56}Se_{44}$, exhibits the largest memory window ($\Delta V_t = V_{tR} - V_{tS}$) of 1.3 V compared with the Ge-rich and Se-rich compositions (**Figure 4b,c**). These results suggest that optimized compositions provide an effective route for enhancing memory window, state stability and reducing operational variability.

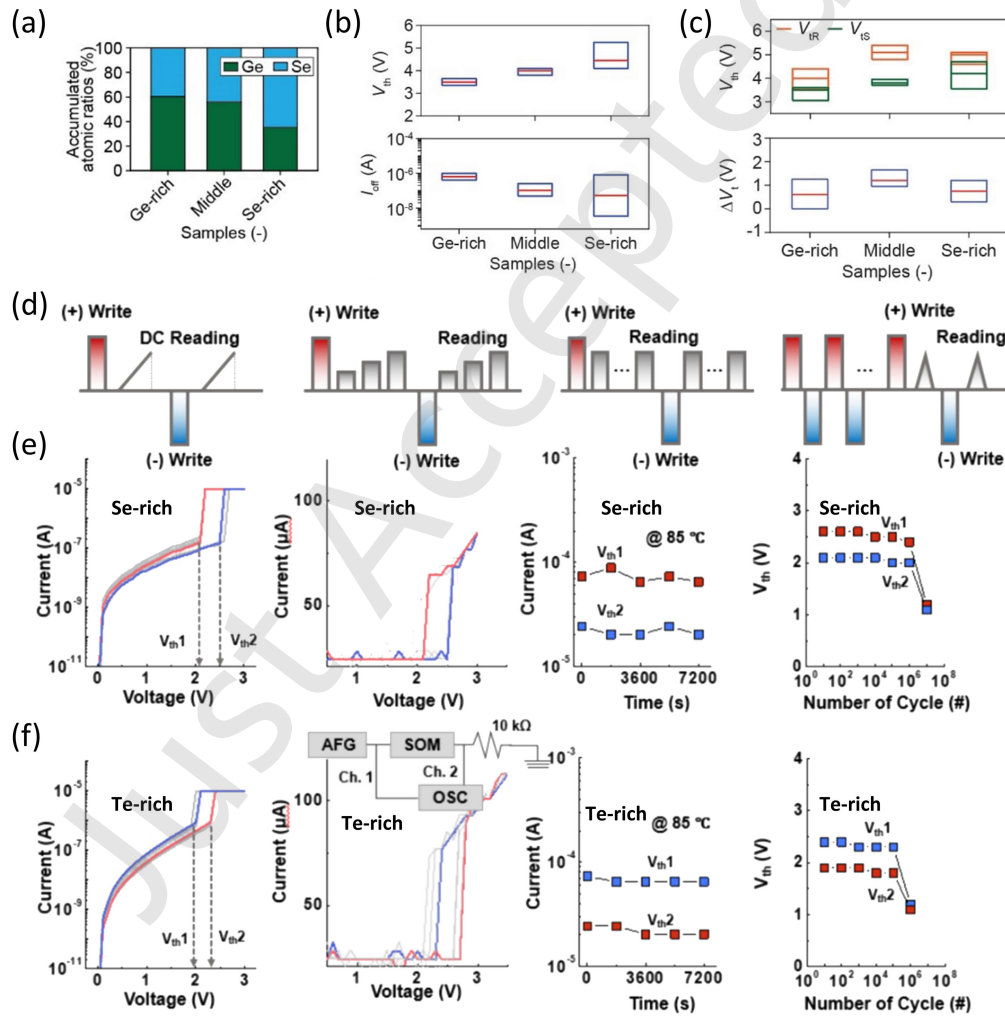


Figure 4. (a) Compositions of GeSe-based SOM (b) Ge_xSe_{1-x} 's V_{th} increases (top) and I_{off} decreases (bottom) with higher Se content. (c) The top panel indicates the variation of reset voltage (V_{tR}) and set voltage (V_{tS}). The bottom panel demonstrates the ΔV_t with increased Se content. The upper and lower edges of the boxes represent the 75 and 25 percentiles of the data. (a–c) Reproduced with permission from Ref. [91], © Springer Nature 2024. (d) Voltage schemes used for electrical characterization of SOM devices. (e,f) Electrical characteristics, memory characteristics, and endurance performance of Se-rich and Te-rich SOM. (d–f) Reproduced with permission from Ref. [101], © Elsevier 2026.

The importance of composition becomes even more evident in Ge–Se–Te materials, where compositional variation can alter not only the memory window magnitude and electrical characteristics, but even the polarity-switching direction itself [101]. Se-rich ($Ge_{34}Se_{45}Te_{21}$) and Te-rich ($Ge_{26}Se_{23}Te_{51}$) compositions were

compared. As seen in **Figures 4d–f**, the two devices with different compositions exhibit opposite polarity-dependent switching characteristics. In both SOM devices, the individual V_{th} states were stably maintained under accelerated retention conditions, confirming their reliable non-volatile characteristics. However,

when a negative-voltage write pulse was applied, the threshold voltage of Se-rich increased, whereas that of Te-rich decreased.

These observations highlight compositional optimization as a critical and practically indispensable step for SOM device. In practice, compositional tuning provides an important materials-level route for balancing polarity response, stability, and reliability before further device-level optimization [102]. It is therefore an important part of SOM materials engineering alongside doping and other performance-enhancement strategies.

3.1.2 Doping

Doping engineering is an effective and widely used strategy for enhancing device performance. By introducing selected foreign atoms into chalcogenide hosts, doping can modify the local bonding configuration, defect-state energetics, atomic migration kinetics, and the structural stability of the amorphous network. One effective idea of doping is to suppress electric field-induced atomic or structural rearrangement, thereby improving threshold stability and device reliability. Wen et al. [94] showed that In doping in GeSe-based materials improves both memory window size and write endurance by suppressing excessive Se migration during repeated

switching. The V_{th} and memory window vary with indium concentration (Figure 5a), but the endurance improvement is non-monotonic, with the best performance obtained at 3% indium rather than at higher concentrations (Figure 5b). This result indicates that optimizing device performance is a process that requires comprehensive consideration. A similar stabilization effect is observed for Ga doping in GeSe SOM. [98] A Ga concentration of 6% Ga doping yields a minimum C2C (cycle-to-cycle) variability (Figure 5c), and the corresponding V_{th} drift is reduced to 16.5 mV/decade, less than half that of undoped device (Figure 5d). This improvement is associated with strong Ga–Se bonding, which suppresses atomic diffusion and stabilizes the defect configuration during switching. Si doping likewise improves reliability by suppressing unstable homopolar bonds and strengthening the amorphous backbone [100, 103]. As illustrated in Figure 5e–h, Si-doped GeS SOM exhibits a larger memory window than undoped GeS, together with greatly enhanced endurance and retention, increasing from $\sim 4 \times 10^6$ to beyond 4×10^8 cycles, and the retention extends from $> 3 \times 10^5$ s to beyond 10^7 s, respectively. Moreover, the memory window broadens progressively with increasing Si concentration (Figure 5h).

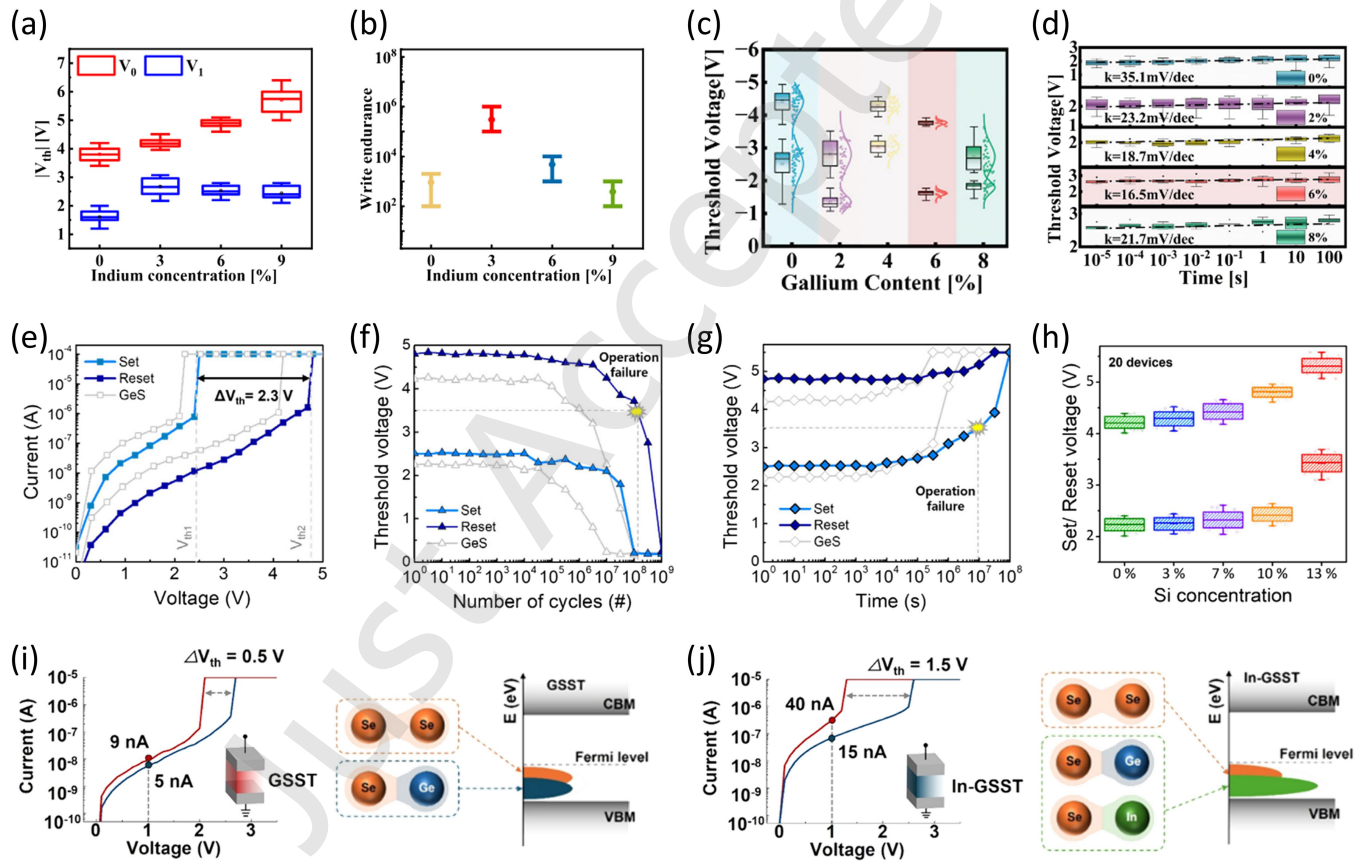


Figure 5. (a) Memory window and (b) Endurance in GeSe-based SOM devices of different In concentrations. (a,b) Reproduced with permission from Ref. [94], © IEEE 2025. (c) C2C distributions and (d) V_{th} relaxation of GeSe-based SOM with varying Ga concentrations. (c,d) Reproduced with permission from Ref. [98], © IEEE 2025. Reliability and multi-level operation characteristics of Si-doped GeS-based SOM devices: (e) I–V curve of the Si-doped GeS-based SOM device. (f) Endurance characteristics of the Si–GeS device. (g) Data retention characteristics of the Si–GeS device. (h) V_{th} dependence on Si concentration. (e–h) Reproduced with permission from Ref. [100], © Elsevier 2026. The I–V curve and band diagrams of (i) GSST-based SOM. and (j) In-GSST-based SOM. Reproduced with permission from Ref. [93], © Elsevier 2025.

From an energetic perspective, the effect of doping is more explicitly manifested in the direct modulation of the trap landscape responsible for memory window formation. In GeSbSeTe (GSST), Indium doping enhances the memory window by altering the local bonding environments around Se atoms and introduces In–Se heterobonds at the expense of part of the original Ge–Se bonding network by XPS analysis, thereby changing the local chemical environments around Se atoms [93, 104]. Se–Se homopolar bonds

tend to form relatively deep traps, whereas heteropolar bonds such as Se–Ge and Se–In are associated with shallower traps. As a result, Indium doping shifts the trap population toward shallower states and further lowers the trap depth of the low- V_{th} state relative to the high- V_{th} state. This enlarged inter-state trap-depth contrast directly widens the separation between two V_{th} states, leading to a substantial increase in memory window. Compared with undoped GSST, the memory window increases from about 0.5 V to about 1.5 V after Indium doping (Figures 5i,j). These changes strengthen the

polarity-dependent V_{th} separation and improve the distinguishability of memory states. A similar trap-landscape engineering effect has also been demonstrated by Sn doping in GSST-based SOM. Seo et al. showed that Sn incorporation broadens the memory window from about 0.4 to 0.8 V by reducing trap depth and increasing the population of shallow band-tail trap states, thereby improving the distinguishability and stability of the programmed threshold states and enhanced endurance [105]. These examples highlight that, beyond suppressing structural rearrangement, doping can also enhance SOM performance through more direct engineering of defect energetics.

Overall, doping improves SOM performance through coupled structural and electronic effects, but balancing different performance metrics is equally important. In many cases, excessive doping can degrade characteristics, such as endurance, V_{th} stability, and switching speed, reflecting inherent trade-offs [94, 98, 100, 104]. Therefore, doping in SOM requires a comprehensive mechanism-informed strategy to balance these competing performance requirements.

3.1.3 Post-treatment

Chalcogenide-based amorphous alloys contain abundant defects, and not all defect states are beneficial for memory window

formation or switching stability. Excessive or unstable defect populations may aggravate V_{th} drift and C2C variability. Microwave annealing (MWA) and ultraviolet (UV) exposure has been reported as an effective means of regulating bonding configurations and defect populations after film deposition, thereby improving V_{th} uniformity, suppressing drift and variability, and enhancing endurance and retention without altering the material composition or device architecture in OTS [106, 107]. Similar approaches have therefore been explored to stabilize switching behavior in Se-based chalcogenide SOM.

In Se-based SOM systems, unstable Se-Se homopolar bonds have been identified as one important origin of switching variability and nonuniformity [49, 108]. MWA has been shown to improve switching uniformity by suppressing these bonds and thereby reducing the number of switching-active traps [109]. Raman analysis confirmed the reduction in the number of traps that induce memory switching by the decreased of the Se-Se bonding peak after MWA treatment (**Figure 6a,b**) [110, 111]. As a result, the treated device retained a similar average memory window but exhibited a much tighter V_{th} distribution than the untreated control (**Figure 6c,d**). However, excessive MWA led to overall structural degradation, indicating that the benefit of defect reduction must be balanced against preservation of network integrity.

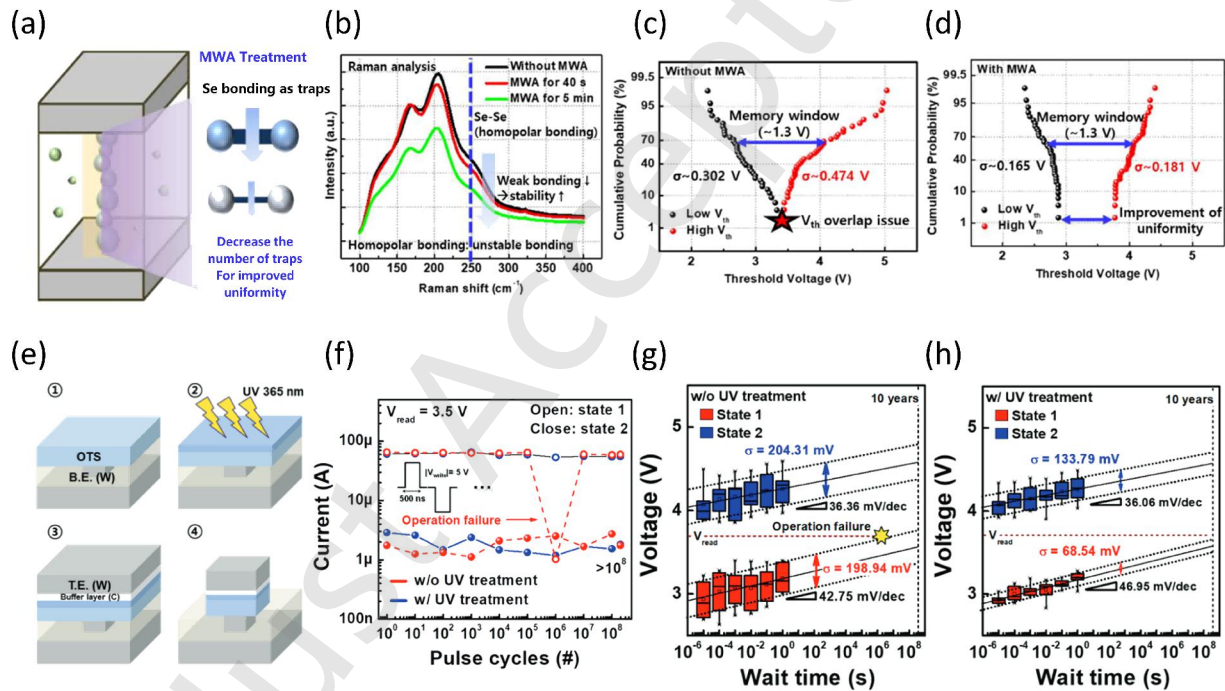


Figure 6. (a) Schematic structure of MWA treatment. (b) Raman spectroscopy analysis of SOM devices. V_{th} distribution of SOM with (c) and without (d) MWA. (a-d) Reproduced with permission from Ref. [109], © IEEE 2024.. (e) The fabrication flow for the UV-treated OTS device. (f) Cycling endurance characteristics of the film with and without UV treatment. V_{th} drift characteristics of OTS devices (g) before and (h) after the UV treatment. (e-h) Reproduced with permission from Ref. [89], © IEEE 2023.

UV treatment likewise provides an effective route for stabilizing Se-based SOM devices [89]. By inducing localized bond rearrangement and reducing electrically active interface states, UV exposure improves the stability of programmed defect configurations. Although both treated and untreated devices showed endurance exceeding 10^8 cycles, UV-treated devices exhibited much lower variability and markedly improved retention, while the untreated devices suffered from large V_{th} variation and poor retention behavior (**Figures 6e–h**). Notably, the retention improvement was achieved without a substantial change in the V_{th} drift slope, indicating that variability reduction, rather than drift suppression itself, was the key factor underlying the enhanced

retention. Similar to MWA, excessive treatment can also degrade device performance; therefore, the treatment duration needs to be carefully optimized.

Overall, post-treatment highlights the importance of defect conditioning after film deposition in SOM devices. When properly optimized, such treatments provide an effective route to improve switching uniformity and long-term reliability, serving as a defect-regulation strategy that does not require changes in material composition or device structure.

3.1.4 Pulse-Scheme Engineering

Pulse-scheme engineering is an important operation-level strategy for SOM because the programmed threshold state is highly

sensitive to the temporal profile of the applied voltage. In OTS-based materials, V_{th} can be influenced by multiple pulse parameters, including polarity [112, 113], amplitude [17], width [49, 114], rise time [15], and fall time [115], indicating that the pulse configuration affects not only switching itself but also the stability and accessibility of the stored threshold states. Therefore, optimization of the pulse scheme is essential for improving SOM performance.

In SOM operation, write pulses are typically stronger than read pulses and thus impose a greater reliability burden on the device. In particular, the use of square (SQ) voltage pulses during programming often induces an overshoot current (I_{over}), which can degrade device performance and even cause device damage [116].

To suppress this effect, Seo et al. [92] introduced an optimized multi-step (MS) pulse scheme for SOM. As shown in **Figure 7a**, the abrupt OFF-to-ON transition under a SQ pulse causes rapid discharge of the parasitic capacitance, producing a pronounced I_{over} . In contrast, the MS pulse enables a more controlled switching event. When the rising-step amplitude exceeds V_{th} , the device turns on during the intermediate step rather than at the full programming voltage, reducing I_{over} by about 40%. The same strategy also mitigates the undershoot current (I_{under}) during turn-off by reducing the instantaneous voltage drop and moderating the collapse of the conductive path [117, 118]. These results show that properly designed pulse sequences can effectively reduce transient-current stress and improve programming reliability.

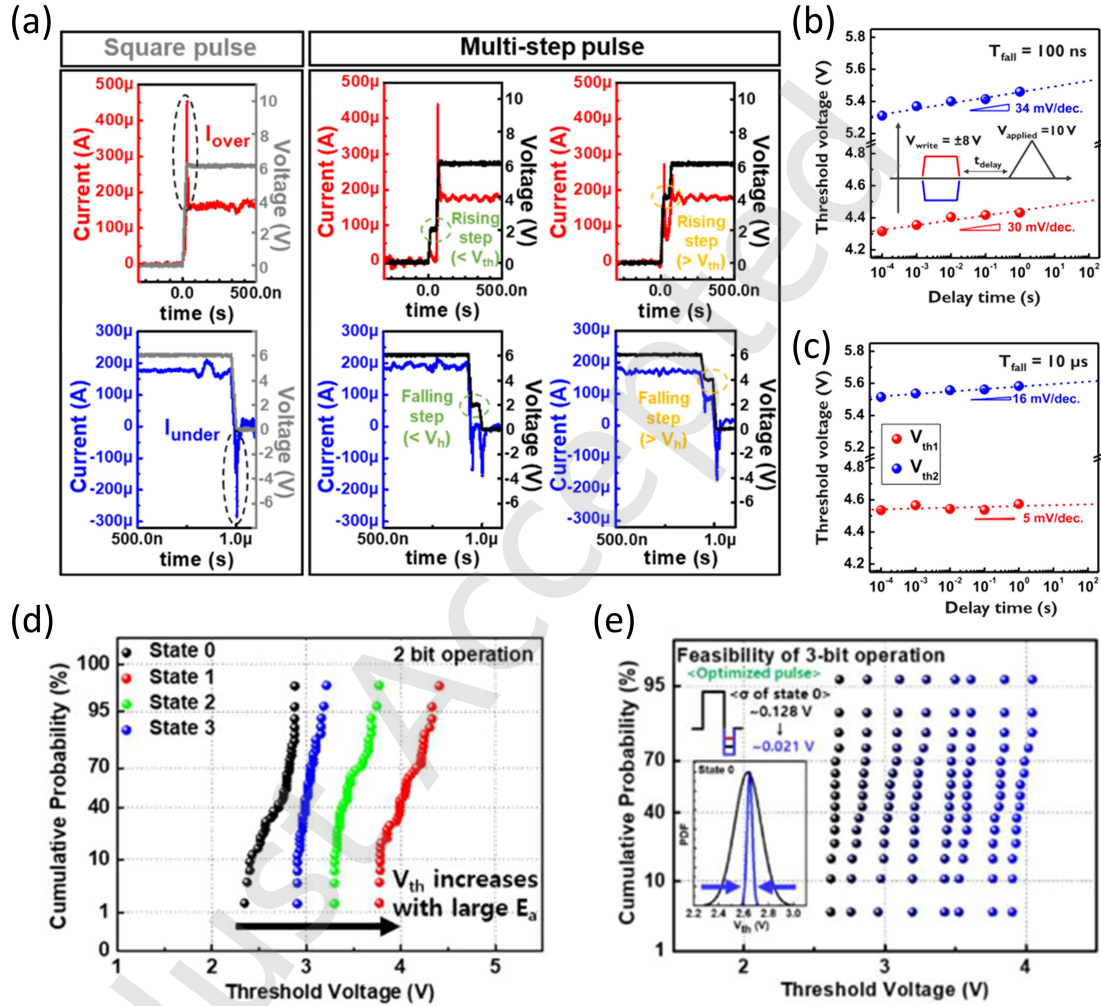


Figure 7. (a) Optimization of rising and falling steps in the multi-step (MS) pulse for write pulse. Reproduced with permission [92]. (b,c) V_{th} drift as a function of delay time at 100 ns and 10 μs. Reproduced with permission from Ref. [119], © IEEE 2025. (d) Cumulative probability result of V_{th} in each state with bipolar pulse scheme. 2-bit operation was confirmed without overlap. (e) Cumulative probability curve of device-to-device V_{th} using optimizing programming pulse scheme for lower σ value, exhibiting the feasibility of 3-bit operation. (d,e) Reproduced with permission from Ref. [109], © IEEE 2024.

In addition to transient-current suppression, the falling time (T_{fall}) of the programming pulse also plays an important role in regulating V_{th} drift in SOM devices. Lee et al. [119] showed that increasing T_{fall} from 100 ns to 10 μs significantly improved the drift characteristics from about 30 mV dec^{-1} to below 10 mV dec^{-1} for both memory states (**Figure 7b,c**). Similarly, Song et al. [120] reported that optimization of the T_{fall} can also improve the memory window and endurance of SOM devices, enlarging the memory margin from 0.6 to 1.4 V and enhancing endurance by four orders of magnitude. However, these improvements were accompanied by an 18% increase in the OFF-state current and broader C2C distributions, highlighting the trade-off between improved memory

characteristics and increased leakage or variability.

Beyond reliability optimization, pulse-scheme engineering also provides a direct route to multilevel and multibit SOM operation. Because the programmed V_{th} state depends on the write-pulse condition, tailored pulse sequences can be used to generate multiple nonvolatile threshold states with controlled separation. Jung et al. [109] demonstrated that improved V_{th} uniformity enabled multibit operation in SOM devices, including 2-bit operation with excellent endurance and retention, and the feasibility of 3-bit operation with tight V_{th} distribution as presented in **Figure 7d,e**. Seo et al. [121] further developed a pulse-based programming algorithm for reliable multilevel V_{th} control and demonstrated stable 3-bit operation with low adjacent-state overlap, which was subsequently extended to a 4k crossbar array. These studies show

that pulse programming in SOM is not limited to stress mitigation, but can also be used to define and access multiple memory states in a controllable manner.

In summary, pulse-scheme engineering offers a fabrication-compatible and low-cost route to improve SOM performance at the operation level. By controlling transient current, T_{fall} and programmed-state separation, it can optimize reliability, V_{th} drift, and achieve multibit programmability.

3.1.5 Structural Innovation

Optimizing device structure provides a feasible and promising route for improving SOM performance. In SOM devices, the memory and selector functions are integrated within a homogeneous single amorphous layer, making it difficult to simultaneously optimize memory window formation, leakage suppression, endurance, and operating current. By intentionally breaking this structural homogeneity, strategies based on functional decoupling can help relax these intrinsic trade-offs.

A related strategy was demonstrated in a multi-stack design, in which the trap distribution was deliberately engineered by using different compositions on the two sides to improve endurance and reduce the write current [97, 99]. As illustrated in **Figure 8a**, the SOM device was separated into a memory-switching layer and a selector-switching layer. In such a structure, each layer can be independently engineered to perform its respective function, thereby enabling bifunctional switching behavior while overcoming the intrinsic limitations of homogeneous single-layer designs. As depicted in **Figure 8b**, devices with an interlayer thickness of $t_i = 3$ nm exhibited a sufficiently large memory window (> 1.3 V) together with a low OFF-state current (I_{off}). Structural innovation can also be implemented by shifting the defect source from the active layer to the electrode side. Because Cu atoms are mobile under an electric field, and have been reported to be utilized in SOM devices [90]. Exploiting this characteristic, Lee et al. [122] achieved SOM functionality in an OTS device by introducing Cu from an external electrode together with a C diffusion barrier. The C barrier is used to regulate excessive Cu migration, enabling stable operation with a memory window of approximately 3 V (**Figure 8c**). In contrast, the device without Cu did not exhibit SOM characteristics (**Figure 8d**), whereas the device without the C blocking layer showed conductive-filament-based RRAM behavior (**Figure 8e**). This result highlights that controlled defect supply from external structural components can provide an alternative

route to SOM operation without relying solely on intrinsic defect formation within the amorphous layer. Taken together, these examples demonstrate that structural innovation offers a powerful means of improving SOM performance through spatial decoupling of competing functions. By separating memory formation, selector switching, and defect regulation into different structural regions, these strategies alleviate the intrinsic constraints of single-layer devices and open a more flexible route for optimizing memory window, leakage, endurance, and operating current simultaneously.

Overall, the performance-enhancement strategies discussed above do not represent independent optimization routes; rather, they constitute complementary approaches acting at different levels of SOM device. At the materials level, compositional optimization determines the basic bonding configuration, defect distribution, and polarity-dependent switching characteristics of the amorphous active layer. Doping provides a more targeted and function-oriented engineering strategy by modifying specific bonds, trap energetics, and amorphous-network stability, which can further improve V_{th} stability, retention, and state distinguishability; however, dopant selection should also consider practical constraints such as toxicity, process compatibility, and cost. Since both compositional optimization and doping inevitably involve trade-offs among memory window, leakage current, endurance, and switching uniformity, material design alone is unlikely to simultaneously optimize all key metrics. Post-treatment offers an additional defect-conditioning route after film deposition, improving switching uniformity and retention without changing the original device stack, although excessive treatment may damage the amorphous network. Pulse-scheme engineering shifts the optimization from material design to operation control, allowing programmed threshold states to be stabilized or separated through tailored voltage waveforms, but this benefit may be accompanied by increased peripheral-circuit complexity and leakage-related trade-offs. Structural innovation provides a device-level route to relax the intrinsic limitations of homogeneous single-layer SOM devices by spatially decoupling memory formation, selector switching, and defect regulation, although this strategy may also increase fabrication and structural complexity. Therefore, the future development of high-performance SOM devices should be regarded as a multi-factor optimization problem, in which device performance, material selection, process complexity, cost, and manufacturing compatibility need to be balanced in an integrated manner.

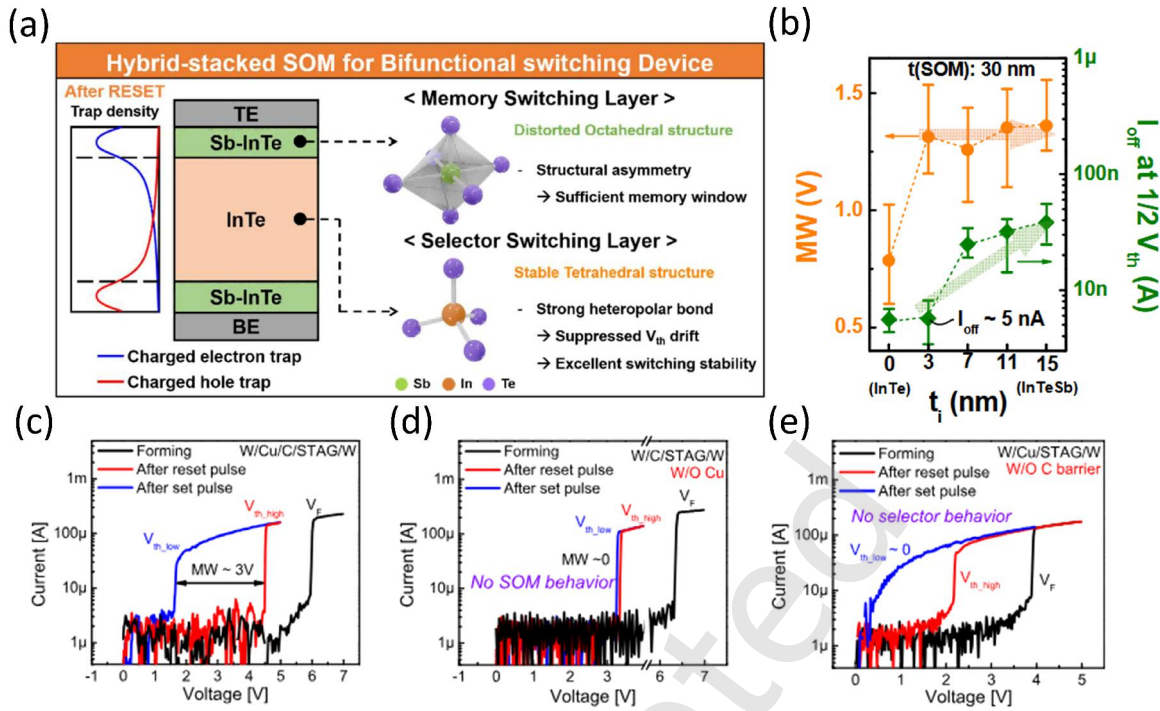


Figure 8. (a) Schematic of the hybrid-stacked SOM structure. Sb-InTe and InTe serve as memory and selector layers, respectively. (b) I_{off} (green) and memory window (orange) of the hybrid SOM devices as a function of the interlayer thickness (t_i). The total SOM thickness was fixed at 30 nm for all devices. (a,b) Reproduced with permission from Ref. [99], © IEEE 2025. Typical AC I-V characteristics under three different conditions for Cu-based SiTeAsGe (STAG). (c) W/Cu/C/STAG/W device with both Cu and a C barrier, (d) W/C/STAG/W device, (e) W/Cu/STAG/W device with Cu but without a C barrier. (c-e) Reproduced with permission from Ref. [122], © IEEE 2025.

3.2 Materials Selection and Reliability Modeling

For SOM, materials evaluation requires more than conventional selector-oriented criteria. In addition to threshold-switching performance, it is necessary to assess whether a material can support stable polarity-dependent threshold states and maintain them during repeated operation. Extensive efforts have been devoted to identifying chalcogenide compositions that satisfy the requirements for high-performance OTS operation and to understanding these requirements from a theoretical perspective [123–125]. However, it remains challenging to establish quantitative metrics that directly reflect polarity-dependent stability, including field-direction-dependent defect occupation, asymmetric electronic-state response under opposite bias, and the coupling between electronic excitation, structural relaxation, and memory window formation.

Recent studies have begun to extend first-principles-based screening frameworks toward SOM-oriented materials discovery. In the work of Sung et al. [35], the memory window was modeled on

the basis of a charged-defect-induced space charge region under a non-uniform electric field, which was further converted into a barrier factor governing the increase in activation energy during read operation. This treatment enabled ΔV_{th} to be evaluated within a materials-screening framework, rather than being considered only at the empirical device level. By combining bonding characteristics, thermal stability, electrical properties, memory window formation, and V_{th} drift into a unified screening workflow, ultimately identifying 18 promising Se-based candidates from 3888 ternary amorphous chalcogenide compositions. The screening outcome was further summarized through a five-dimensional performance map, in which thermodynamic stability, glass transition temperature (T_g), off-state current (I_{OFF}), ΔV_{th} , and V_{th} drift were simultaneously compared for the candidate materials (Figure 9). This visualization highlights the multidimensional trade-offs involved in SOM materials design, where electrical performance, thermal robustness, and reliability must be balanced simultaneously.

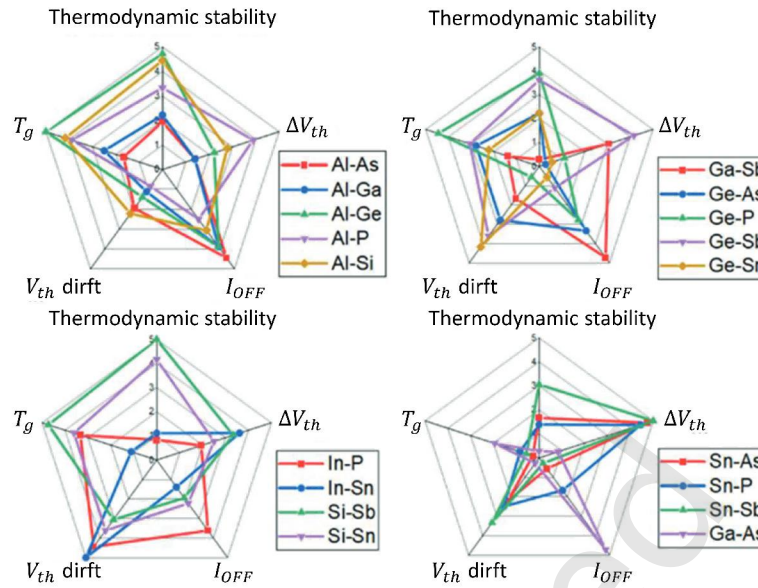


Figure 9. SOM performance comparison for candidate materials. For the 18 screened Se-based compositions, the pentagon diagram were plotted from the worst (score: 0) to the best (score: 5) for each property. Reproduced with permission from Ref. [35], © IEEE 2024.

Reliability modeling is equally important for SOM, especially in view of endurance degradation during repeated programming and readout. Unlike conventional selectors, in which endurance failure is mainly evaluated in terms of switching degradation or catastrophic breakdown, SOM endurance is directly coupled to the stability of polarity-encoded threshold states. Sung et al. [126] developed the Ab-initio Informed Multi-scale Endurance Modeling for SOM (AIMES) framework, which links electrothermal evolution, atomic diffusion, compositional relaxation, and device-level electrical degradation across multiple scales (**Figure 10a–e**).

In this framework, repetitive pulse operation is first translated into local electrothermal stress through finite-element simulation of the device structure. The resulting temperature field is then used in ab-initio molecular dynamics (AIMD) to extract the temperature-dependent diffusivity of the constituent species. These diffusivities are subsequently introduced into a drift-diffusion model, in which repeated electric-field cycling progressively generates an axial composition gradient inside the active layer, while interfacial mass loss is described through an out-diffusion boundary condition. The obtained cycle-dependent composition profile is not treated as a single averaged quantity, but is further converted into spatially resolved electronic-structure descriptors by assigning composition-dependent band-gap (E_g) and trap-density (N_T) values to each local

region, thereby generating $E_g(Z)$ and $N_T(Z)$ maps across the device. These position-dependent material parameters are then implemented in TCAD simulations, which self-consistently solve the electrical response of the non-uniform device and reproduce the evolution of the I–V characteristics, $V_{th,set}$, $V_{th,reset}$ and the memory window with cycling. In this way, endurance is predicted from the cycle at which the simulated threshold-state separation collapses below the readable margin. The model further shows that out-diffusion-induced band-gap narrowing affects the RESET state more strongly than the SET state because the former follows a classical Poole–Frenkel conduction that is more sensitive to activation-energy variations, thereby explaining the asymmetric collapse of the memory window during late-stage degradation.

This framework highlights amorphous-network rigidity as an important factor governing endurance degradation, thereby helping to rationalize reliability improvements achieved through compositional tuning and targeted doping, offering a physics-based route for predicting SOM endurance and guiding reliability-oriented materials optimization. Looking forward, more efficient SOM-oriented methodological frameworks can be developed by integrating first-principles calculations with machine-learning-assisted approaches, thereby enabling more predictive materials design, deepening the mechanistic understanding of SOM, and extending atomistic insights to the mesoscale and device-relevant length scales.

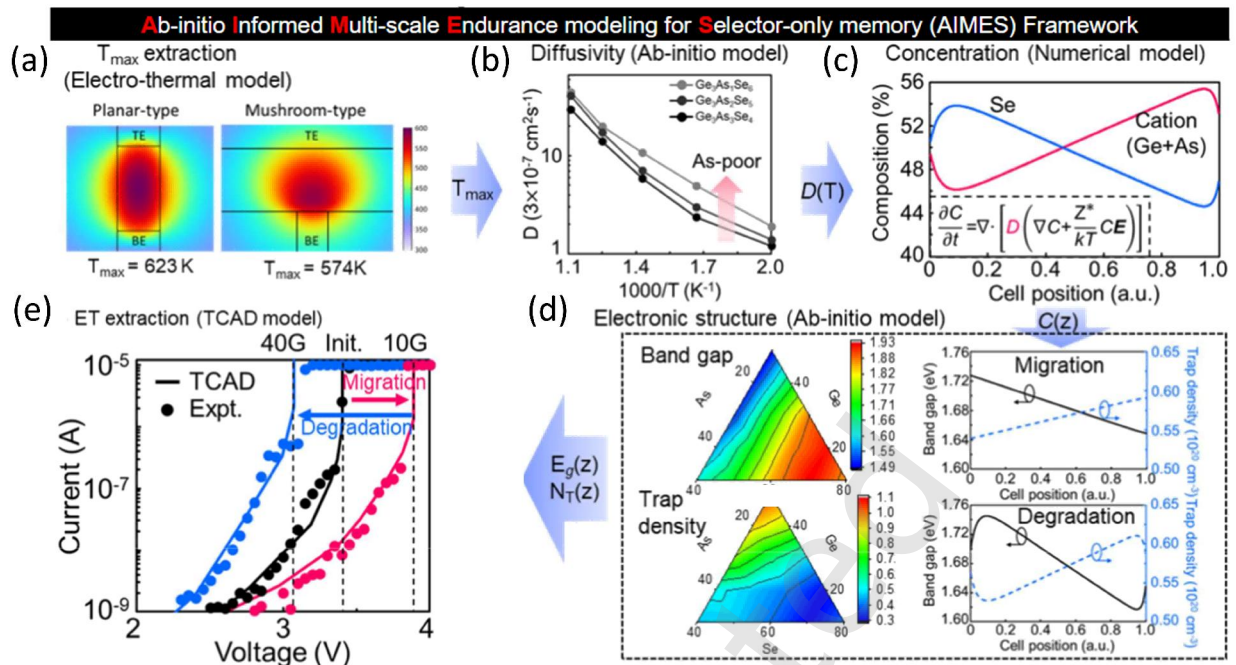


Figure 10. AIMES Framework: Coupled electro-thermal, atomistic, numerical and TCAD modeling scheme that qualitatively reproduces the endurance-induced shift of the V_{th} . (a) Spatial temperature maps obtained from electro-thermal simulations for planar-type and mushroom-type. (b) Diffusivity curves for three amorphous Ge-As-Se alloys derived from AIMD trajectories. (c) Drift-diffusion calculation that converts the temperature-dependent diffusivity into a steady-state compositional gradient $C(z)$ generated by repetitive electric-field cycling. (d) Electronic structure response to the $C(z)$ profile, obtained from firstprinciples density-of-states sampling. (e) I-V characteristics simulated with TCAD. (a-e) Reproduced with permission from Ref. [126], © IEEE 2025.

4 Integration and Industrial Demonstrations of SOM

The transition of SOM from a materials concept to a practical memory technology depends critically on its integrability, scalability, and reliability at the array and system levels. Beyond its device-level functionality, the industrial interest in SOM is largely driven by its potential to overcome the scaling limitations of conventional chalcogenide cross-point memories based on PCM-selector stacks. As highlighted by SK hynix in its 20 nm 4-deck 256 Gb cross-point memory study [13], although PCM-based cross-point memory can achieve high-density integration through advanced process optimization, its continued scaling is increasingly constrained by shrinking write-program margins, the high aspect ratio of the 1S1R stack, thermal disturbance associated with PCM melting, and endurance degradation related to PCM failure. In this context, SOM, which employs only two electrodes and a single dual-functional material (DFM), offers a structurally simpler and potentially more scalable alternative by reducing aspect ratio, easing self-aligned etching and related integration processes, and eliminating PCM-induced thermal disturbance.

Representative integrated SOM demonstrations from several companies are summarized in **Figure 11**. At the 20 nm technology node, SK hynix [18] showed that selector-only concepts can support reliable cross-point array operation while significantly reducing write current and eliminating the thermal disturbance associated with phase-change switching. The simplified stack structure also alleviated lithography and etching challenges at advanced nodes, consistent with the broader industrial motivation for replacing the more complex PCM-based 1S1R architecture.

Micron Technology subsequently demonstrated a 20 nm half-pitch, 256 Gb, four-deck single-chalcogenide Xpoint memory, together with further scaling toward the 1x-nm regime, highlighting the substantial structural simplification and scaling potential[127]. IBM and Macronix subsequently fabricated a 30 nm GeSe SOM array [91], further demonstrating the integrability of SOM materials in practical array structures. Samsung Electronics then demonstrated SOM operation in a 64 Gb array at the 16 nm node [32], indicating the scalability of the concept toward high-density integration. SK hynix reported the first fully integrated 16 nm half-pitch SOM [31], highlighting the potential of SOM for data-centric computing systems. These studies collectively confirmed stable read-window margins, low operating current, and promising endurance under practically relevant operating conditions. SK hynix further demonstrated, for the first time, a 16 nm half-pitch SOM with a two-deck architecture [95], marking an important step toward vertical integration and higher storage density. Samsung Electronics [96] advanced SOM scaling through simultaneous lateral shrinkage and vertical stacking. They reported the first fully integrated 14 nm 2-stack SOM with a 1 Gb main cell array while maintaining robust read-window margins and acceptable endurance characteristics. More recently, Samsung Electronics further improved the reliability of fully integrated 14 nm SOM, achieving more than 10^8 write cycles [128].

Taken together, these industrial demonstrations mark clear progress toward advanced-node scaling and vertically integrated SOM architectures. More broadly, they reinforce the potential of SOM as a structurally simplified and integration-friendly route for extending chalcogenide memory technologies beyond the practical scaling limits of PCM-based cross-point memory.

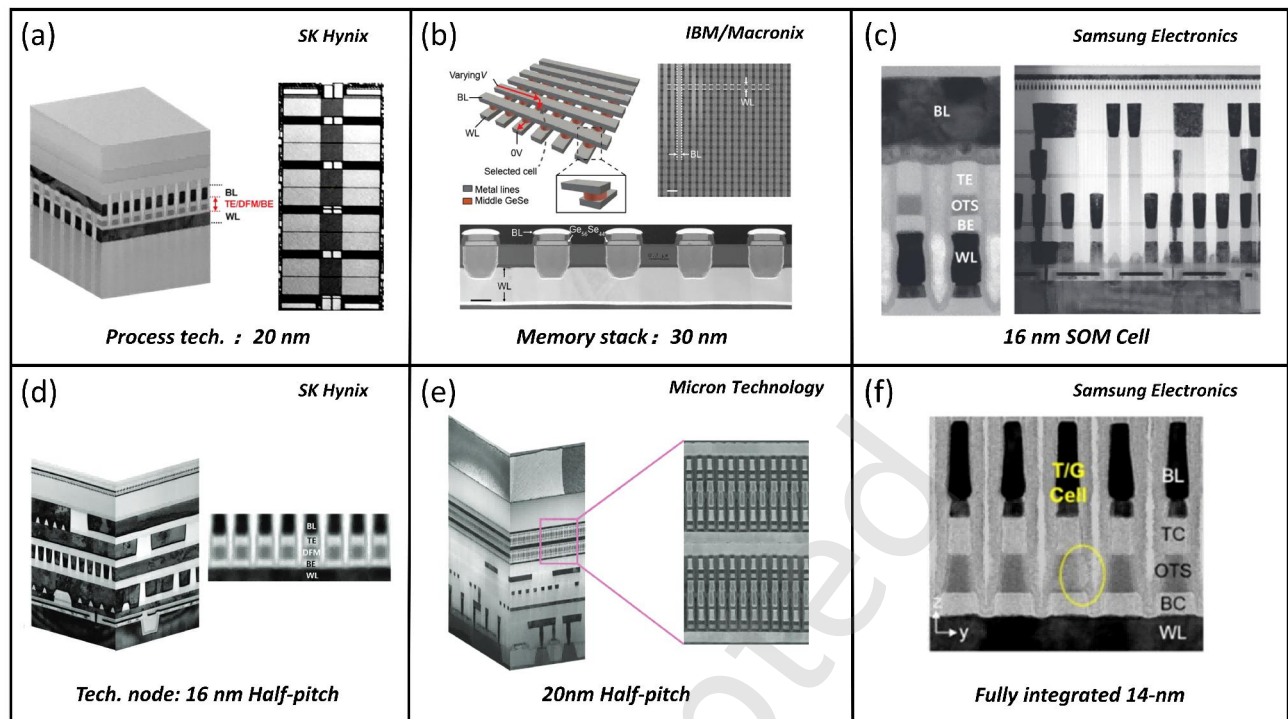


Figure 11. (a) Cross sectional TEM of SOM cell array and 8-Mats SEM of 32 Mb SOM, demonstrated by SK Hynix in 2022. Reproduced with permission from Ref. [18], © IEEE 2022. (b) Prototype of the GeSe SOM cross-point array, demonstrated by IBM/Macronix in 2024. Reproduced with permission from Ref. [91], © Springer Nature 2024. (c) Cross-sectional TEM image of 16 nm SOM cell (left) and the entire device of 64 Gb SOM (right), demonstrated by Samsung Electronics in 2023. Reproduced with permission from Ref. [32], © IEEE 2023. (d) Cross-sectional TEM image of 16 nm half-pitch cross-point SOM with SOM cell array, demonstrated by SK Hynix in 2024. Reproduced with permission from Ref. [31], © IEEE 2024. (e) Cross-sectional TEM image of a 20 nm half-pitch 256Gb SOM with 4-deck array architecture, demonstrated by Micron Technology in 2023. Reproduced with permission from Ref. [127], © IEEE 2023. (f) Cross-sectional TEM Image of the 14 nm OTS cells, demonstrated by Samsung Electronics in 2026. Reproduced with permission from Ref. [128], © IEEE 2026.

5 Challenges

SOM has advanced rapidly in recent years, yet several fundamental challenges still hinder its development into a mature and practically deployable memory technology. One of the most critical issues is that its physical mechanism remains insufficiently unified. Although threshold switching and polarity-dependent V_{th} modulation have been discussed from multiple perspectives, the microscopic origin and identification of the relevant defect states, the detailed nature of defect evolution, the local structural changes associated with programming, and the nonvolatile retention of the programmed threshold states are still not fully understood. At present, mechanistic studies of SOM rely mainly on experiments and first-principles calculations. However, experiments can't directly resolve the relevant microscopic evolution, whereas conventional DFT is typically restricted to relatively small structural models because of its computational cost. Moreover, it is difficult for DFT to capture the full process of defect relaxation and field-driven structural evolution at quasi-device-relevant length scales. Machine-learning interatomic potentials may offer a promising route for extending SOM studies to large-scale structural models on quasi-device-relevant scales.

Recent advances in machine-learning-based molecular dynamics provide a promising route to overcome the intrinsic spatial and temporal limitations of AIMD simulations[129–132]. Machine-learning interatomic potentials trained on first-principles data have enabled large-scale and long-time atomistic simulations of PCMs while maintaining near-first-principles accuracy, facilitating the investigation of amorphization, crystallization, and structural evolution[133–136]. Similar approaches could be extended to SOM

materials to explore threshold-switching-related structural dynamics over experimentally relevant length and time scales. In particular, machine-learning-based simulations may enable statistical identification of switching-related local structural motifs, investigation of thermally or electrically induced atomic rearrangements, and efficient screening of candidate SOM materials. For electrically driven switching, however, further developments that explicitly incorporate electric-field effects, charge redistribution, or electronic degrees of freedom may be required. When combined with first-principles calculations and experimental validation, such approaches could provide a powerful framework for establishing quantitative structure–property relationships and accelerating the rational design of SOM materials.

However, at such scales, the accuracy of the structural-evolution models themselves becomes a critical issue, particularly for amorphous materials[137]. For example, structurally inaccurate models may introduce spurious gap states in amorphous GeSe [138]. Besides, deep-learning density functional theory Hamiltonian (DeepH) [139] offers an attractive strategy toward scalable electronic-structure analysis by learning the mapping from material structure to the DFT Hamiltonian. Such a framework is particularly valuable because it provides a feasible route for identifying defects and electronic states in large-scale models beyond the practical scale of conventional DFT. Nevertheless, because SOM materials are typically amorphous, the quantitative applicability of DeepH to such structurally disordered systems still requires further systematic validation. Therefore, representative amorphous SOM structures and corresponding DFT benchmarks are still needed to evaluate its accuracy in describing defect-related electronic states in amorphous active layers.

Another major challenge is to achieve a sufficiently large memory window together with tight V_{th} distributions, stable retention, good endurance, and acceptable variability in device level. In SOM, these metrics are strongly coupled rather than independently tunable, because both selector and memory functions are integrated into the same amorphous layer. Thus, improving one aspect often comes at the expense of another, making it difficult to establish a balanced operating regime. Therefore, the discovery of novel materials that simultaneously provide large memory windows and high stability remains a key question for future SOM development. A further challenge is the lack of predictive SOM-oriented materials design principles. Existing materials-screening frameworks are not sufficient, because the mechanistic understanding of SOM remains limited, as discussed above. Therefore, further theoretical and data-driven modeling frameworks are required to more explicitly capture the structure-property relations governing SOM behavior. In this context, AI-driven materials screening and design could provide an important paradigm for accelerating SOM material discovery. By combining experimental datasets, first-principles calculations, machine-learning models, such approaches may help predict high-performance material compositions and identify composition-structure-property relationships that are difficult to obtain through trial-and-error experiments alone, as exemplified by the AIMES framework discussed in Section 3.2. This paradigm could provide a useful route for connecting microscopic material descriptors with practical SOM performance metrics. Materials selection for SOM implementation is also constrained by practical integration requirements. Even if a material exhibits promising SOM characteristics at the device level, it may not necessarily be an optimal choice for practical implementation, because materials selection must also consider factors such as toxicity, cost and process compatibility. In addition, although SOM offers clear integration-related advantages, translating these benefits into practical VXP-type remains challenging. Their realization still requires careful control over film uniformity, interface stability, process-induced structural damage or compositional deviation, while maintaining compatibility with CMOS integration flows, especially for advanced-node and vertically stacked architectures. Therefore, future SOM development must address not only intrinsic device performance, but also broader challenges associated with integration, architecture-level implementation, and manufacturing compatibility.

6 Conclusion

SOM has emerged as a promising memory concept by integrating selector and storage functions into a single active material, thereby enabling a 1S0R architecture with potential advantages in structural simplicity, scalability, and low operating current. In this review, recent developments of SOM have been reviewed from several key aspects, including the physical understanding of threshold switching and polarity-dependent memory formation, experimental approaches for performance and reliability improvement, computational and modeling frameworks for materials selection and device optimization, and recent progress in array integration and industrial demonstrations. Together, these advances highlight the growing potential of SOM as an emerging high-density memory technology. With continued progress in resolving challenges related to both mechanistic understanding and device performance, SOM is expected to further advance toward practical high-density memory and AI applications.

Acknowledgements

This work was supported by the National Science and Technology Major Project (Grant No. 2022ZD0117600), the National Natural Science Foundation of China (Grants No.

12274172, 12274180, 12504075), the Science and Technology Development Plan Project of Changchun, China (Grant No. 2024GZZ07).

Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

References

- [1] Bourzac, K. Fixing AI's energy crisis. *Nature* 2024, d41586-024-03408-z.
- [2] Sebastian, A.; Le Gallo, M.; Khaddam-Aljameh, R.; Eleftheriou, E. Memory devices and applications for in-memory computing. *Nat. Nanotechnol.* 2020, 15, 529–544.
- [3] Xu, M.; Wang, S.; He, Y.; Li, Y.; Zhang, W.; Yang, M.; Qi, X.; Wang, Z.; Xu, M.; Shang, D.; et al. Efficient modeling of ionic and electronic interactions by a resistive memory-based reservoir graph neural network. *Nat Comput Sci* 2025, 5, 1178–1191.
- [4] Le Gallo, M.; Sebastian, A. An overview of phase-change memory device physics. *J. Phys. D: Appl. Phys.* 2020, 53, 213002.
- [5] Huang, Z.; Wang, C.; Shi, W.; Wu, S.; He, Y.; Li, Y.; Zhang, C.; Chen, H. Review of optical pre-sensor computing. *Photonix Synergy* 2026, 1, 7.
- [6] Zheng, J.; Wang, H.; Zhang, Y.; Li, G.; Lu, S.; Lei, L.; Li, H.; Wang, L.; Hao, Z.; Xiong, B. A review and outlook on optical edge intelligent computing. *Photonix Synergy* 2026, 1, 2.
- [7] Ban, S.; Lee, J.; Seo, Y.; Lee, W.; Kim, T.; Hwang, H. Advances in Ovonic Threshold Switch Selector Technologies for Storage Class Memory: From Fundamentals to Development and Beyond. *Adv Elect Materials* 2025, 11, 2400665.
- [8] Wu, H.; Wang, X. H.; Gao, B.; Deng, N.; Lu, Z.; Haukness, B.; Bronner, G.; Qian, H. Resistive Random Access Memory for Future Information Processing System. *Proc. IEEE* 2017, 105, 1770–1789.
- [9] DerChang Kau; Tang, S.; Karpov, I. V.; Dodge, R.; Klehn, B.; Kalb, J. A.; Strand, J.; Diaz, A.; Leung, N.; Wu, J.; et al. A stackable cross point Phase Change Memory. In *2009 IEEE International Electron Devices Meeting (IEDM)*, Baltimore, MD, USA, 2009, pp 1–4.
- [10] Yu, S.; Chen, P.-Y. Emerging Memory Technologies: Recent Trends and Prospects. *IEEE Solid-State Circuits Mag.* 2016, 8, 43–56.
- [11] Lanza, M.; Sebastian, A.; Lu, W. D.; Le Gallo, M.; Chang, M.-F.; Akinwande, D.; Puglisi, F. M.; Alshareef, H. N.; Liu, M.; Roldan, J. B. Memristive technologies for data storage, computation, encryption, and radio-frequency communication. *Science* 2022, 376, eabj9979.
- [12] Fazio, A. Advanced Technology and Systems of Cross Point Memory. In *2020 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2020, pp 24.1.1–24.1.4.
- [13] Yi, J.; Kim, M.; Seo, J.; Park, N.; Lee, S.; Kim, J.; Do, G.; Jang, H.; Koo, H.; Cho, S.; et al. The chalcogenide-based memory technology continues: beyond 20nm 4-deck 256Gb cross-point memory. In *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, 2023, pp 1–2.
- [14] Yi-Chou Chen; Chen, C. F.; Chen, C. T.; Yu, J. Y.; Wu, S.; Lung, S. L.; Liu, R.; Chih-Yuan Lu. An access-transistor-free (0T/1R) non-volatile resistance random access memory (RRAM) using a novel threshold switching, self-rectifying chalcogenide device. In *IEEE International Electron Devices Meeting 2003*, Washington, DC, USA, 2003, pp 37.4.1–37.4.4.
- [15] Kabuyanagi, S.; Garbin, D.; Fantini, A.; Clima, S.; Degraeve, R.; Donadio, G. L.; Devulder, W.; Delhougne, R.; Cellier, D.; Cockburn, A.; et al. Understanding of Tunable Selector Performance in Si-Ge-As-Se OTS Devices by Extended Percolation Cluster Model Considering Operation Scheme and Material Design. In *2020 IEEE Symposium on VLSI Technology*, Honolulu, HI, USA, 2020, pp 1–2.
- [16] Ravsher, T.; Garbin, D.; Fantini, A.; Degraeve, R.; Clima, S.; Donadio, G. L.; Kundu, S.; Hody, H.; Devulder, W.; Van Houdt, J.; et al. Self-Rectifying Memory Cell Based on SiGeAsSe Ovonic Threshold Switch. *IEEE Trans. Electron Devices* 2023, 70, 2276–2281.
- [17] Ban, S.; Choi, H.; Lee, W.; Hong, S.; Zang, H.; Lee, B.; Kim, M.; Lee, S.; Lee, H.; Kim, T. Pulse Dependent Threshold Voltage Variation of the Ovonic Threshold Switch in Cross-Point Memory. *IEEE Electron Device Lett.* 2020, 41, 373–376.
- [18] Hong, S.; Choi, H.; Park, J.; Bae, Y.; Kim, K.; Lee, W.; Lee, S.; Lee, H.; Cho, S.; Ahn, J.; et al. Extremely high performance, high density 20nm self-selecting cross-point memory for Compute Express Link. In *2022 International Electron Devices Meeting (IEDM)*, San Francisco,

- CA, USA, 2022, pp 18.6.1-18.6.4.
- [19] Haratipour, N.; Chang, S.-C.; Shivaraman, S.; Neumann, C.; Liao, Y.-C.; Alpizar, B. G.; Tung, I.-C.; Li, H.; Kumar, V.; Doyle, B.; et al. Hafnia-Based FeRAM: A Path Toward Ultra-High Density for Next-Generation High-Speed Embedded Memory. In *2022 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2022, pp 6.7.1-6.7.4.
- [20] Cheng, H. Y.; Grun, A.; Chien, W. C.; Yeh, C. W.; Ray, A.; Cheng, C. W.; Lai, E. K.; Lavoie, C.; Gignac, L.; Hopstaken, M.; et al. New Phase-Change Materials by Atomic-Level Engineering the Dopants for Extremely Low V_{th} Drift at 85 °C and High Endurance 3D Crosspoint Memory: IBM/Macronix PCRAM Joint Project. In *2022 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2022, pp 18.5.1-18.5.4.
- [21] Arnaud, F.; Zuliani, P.; Reynard, J. P.; Gandolfo, A.; Disegni, F.; Mattavelli, P.; Gomiero, E.; Samanni, G.; Jahan, C.; Berthelon, R.; et al. Truly Innovative 28nm FDSOI Technology for Automotive Micro-Controller Applications embedding 16MB Phase Change Memory. In *2018 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, 2018, pp 18.4.1-18.4.4.
- [22] Park, S.-O.; Hong, S.; Sung, S.-J.; Kim, D.; Seo, S.; Jeong, H.; Park, T.; Cho, W. J.; Kim, J.; Choi, S. Phase-change memory via a phase-changeable self-confined nano-filament. *Nature* 2024, 628, 293–298.
- [23] Lee, M.-J.; Lee, C. B.; Lee, D.; Lee, S. R.; Chang, M.; Hur, J. H.; Kim, Y.-B.; Kim, C.-J.; Seo, D. H.; Seo, S.; et al. A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta₂O₅-x/TaO₂-x bilayer structures. *Nature Mater* 2011, 10, 625–630.
- [24] Hayakawa, Y.; Himeno, A.; Yasuhara, R.; Boullart, W.; Vecchio, E.; Vandeweyer, T.; Witters, T.; Crotti, D.; Jurczak, M.; Fujii, S.; et al. Highly reliable TaOx ReRAM with centralized filament for 28-nm embedded application. In *2015 Symposium on VLSI Circuits (VLSI Circuits)*, Kyoto, Japan, 2015, pp T14–T15.
- [25] Aratani, K.; Ohba, K.; Mizuguchi, T.; Yasuda, S.; Shiimoto, T.; Tushima, T.; Sone, T.; Endo, K.; Kouchiyama, A.; Sasaki, S.; et al. A Novel Resistance Memory with High Scalability and Nanosecond Switching. In *2007 IEEE International Electron Devices Meeting*, Washington, DC, 2007, pp 783–786.
- [26] Huang, Y.-C.; Liu, S.-H.; Chen, H.-S.; Feng, H.-C.; Li, C.-F.; Yang, C.-Y.; Chang, W.-K.; Yang, C.-F.; Wu, C.-Y.; Lin, Y.-C.; et al. 15.7 A 32Mb RRAM in a 12nm FinFet Technology with a 0.0249μm² Bit-Cell, a 3.2GB/S Read Throughput, a 10KCycle Write Endurance and a 10-Year Retention at 105°C. In *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2024, pp 288–290.
- [27] Boujamaa, E. M.; Ali, S. M.; Wandji, S. N.; Gourio, A.; Pyo, S.; Koh, G.; Song, Y.; Song, T.; Kye, J.; Vial, J. C.; et al. A 14.7Mb/mm² 28nm FDSOI STT-MRAM with Current Starved Read Path, 52Q/Sigma Offset Voltage Sense Amplifier and Fully Trimmable CTAT Reference. In *2020 IEEE Symposium on VLSI Circuits*, Honolulu, HI, USA, 2020, pp 1–2.
- [28] Golonzka, O.; Alzate, J.-G.; Arslan, U.; Bohr, M.; Bai, P.; Brockman, J.; Buford, B.; Connor, C.; Das, N.; Doyle, B.; et al. MRAM as Embedded Non-Volatile Memory Solution for 22FFL FinFET Technology. In *2018 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, 2018, pp 18.1.1-18.1.4.
- [29] Lee, T. Y.; Lee, J. M.; Kim, M. K.; Oh, J. S.; Lee, J. W.; Jeong, H. M.; Jang, P. H.; Joo, M. K.; Suh, K.; Han, S. H.; et al. World-most energy-efficient MRAM technology for non-volatile RAM applications. In *2022 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2022, pp 10.7.1-10.7.4.
- [30] Lee, P.-H.; Lee, C.-F.; Shih, Y.-C.; Lin, H.-J.; Chang, Y.-A.; Lu, C.-H.; Chen, Y.-L.; Lo, C.-P.; Chen, C.-C.; Kuo, C.-H.; et al. 33.1 A 16nm 32Mb Embedded STT-MRAM with a 6ns Read-Access Time, a 1M-Cycle Write Endurance, 20-Year Retention at 150°C and MTJ-OTP Solutions for Magnetic Immunity. In *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp 494–496.
- [31] Kim, M.; Bae, Y.; Park, J.; Yeon, J.; Shim, H.; Jin, S.; Kim, H.; Oh, S.; Do, G.; Yun, D.; et al. First Demonstration of Fully Integrated 16 nm Half-Pitch Selector Only Memory (SOM) for Emerging CXL Memory. In *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2024, pp 1–2.
- [32] Park, I.-M.; Lee, K. W.; Park, J.-H.; Song, S. J.; Kim, T. Y.; Wu, Z.; Lee, W. J.; Choi, B. D.; Jeong, Y. J.; Oh, S. C.; et al. Enhanced Endurance Characteristics in High Performance 16nm Selector Only Memory (SOM). In *2023 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2023, pp 1–4.
- [33] Zhao, J.; Sun, Y.; Ren, K.; Ravsher, T.; Garbin, D.; Clima, S.; Zhu, M. Chalcogenide Selector-Only Memory. *Materials Today* 2026, 98, 103429.
- [34] Ravsher, T.; Degraeve, R.; Garbin, D.; Fantini, A.; Clima, S.; Donadio, G. L.; Kundu, S.; Hody, H.; Devulder, W.; Van Houdt, J.; et al. Polarity-dependent threshold voltage shift in ovonic threshold switches: Challenges and opportunities. In *2021 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2021, pp 28.4.1-28.4.4.
- [35] Sung, H.-J.; Choi, M.; Kang, Y.; Yang, K.; Koo, B.; Zhe, W.; Chae, H.; Lee, C. S. Ab-Initio Screening of Amorphous Chalcogenides for Selector-Only Memory (SOM) through Electrical Properties and Device Reliability. In *2024 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2024, pp 1–4.
- [36] Warren, A. C. Reversible thermal breakdown as a switching mechanism in chalcogenide glasses. *IEEE Trans. Electron Devices* 1973, 20, 123–131.
- [37] Böer, K. W.; Ovshinsky, S. R. Electrothermal Initiation of an Electronic Switching Mechanism in Semiconducting Glasses. *Journal of Applied Physics* 1970, 41, 2675–2681.
- [38] Kroll, D. M. Theory of electrical instabilities of mixed electronic and thermal origin. *Phys. Rev. B* 1974, 9, 1669–1706.
- [39] Shaw, M. P. Thermal instability-The precursor to switching in inhomogeneous thin films. *IEEE Trans. Electron Devices* 1979, 26, 1766–1771.
- [40] Warren, A. C.; Male, J. C. Field-enhanced conductivity effects in thin chalcogenide-glass switches. *Electron. Lett. (UK)* 1970, 6, 567–569.
- [41] Kaplan, T.; Bullock, D. C.; Adler, D.; Epstein, D. J. Thermally Induced Negative Resistance in Si-Doped YIG. *Applied Physics Letters* 1972, 20, 439–441.
- [42] Kaplan, T.; Adler, D. Thermal Effects in Amorphous-Semiconductor Switching. *Applied Physics Letters* 1971, 19, 418–420.
- [43] Kaplan, T.; Adler, D. Electrothermal switching in amorphous semiconductors. *Journal of Non-Crystalline Solids* 1972, 8–10, 538–543.
- [44] Kroll, D. M. Theory of electrical instabilities of mixed electronic and thermal origin. *Phys. Rev. B* 1974, 9, 1669–1706.
- [45] Kroll, D. M. Theory of electrical instabilities of mixed electronic and thermal origin. II. Switching as a nucleation process. *Phys. Rev. B* 1975, 11, 3814–3821.
- [46] Adler, D.; Shur, M. S.; Silver, M.; Ovshinsky, S. R. Threshold switching in chalcogenide-glass thin films. *Journal of Applied Physics* 1980, 51, 3289–3309.
- [47] Le Gallo, M.; Athmanathan, A.; Krebs, D.; Sebastian, A. Evidence for thermally assisted threshold switching behavior in nanoscale phase-change memory cells. *Journal of Applied Physics* 2016, 119, 025704.
- [48] Chen, N.; Wang, B.; Niu, M.; Sun, H.; Zhang, S.; Li, X. Intensive Structural Disorder Induces Electronic Delocalization: Amorphous Solid - Liquid Transition in Ovonic Threshold Switching Materials. *Adv Funct Materials* 2024, 34, 2410622.
- [49] Lee, J.; Seo, Y.; Ban, S.; Kim, D. G.; Park, Y. B.; Lee, T. H.; Hwang, H. Understanding Switching Mechanism of Selector-Only Memory Using Se-Based Ovonic Threshold Switch Device. *IEEE Trans. Electron Devices* 2024, 71, 3351–3357.
- [50] Karpov, V. G.; Kryukov, Y. A.; Savransky, S. D.; Karpov, I. V. Nucleation switching in phase change memory. *Applied Physics Letters* 2007, 90, 123504.
- [51] Karpov, V. G.; Kryukov, Y. A.; Karpov, I. V.; Mitra, M. Field-induced nucleation in phase change memory. *Phys. Rev. B* 2008, 78, 052201.
- [52] Nardone, M.; Karpov, V. G.; Jackson, D. C. S.; Karpov, I. V. A unified model of nucleation switching. *Applied Physics Letters* 2009, 94, 103509.
- [53] Lee, S.; Yoo, J.; Park, J.; Hwang, H. Field-induced nucleation switching in binary ovonic threshold switches. *Applied Physics Letters* 2019, 115, 233503.
- [54] Li, H.; Chen, W. First-principles prediction of the native filament/dielectric interfaces for the possible filamentary switching mechanism in chalcogenide selector devices. *Journal of Applied Physics* 2020, 127, 045105.
- [55] Ielmini, D.; Zhang, Y. Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices. *Journal of Applied Physics* 2007, 102, 054517.
- [56] Ielmini, D. Threshold switching mechanism by high-field energy gain in the hopping transport of chalcogenide glasses. *Phys. Rev. B* 2008, 78, 035308.
- [57] Noé, P.; Verdy, A.; d'Acapito, F.; Dory, J.-B.; Bernard, M.; Navarro, G.; Jager, J.-B.; Gaudin, J.; Raty, J.-Y. Toward ultimate nonvolatile resistive memories: The mechanism behind ovonic threshold switching revealed. *Sci. Adv.* 2020, 6, eaay2830.
- [58] Buscemi, F.; Piccinini, E.; Vandelli, L.; Nardi, F.; Padovani, A.;

- Kaczer, B.; Garbin, D.; Clima, S.; Degraeve, R.; Kar, G. S.; et al. A HydroDynamic Model for Trap-Assisted Tunneling Conduction in Ovonic Devices. *IEEE Trans. Electron Devices* 2023, 70, 1808–1814.
- [59] Emin, D. Current-driven threshold switching of a small polaron semiconductor to a metastable conductor. *Phys. Rev. B* 2006, 74, 035206.
- [60] Ding, H.-R.; Zhao, T.-Y.; Chen, N.-K.; Wang, B.-Q.; Qin, S.-Y.; Niu, M.; Wang, S.-B.; Huang, Y.-T.; Xu, M.; Li, X.-B. Polaron-Induced Midgap States in Ovonic Threshold Switching Material for 3D Phase-Change Memory Applications. *J. Phys. Chem. Lett.* 2026, 17, 2213–2221.
- [61] Li, H.; Robertson, J. Materials Selection and Mechanism of Non-linear Conduction in Chalcogenide Selector Devices. *Sci Rep* 2019, 9, 1867.
- [62] Guo, Y.; Li, H.; Zhang, W.; Robertson, J. Structural changes during the switching transition of chalcogenide selector devices. *Applied Physics Letters* 2019, 115, 163503.
- [63] Raty, J.-Y.; Noé, P. Ovonic Threshold Switching in Se - Rich $\text{Ge}_x\text{Se}_{1-x}$ Glasses from an Atomistic Point of View: The Crucial Role of the Metavalent Bonding Mechanism. *Physica Rapid Research Ltrs* 2020, 14, 1900581.
- [64] Jia, S.; Li, H.; Gotoh, T.; Longeaud, C.; Zhang, B.; Lyu, J.; Lv, S.; Zhu, M.; Song, Z.; Liu, Q.; et al. Ultrahigh drive current and large selectivity in GeS selector. *Nat Commun* 2020, 11, 4636.
- [65] Nardone, M.; Simon, M.; Karpov, I. V.; Karpov, V. G. Electrical conduction in chalcogenide glasses of phase change memory. *Journal of Applied Physics* 2012, 112, 071101.
- [66] Zhao, Z.; Clima, S.; Garbin, D.; Degraeve, R.; Pourtois, G.; Song, Z.; Zhu, M. Chalcogenide Ovonic Threshold Switching Selector. *Nano-Micro Lett.* 2024, 16, 81.
- [67] Fantini, P.; Ghetti, A.; Varesi, E.; Pirovano, A.; Pellizzer, F.; Baratella, D.; Ribaldone, C.; Caravati, S.; Campi, D.; Bernasconi, M.; et al. Microscopic model of the operation of the single-chalcogenide X-point memory. *Commun Mater* 2026, 7, 26.
- [68] Fantini, P.; Polino, N.; Ghetti, A.; Ielmini, D. Threshold Switching by Bipolar Avalanche Multiplication in Ovonic Chalcogenide Glasses. *Adv Elect Materials* 2023, 9, 2300037.
- [69] Mott, N. F. Conduction in non-crystalline systems: VII. Non-ohmic behaviour and switching. *Philosophical Magazine* 1971, 24, 911–934.
- [70] Henisch, H. K.; Fagen, E. A.; Ovshinsky, S. R. A qualitative theory of electrical switching processes in monostable amorphous structures. *Journal of Non-Crystalline Solids* 1970, 4, 538–547.
- [71] Fantini, P.; Pirovano, A.; Ventrice, D.; Redaelli, A. Experimental investigation of transport properties in chalcogenide materials through $1/f$ noise measurements. *Applied Physics Letters* 2006, 88, 263506.
- [72] Pirovano, A.; Lacaita, A. L.; Benvenuti, A.; Pellizzer, F.; Bez, R. Electronic Switching in Phase-Change Memories. *IEEE Trans. Electron Devices* 2004, 51, 452–459.
- [73] Redaelli, A.; Pirovano, A.; Benvenuti, A.; Lacaita, A. L. Threshold switching and phase transition numerical models for phase change memory simulations. *Journal of Applied Physics* 2008, 103, 111101.
- [74] Pirovano, A.; Lacaita, A. L.; Merlani, D.; Benvenuti, A.; Pellizzer, F.; Bez, R. Electronic switching effect in phase-change memory cells. In *Digest. International Electron Devices Meeting.*, San Francisco, CA, USA, 2002, pp 923–926.
- [75] Sun, Y.; Gotoh, T.; Zhao, J.; Zhang, M.; Shi, S.; Zhang, H.; Liu, Z.; Shen, J.; Dronskowski, R.; Song, Z.; et al. Charge-triggered switching mechanism in selenium selector enabling ultralow leakage current. *Nat. Mater.* 2026, 25, 651–658.
- [76] Degraeve, R.; Ravsher, T.; Kabuyanagi, S.; Fantini, A.; Clima, S.; Garbin, D.; Kar, G. S. Modeling and spectroscopy of ovonic threshold switching defects. In *2021 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, 2021, pp 1–5.
- [77] Clima, S.; Govoreanu, B.; Opsomer, K.; Velea, A.; Avasarala, N. S.; Devulder, W.; Shlyakhov, I.; Donadio, G. L.; Witters, T.; Kundu, S.; et al. Atomistic investigation of the electronic structure, thermal properties and conduction defects in Ge-rich GexSe_{1-x} materials for selector applications. In *2017 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, 2017, pp 4.1.1–4.1.4.
- [78] Ambrosi, E.; Wu, C. H.; Lee, H. Y.; Chang, P. C.; Hsu, C. F.; Lee, C. M.; Chang, C. C.; Chen, Y. Y.; Heh, D. W.; Hou, D. H.; et al. Low variability high endurance and low voltage arsenic-free selectors based on GeCTe . In *2021 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2021, pp 28.5.1–28.5.4.
- [79] Lee, J.; Ban, S.; Lee, T. H.; Hwang, H. Defect Engineering of BTe Ovonic Threshold Switch (OTS) With Nitrogen Doping for Improved Electrical and Reliability Performance. *IEEE Electron Device Lett.* 2023, 44, 1468–1471.
- [80] Ban, S.; Lee, J.; Kim, T.; Hwang, H. Simple Binary In-Te OTS with Sub-nm HfO_x Buffer Layer for 3D Vertical X-point Memory Applications. In *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, 2023, pp 1–2.
- [81] Tikhomirov, V. K.; Elliott, S. R. Model for photoinduced anisotropy and its dark relaxation in chalcogenide glasses. *Phys. Rev. B* 1995, 51, 5538–5541.
- [82] Ravsher, T.; Degraeve, R.; Garbin, D.; Clima, S.; Fantini, A.; Donadio, G.; Kundu, S.; Devulder, W.; Hody, H.; Potoms, G.; et al. Comprehensive Performance and Reliability Assessment of Se-based Selector-Only Memory. In *2024 IEEE International Reliability Physics Symposium (IRPS)*, Grapevine, TX, USA, 2024, pp 7A.5-1–7A.5-9.
- [83] Ielmini, D.; Zhang, Y. Evidence for trap-limited transport in the subthreshold conduction regime of chalcogenide glasses. *Applied Physics Letters* 2007, 90, 192102.
- [84] Sung, H.; Choi, M.; Wu, Z.; Chae, H.; Heo, S.; Kang, Y.; Koo, B.; Park, J.; Yang, W.; Park, Y.; et al. Microscopic Origin of Polarity - Dependent V_{TH} Shift in Amorphous Chalcogenides for 3D Self - Selecting Memory. *Advanced Science* 2024, 11, 2408028.
- [85] Clima, S.; Ducry, F.; Garbin, D.; Ravsher, T.; Degraeve, R.; Belmonte, A.; Kar, G. S.; Pourtois, G. Selector Only Memory: Exploring Atomic Mechanisms from First-Principles. In *2024 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2024, pp 1–4.
- [86] Wang, Y.; Song, W.; Song, S.; Xin, T.; Cheng, Y.; Song, Z. Atomic migration enables multilevel states in Sb_2Se_3 -based selector-only memory. *Device* 2026, 4, 101077.
- [87] Ravsher, T.; Garbin, D.; Fantini, A.; Degraeve, R.; Clima, S.; Donadio, G. L.; Kundu, S.; Hody, H.; Devulder, W.; Potoms, G.; et al. Evidence of Heat - Assisted Atomic Migration in GeSe Self - Selecting Memory at High Operating Current Density. *Physica Rapid Research Ltrs* 2024, 2300415.
- [88] Fantini, P.; Ghetti, A.; Varesi, E.; Pirovano, A.; Pellizzer, F.; Baratella, D.; Ribaldone, C.; Caravati, S.; Campi, D.; Bernasconi, M.; et al. Microscopic model of the operation of the single-chalcogenide X-point memory. *Commun Mater* 2026, 7, 26.
- [89] Lee, J.; Seo, Y.; Ban, S.; Kim, D.; Heo, S.; Kang, D.; Hwang, H. Enhancing Se-based Selector-only Memory with Ultra-fast Write Speed (~ 10 ns) and Superior Retention Characteristics (> 10 years at RT) via Material Design and UV Treatment Engineering. In *2023 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2023, pp 1–4.
- [90] Chien, W. C.; Zheng, J. X.; Yeh, C. W.; Gignac, L. M.; Cheng, H. Y.; Liu, Z. L.; Grun, A.; Sung, C. L.; Lai, E. K.; Cheng, S.; et al. A Novel Chalcogenide Based CuGeSe Selector Only Memory (SOM) for 3D Xpoint and 3D Vertical Memory Applications. In *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2024, pp 1–2.
- [91] Liu, Z.-L.; Grun, A.; Chien, W.-C.; Ray, A.; Lai, E.-K.; Kuo, I.-T.; Gignac, L.; Lavoie, C.; BrightSky, M.; Lung, H.-L.; et al. A GexSe $_{1-x}$ switch-only-memory technology through polarized atomic distribution. *Sci Rep* 2024, 14, 22115.
- [92] Seo, Y.; Ban, S.; Lee, J.; Kim, D.; Jung, L.; Hwang, H. Enhancing Selector-Only Memory Reliability Through Multi-Step Write Pulse. *IEEE Electron Device Lett.* 2024, 45, 2383–2386.
- [93] Jeong, W. H.; Jung, J.; Jeong, J.-S.; Yang, M. K.; Kim, G. H. In-doped GeSbSeTe thin films for increased memory window of selector-only-memory devices. *Journal of Alloys and Compounds* 2025, 1031, 181079.
- [94] Wen, J.; Yi, C.; Chen, J.; Wang, L.; Liu, Z.; Chen, Z.; Tong, H.; Miao, X. Write Endurance Enhanced and Large Memory Window of GeSe-Based Selector-Only Memory With Indium Doping Scheme. *IEEE Electron Device Lett.* 2025, 46, 115–118.
- [95] Ban, S.; Kim, M.; Park, N.; Park, J.; Yeon, J.; Yun, D.; Park, T.; Oh, S.; Lee, B.; Lee, W.; et al. Achieving Outstanding Endurance ($>10^7$) in Large-Array Two-Deck 16 Nm SOM Through Process, Structure, and Design Strategies for Emerging SCM Applications. In *2025 Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, 2025, pp 1–3.
- [96] Park, J. H.; Lee, C. H.; Park, W. H.; Park, K. D.; Song, S. J.; Eun, S. H.; Park, Y. J.; Lee, K. W.; Park, I. M.; Wu, Z.; et al. Scalable Fabrication and Demonstration of the First Fully Integrated 14nm 2-Stack SOM (Selector Only Memory) Device. In *2025 Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, 2025, pp 1–3.
- [97] Seo, Y.; Kim, D.; Jung, L.; Lee, J.; Kwon, O.; Baek, C.; Park, Y. B.; Lee, T. H.; Hwang, H. Multi-Stack InTe Selector-Only Memory (SOM) Achieving Ultra-Low Power Operation (10 μA) and Excellent

- Endurance ($\sim 10^{10}$ cycles). In *2025 Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, 2025, pp 1–3.
- [98] Zhang, Y.; Wen, J.; Yi, C.; Wang, L.; Liu, Z.; Chen, Z.; Tong, H.; Miao, X. High-Threshold-Stability GeSe-Based Selector-Only Memory Enabled by Gallium Doping. *IEEE Electron Device Lett.* 2025, 46, 1765–1768.
- [99] Lee, J.; Seo, Y.; Kwon, O.; Jung, L.; Hwang, H. Hybrid-Stacked Sb-based Selector-Only Memory with Large Memory Window (> 1.3 V) and Excellent Endurance ($> 10^{10}$) via Decoupled Memory and Selector Functions. In *2025 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2025, pp 1–4.
- [100] Joo, J. M.; Choi, J. Y.; Kim, D. H.; Oh, J. S.; Kang, M. S.; Park, J. E.; Yuk, S. H.; Kim, T. G. Improved reliability of Si-doped GeSb-based selector-only memory via homopolar bond suppression and enhanced memory window. *Journal of Materials Science & Technology* 2026, 256, 193–202.
- [101] Mun, Y. Y.; Yang, M. K.; Kim, G. H. Composition-dependent electrical characteristics of GeSeTe-based selector-only memory device. *Applied Surface Science* 2026, 722, 165576.
- [102] Jung, J.; Jeong, W. H.; Yang, M. K.; Kim, G. H. Compositional engineering for oxidation-induced drift suppression in GeSbSeTe-based selector-only memory devices. *Applied Surface Science* 2026, 733, 166616.
- [103] Wang, Y.; Yan, Y.; Fu, Q.; Wang, H.; Tong, H.; Xu, M.; Miao, X. Large Memory Window and Low Drift of In-Te-Based Selector-Only Memory Enabled by Silicon Doping. *IEEE Electron Device Lett.* 2026, 1–1.
- [104] Jeong, W. H.; Lee, S. H.; Kim, G. H. Effect of Indium Doping on the Reliability Characteristics of Chalcogenide GeSbSeTe Thin-Film-Based Selector-Only Memory Devices. *ACS Appl. Mater. Interfaces* 2025, 17, 68123–68135.
- [105] Seo, H. K.; Jung, J.; Jeong, J.-S.; Park, M. H.; Kim, G. H.; Yang, M. K. Sn-Doped selector-only memory with stable threshold voltage margin for robust binary neural network inference. *Adv Compos Hybrid Mater* 2026, 9, 116.
- [106] Lee, J.; Kim, S.; Lee, S.; Ban, S.; Heo, S.; Lee, D.; Mosendz, O.; Hwang, H. Improving the SiGeAsTe Ovonic Threshold Switching (OTS) Characteristics by Microwave Annealing for Excellent Endurance ($> 10^{11}$) and Low Drift Characteristics. In *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2022, pp 320–321.
- [107] Seo, Y.; Lee, J.; Ban, S.; Kim, D.; Han, G.; Hwang, H. Improving the selector characteristics of ovonic threshold switch via UV treatment process. *Applied Physics Letters* 2023, 123, 242103.
- [108] Choi, M.; Sung, H.; Koo, B.; Park, J.; Yang, W.; Kang, Y.; Park, Y.; Ham, Y.; Yun, D.; Ahn, D.; et al. Mechanism for Local - Atomic Structure Changes in Chalcogenide - based Threshold - Switching Devices. *Advanced Science* 2024, 11, 2404035.
- [109] Jung, L.; Lee, J.; Seo, Y.; Hwang, H. Achieving 3-bit Operation in Selector-only-memory by Controlling Variability with Microwave Annealing and Bipolar Pulse Scheme. In *2024 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2024, pp 1–4.
- [110] Cheng, H. Y.; Chien, W. C.; Kuo, I. T.; Yeh, C. W.; Gignac, L.; Kim, W.; Lai, E. K.; Lin, Y. F.; Bruce, R. L.; Lavoie, C.; et al. Ultra-High Endurance and Low IOFF Selector based on AsSeGe Chalcogenides for Wide Memory Window 3D Stackable Crosspoint Memory. In *2018 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, 2018, pp 37.3.1–37.3.4.
- [111] Tverjanovich, A.; Cuisset, A.; Fontanari, D.; Bychkov, E. Structure of Se-Te glasses by Raman spectroscopy and DFT modeling. *J Am Ceram Soc* 2018, 101, 5188–5197.
- [112] Ravsher, T.; Garbin, D.; Fantini, A.; Degraeve, R.; Clima, S.; Donadio, G. L.; Kundu, S.; Hody, H.; Devulder, W.; Van Houdt, J.; et al. Polarity - Induced Threshold Voltage Shift in Ovonic Threshold Switching Chalcogenides and the Impact of Material Composition. *Physica Rapid Research Ltrs* 2023, 17, 2200417.
- [113] Ravsher, T.; Garbin, D.; Fantini, A.; Degraeve, R.; Clima, S.; Donadio, G.; Kundu, S.; Hody, H.; Devulder, W.; Van Houdt, J.; et al. Enhanced performance and low-power capability of SiGeAsSe-GeSbTe 1S1R phase-change memory operated in bipolar mode. In *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2022, pp 312–313.
- [114] Ban, S.; Lee, J.; Seo, Y.; Kwon, O.; Lee, W.; Kim, T.; Hwang, H. Subthreshold Bias-Induced Threshold Voltage Shift of the Ovonic Threshold Switch. *IEEE Electron Device Lett.* 2024, 45, 128–131.
- [115] Chen, Z.; Wang, L.; Wen, J.; Tong, H.; Miao, X. Controllable Threshold Voltage (V_{th}) Drift in Ovonic Threshold Switch Devices Under a High-Frequency Continuous Operation. *IEEE Trans. Electron Devices* 2022, 69, 3158–3162.
- [116] Kim, D.; Jang, J. T.; Kim, C.; Kim, H. W.; Hong, E.; Ban, S.; Shin, M.; Lee, H.; Lee, H. D.; Mo, H.-S.; et al. Read Disturbance in Cross-Point Phase-Change Memory Arrays—Part II: Array Simulations Considering External Currents. *IEEE Trans. Electron Devices* 2023, 70, 521–526.
- [117] Yamaguchi, M.; Degraeve, R.; Garbin, D.; Clima, S.; Ravsher, T.; Matsubayashi, D.; Tsukamoto, T.; Delhougne, R.; Goux, L.; Kar, G. S. Understanding the Cycling-Dependent Threshold Voltage Instability in OTS Devices. In *2022 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2022, pp 5.1.1–5.1.4.
- [118] Effects of RESET Current Overshoot and Resistance State on Reliability of RRAM. *IEEE Electron Device Lett.* 2014, 35, 636–638.
- [119] Lee, J.; Ravsher, T.; Garbin, D.; Clima, S.; Degraeve, R.; Belmonte, A.; Hwang, H.; Lee, I. Optimizing Pulse Conditions for Enhanced Memory Performance of Se-Based Selector-Only Memory. *IEEE J. Electron Devices Soc.* 2025, 13, 362–365.
- [120] Song, J. H.; Yang, M. K.; Kim, G. H. GeSbSeTe-based selector-only-memory via unipolar operation. *Journal of Materials Science & Technology* 2026, 250, 175–187.
- [121] Seo, H. K.; Jeong, W. H.; Jung, J.; Park, M. H.; Kim, G. H.; Yang, M. K. Selector-only-memory device using chalcogenide thin film in a 4k crossbar array. *Materials Science and Engineering: R: Reports* 2026, 168, 101169.
- [122] Lee, S.; Jung, L.; Heo, S.; Hwang, H. Enabling Memory Window in Ovonic Threshold Switch Devices Through Cu-Based Trap for Selector-Only Memory Operation. *IEEE Electron Device Lett.* 2025, 46, 753–756.
- [123] Clima, S.; Matsubayashi, D.; Ravsher, T.; Garbin, D.; Delhougne, R.; Kar, G. S.; Pourtois, G. First-principles screening for sustainable OTS materials. *Solid-State Electronics* 2024, 214, 108876.
- [124] Read, J. C.; Stewart, D. A.; Reiner, J. W.; Terris, B. D. Evaluating Ovonic Threshold Switching Materials with Topological Constraint Theory. *ACS Appl. Mater. Interfaces* 2021, 13, 37398–37411.
- [125] Xu, M.; Xu, M.; Miao, X. Deep machine learning unravels the structural origin of mid-gap states in chalcogenide glass for high-density memory integration. *InfoMat* 2022, 4, e12315.
- [126] Sung, H.-J.; Chae, H.; Choi, M.; Park, J.-B.; Koo, B.; Lee, J.; Park, S.; Cheon, S.; Yang, Y.; Kang, Y.; et al. Ab-initio Informed Multi-scale Endurance Modeling for Selector-Only Memory (AIMES). In *2025 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2025, pp 1–4.
- [127] Pellizzer, F.; Pirovano, A.; Bez, R.; Meyer, R. L. Status and Perspectives of Chalcogenide-based CrossPoint Memories. In *2023 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2023, pp 1–4.
- [128] Song, Y. S.; Park, K. D.; Lee, W.; Lee, K.; Yang, H. M.; Koo, B. J.; Jang, G.; Lee, C. H.; Park, W. H.; Park, J. H.; et al. Decoupling Dual Degradation Pathways in OTS Endurance for High-Reliability Selector-Only Memory. In *2026 IEEE/JSAP Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2026, pp 1–3.
- [129] Abou El Kheir, O.; Bonati, L.; Parrinello, M.; Bernasconi, M. Unraveling the crystallization kinetics of the Ge₂Sb₂Te₅ phase change compound with a machine-learned interatomic potential. *npj Computational Materials* 2024, 10, 33.
- [130] Drautz, R. Atomic cluster expansion for accurate and transferable interatomic potentials. *Phys. Rev. B* 2019, 99, 014104.
- [131] Zhou, Y.; Zhang, W.; Ma, E.; Deringer, V. L. Device-scale atomistic modelling of phase-change memory materials. *Nature Electronics* 2023, 6, 746–754.
- [132] Ying, P.; Qian, C.; Zhao, R.; Wang, Y.; Xu, K.; Ding, F.; Chen, S.; Fan, Z. Advances in modeling complex materials: The rise of neuroevolution potentials. *Chemical Physics Reviews* 2025, 6, 011310.
- [133] Wang, B.-Q.; Zhao, T.-Y.; Ding, H.-R.; Liu, Y.-T.; Chen, N.-K.; Niu, M.; Li, X.-D.; Xu, M.; Sun, H.-B.; Zhang, S.; et al. Partial melting nature of phase-change memory Ge-Sb-Te superlattice uncovered by large-scale machine learning interatomic potential molecular dynamics. *Acta Materialia* 2024, 276, 120123.
- [134] Zhou, Y.; Thomas du Toit, D. F.; Elliott, S. R.; Zhang, W.; Deringer, V. L. Full-cycle device-scale simulations of memory materials with a tailored atomic-cluster-expansion potential. *Nature Communications* 2025, 16, 8688.
- [135] Wang, B.; Li, K.; Zhang, W.; Sun, Y.; Zhou, J.; Sun, Z. Thermal Transport of GeTe/Sb₂Te₃ Superlattice by Large-Scale Molecular Dynamics with Machine-Learned Potential. *J. Phys. Chem. C* 2025,

- 129, 6386–6396.
- [136] Li, K.; Liu, B.; Zhou, J.; Sun, Z. Revealing the crystallization dynamics of Sb–Te phase change materials by large-scale simulations. *J. Mater. Chem. C* 2024, 12, 3897–3906.
- [137] Fragapane, N. L.; Deringer, V. L. Amorphous materials as a frontier challenge for universal interatomic potentials. 2026.
- [138] Moon, M.; Hwang, S.; Kim, J.; Park, Y.; Hong, C.; Han, S. Unveiling Defect Motifs in Amorphous GeSe Using Machine Learning Interatomic Potentials. *ACS Appl. Mater. Interfaces* 2025, 17, 57260–57272.
- [139] Li, H.; Wang, Z.; Zou, N.; Ye, M.; Xu, R.; Gong, X.; Duan, W.; Xu, Y. Deep-learning density functional theory Hamiltonian for efficient ab initio electronic-structure calculation. *Nat Comput Sci* 2022, 2, 367–377.

Just Accepted