

Scalable ultrafast non-volatile two-dimensional floating-gate memory arrays based on $\text{Y}_2\text{O}_3/\text{HfO}_2$ hybrid dielectrics

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Nano Res., **Just Accepted Manuscript** • <https://doi.org/10.26599/NR.2026.94909113>

<https://www.sciopen.com/journal/1998-0124> on Aug. 13, 2026

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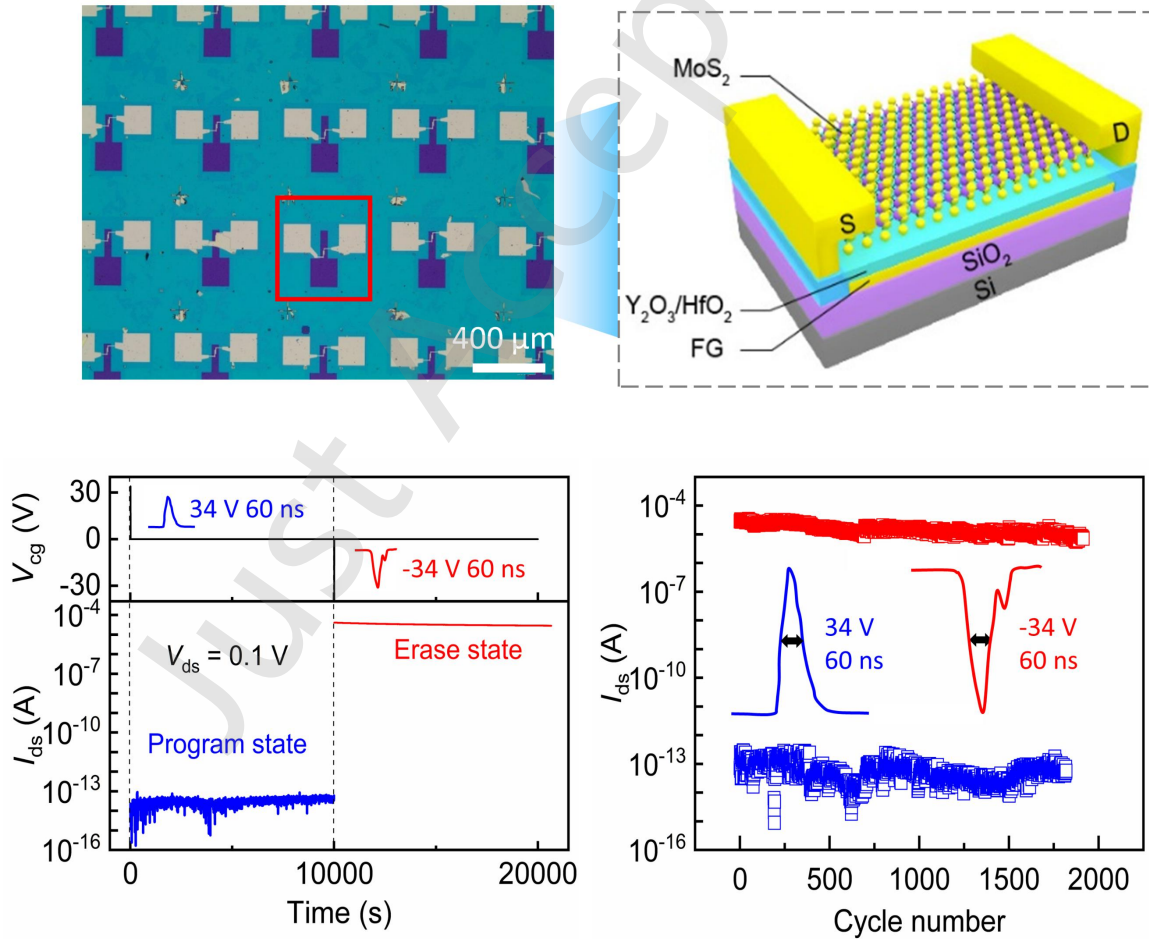
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A scalable non-volatile floating-gate memory array with hybrid $\text{Y}_2\text{O}_3/\text{HfO}_2$ dielectrics achieves ultrafast programming and erasing speeds of ~ 60 ns, high extinction ratios up to $\sim 10^9$, and long-term data retention. The devices also demonstrate efficient optical erasure capability with promising responsivity and detectivity, highlighting the potential of this fabrication approach for high-density storage and photodetection applications.

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Research Article

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Received: 24 June 2026; **Revised:** 23 July 2026; **Accepted:** 13 August 2026

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Cite this article: *Nano Research*, 2026, 19, 94909113 <https://doi.org/10.26599/NR.2026.94909113>

Abstract: The growing demands of artificial intelligence hardware have exposed a fundamental latency bottleneck in conventional floating-gate memory arrays. Although two-dimensional (2D) floating-gate memories have achieved nanosecond-level operations, their large-scale integration remains hindered by the scalability issues of the commonly used hBN dielectric layer. Here, we demonstrate scalable ultrafast non-volatile floating-gate memory arrays with hybrid $\text{Y}_2\text{O}_3/\text{HfO}_2$ dielectrics as the tunneling layer, achieving ~ 60 ns ultrafast programming/erasing speeds, high extinction ratios up to $\sim 10^9$, long-term data retention approaching 10^5 s, and robust cycling endurance exceeding 1800 cycles with multi-bit storage capabilities. A 5×5 memory array shows outstanding uniformity in memory window sizes, on/off ratios, and programmed/erased threshold voltages. Furthermore, the floating-gate memory devices also demonstrate efficient optical erasure with 1,441 A/W responsivity and 9×10^{16} Jones detectivity. The promising uniformity of these memory arrays highlights the potential for larger-scale integration and its scalability for high-density storage and photodetection applications.

Keywords: two-dimensional materials, floating-gate memory, ultrafast, high- κ dielectric, large-scale integration, optoelectronic memory

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Non-volatile memory serves as a fundamental pillar for the contemporary semiconductor industry and artificial intelligence applications.^[1,2] Floating-gate memory has historically dominated the flash market due to its high storage density, superior cell scalability, and reliable read/write endurance.^[3] Nevertheless, the persistent scaling of device footprints causes conventional structures to encounter critical bottlenecks, including low operational speeds^[4,5], limited data retention and endurance^[6,7], and insufficient extinction ratios^[3]. Such limitations impede the realization of high-density integrated arrays.

These performance degradations originate from the interfacial dangling bonds in silicon-based devices.^[8] Two-dimensional (2D) materials and their van der Waals (vdW) heterostructures offer inherently dangling-bond-free surfaces, enabling high-performance electronic^[9–14] and optoelectronic devices,^[15–17] memories,^[17–19] and integrated circuits.^[20–25] Indeed, floating-gate memories employing 2D materials have demonstrated ultrafast programming/erasing speeds (20 ns), high extinction ratios (up to 10^{10}) and extended data retention (> 10 years), alongside exceptional cycling endurance (10^5 to 10^6 cycles).^[26–29] Moreover, based on a hot-carrier-injection mechanism, graphene-channel flash memory achieved 400 ps programming and robust endurance over 5.5×10^6 cycles.^[19] While these promising device-level characteristics are often realized on exfoliated hBN, such an approach is incompatible with large-scale integration. Atomic layer deposition (ALD)-compatible high- κ oxides like HfO_2 and Al_2O_3 have become the standard choice for gate dielectrics and enabled large-area 2D memory arrays, but low programming/erasing speeds remain a challenge.^[23–25] Plasma pretreatment can achieve programming/erasing speeds of 20 ns^[30–33] but introduces secondary defects^[34] and more complex fabrication. Prior research indicates that incorporating a seed layer supplies adequate hydroxyl sites for the ALD growth of HfO_2 , thereby facilitating uniform deposition and minimizing interfacial defects.^[35–38]

In this work, we demonstrate a scalable approach to fabricating ultrafast non-volatile 2D floating-gate memory arrays using a seed-layer strategy. We achieve $\text{Y}_2\text{O}_3/\text{HfO}_2$ hybrid dielectric stacks with high-quality interfaces, as verified by cross-sectional aberration-corrected scanning transmission electron microscopy (STEM) imaging. The resulting devices deliver an on/off ratio of up to 10^9 , ultrafast operation speeds down to 60 ns, reliable retention of 10^5 s, endurance surpassing 1800 cycles, and tightly controlled threshold voltage distributions. A fabricated 5×5 array demonstrates excellent uniformity across key performance parameters. Moreover, the floating-gate memory device also demonstrates efficient optical erasure capability, with a responsivity of 1,441 A/W and a detectivity of

9×10^{16} Jones. These results delineate a highly effective pathway for the large-scale integration of ultrafast non-volatile 2D memory arrays.

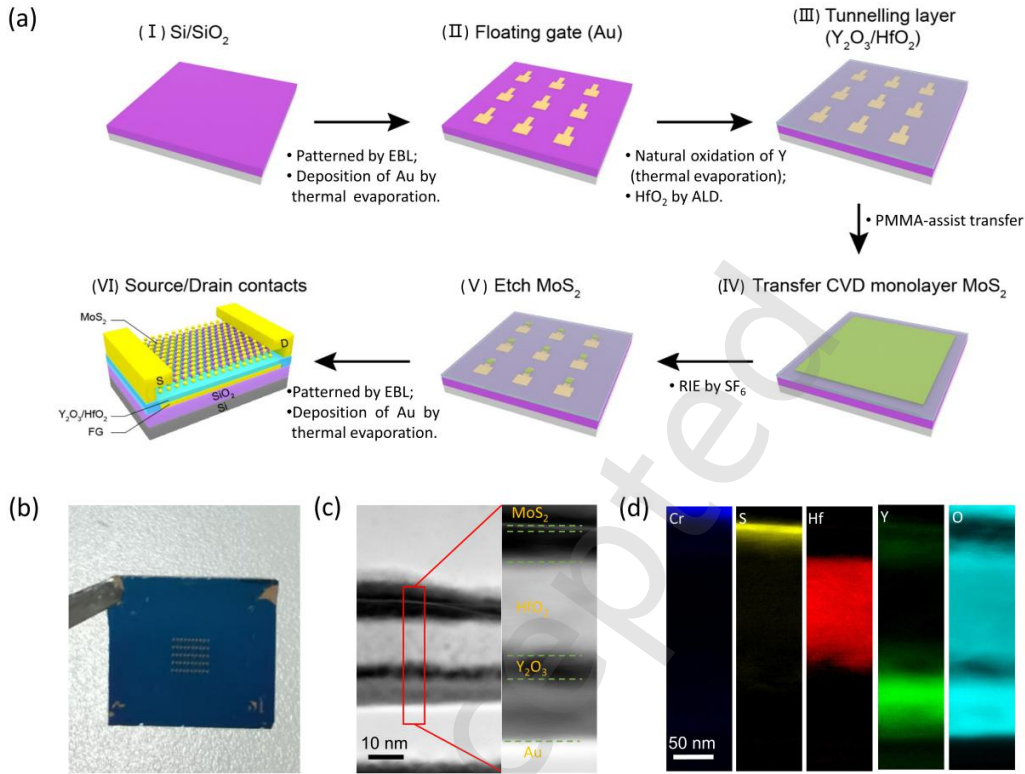


Figure 1. Fabrication and structure characterization of the floating-gate memory array based on Y₂O₃/HfO₂ hybrid dielectric layers. (a) Fabrication process flow of floating-gate memory array. (b) A photograph of the device array. (c) High-resolution HAADF-STEM (left) and magnified view of the region highlighted by the red rectangle (right) images taken at the different heterostructure interfaces, showing atomically sharp interfaces between each functional layers. (d) EELS elemental mapping revealing the uniform spatial distribution of chromium (Cr), sulfur (S), hafnium (Hf), yttrium (Y) and oxygen (O), respectively.

Figure 1a schematically illustrates the fabrication process of the floating-gate memory array based on a Y₂O₃/HfO₂ hybrid dielectric layer. The device employs a vertical stack of Si/SiO₂ (300 nm)/Au (10 nm)/Y₂O₃ (4 nm)/HfO₂ (12 nm)/MoS₂ layer, where Si, SiO₂, Au, Y₂O₃, HfO₂ and MoS₂ serve as the control gate, control-gate dielectric, floating gate, seed layer, tunnel barrier and channel, respectively. A first electron-beam lithography (EBL) defines floating-gate electrode patterns, followed by thermal evaporation of Cr (2 nm)/Au (10 nm) and lift-off. To address the capacitance mismatch, we designed $150 \times 150 \mu\text{m}^2$ capacitor pads, achieving a gate-coupling ratio (α) of $\sim 62.4\%$ (see Supplementary Note).^[26,28] Yttrium is deposited via thermal evaporation and then oxidized at room temperature for 12 hours to form 4-nm Y₂O₃ layer.^[35] This layer serves as a seed layer for the HfO₂ growth, and its

high- κ nature also enables it to function as part of the excellent hybrid dielectric layer. Subsequently, 12-nm HfO_2 is deposited through a low-temperature (110°C) ALD process for 100 cycles. Large-area CVD-grown^[39] MoS_2 is then transferred onto the hybrid dielectric using a water-assisted transfer technique^[40] and patterned into a 5×5 array with individual $20 \times 20 \mu\text{m}^2$ channels through SF_6 plasma etching.^[41] Source/drain electrodes (Cr (6 nm)/Au (60 nm)) are defined by thermal evaporation and lift-off, with an optical photograph of the completed array provided in Figure 1b. Cross-sectional high-angle annular dark-field (HAADF) STEM imaging (Figure 1c) demonstrates atomically sharp interfaces, while electron energy loss spectroscopy (EELS) mapping (Figure 1d) confirms the uniform spatial distribution of Cr, S, Hf, Y, and O atoms. Such low-defect interfaces are essential for high-performance and reliable device operation.^[42,43]

Atomic force microscopy (AFM) analysis gives an ultra-low root-mean-square roughness of ~ 468 pm for the $\text{Y}_2\text{O}_3/\text{HfO}_2$ hybrid dielectric (Figure S1a). Figure S1b presents the capacitance characteristics of a $100 \times 100 \mu\text{m}^2$ parallel-plate capacitor. By positioning the seed layer on a metallic substrate rather than directly on the 2D material, carrier doping and interfacial defect states are effectively minimized, as the strong Fermi-level pinning of the metal screens interfacial charges.^[44] Figure S2 presents the dual-sweep transfer characteristics of the transistor and the corresponding leakage current measurements. The stable and extremely low leakage current demonstrates the excellent insulating properties of the dielectric layer. Optical microscopy (Figure S3a) confirms the high coverage and good film uniformity across the growth substrate. Raman spectroscopy (Figure S3b) and transfer characteristics (Figure S4b) of the MoS_2 channel indicate a high-quality single layer characteristic.^[45-47]

Figure 2a shows a schematic of the floating-gate memory device with electrical connections. The dual-sweeping transfer curves (Figure 2b) exhibit a clear clockwise hysteresis. A substantial memory window emerges when the back-gate sweep voltage surpasses 10 V, and expands linearly with the maximum sweep voltage (Figure S5), confirming the precise control over the threshold electric field required for charge tunneling.^[48] The output characteristics are shown in Figure 2c. The output characteristic curve of the fresh state shows an on-state with symmetric current at a V_{ds} range of 0.2 V because of the initial doping of MoS_2 ,^[46] which also demonstrates a good ohmic contact at MoS_2 and Cr/Au interfaces. Under a programming pulse ($V_{\text{bg, pulse}}$ of +34 V, 60 ns), electrons tunnel from the source into the floating-gate layer and deplete the MoS_2 channel, leading to a low-current OFF-state. Under an erasing pulse ($V_{\text{bg, pulse}}$ of -34 V, 60 ns), holes tunnel into

the floating-gate layer and shift the MoS₂ into a high-current ON-state on the order of 10⁻⁵ A, achieving an on/off ratio of $\sim 10^9$.

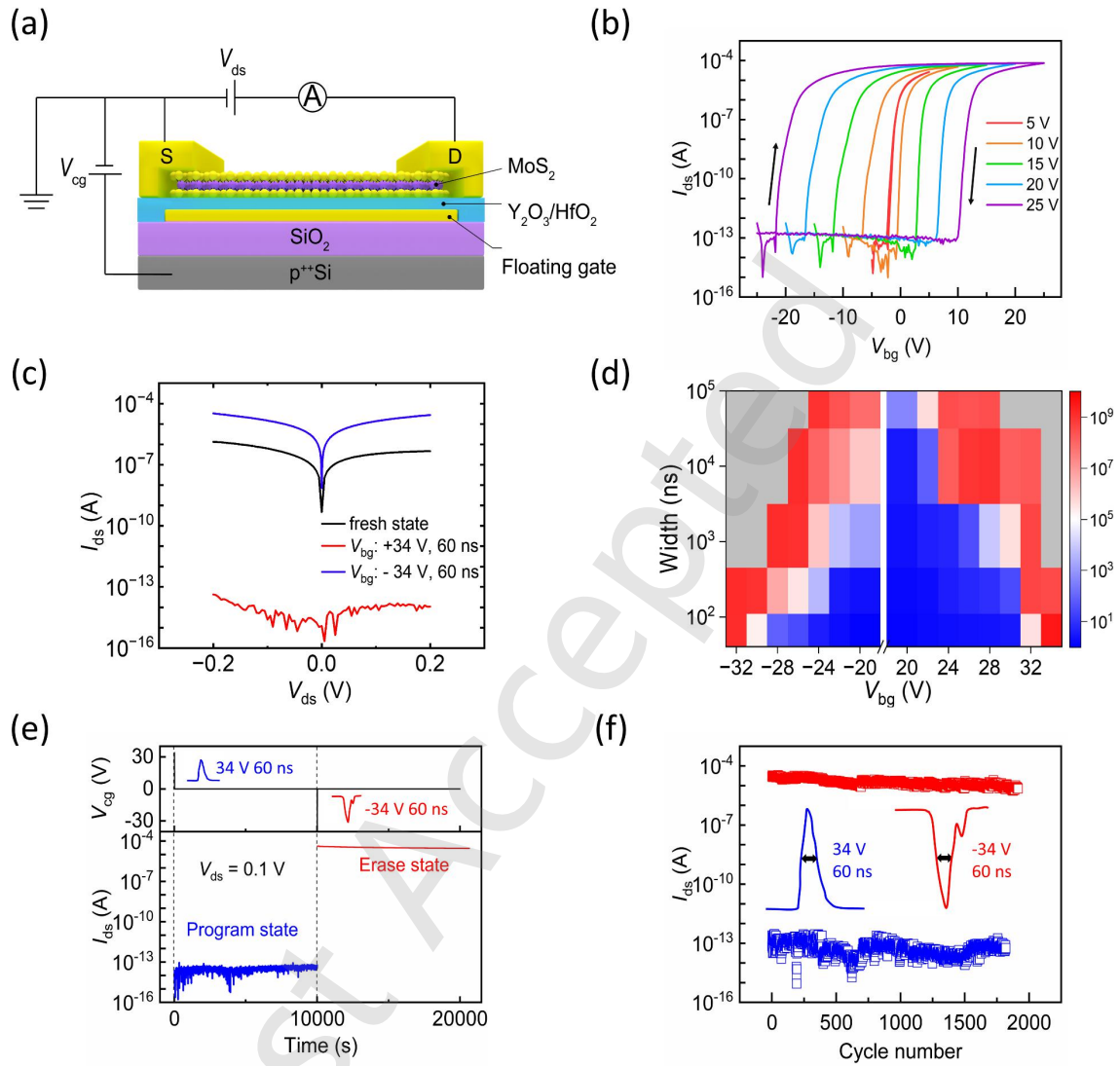


Figure 2. Static and dynamic characteristics of the floating-gate memory based on a Y₂O₃/HfO₂ hybrid dielectric. (a) Schematic of the floating-gate memory based on a Y₂O₃/HfO₂ hybrid dielectric. (b) Transfer characteristics of the device by sweeping the voltage applied on the back gate, exhibiting a large tunable memory window. (c) Output curves of the floating-gate memory under the programmed (blue line), erased (red line), and fresh (black line) states. (d) Extinction ratios obtained under different pulse conditions with varying amplitudes and widths. (e) Time-evolution of current states after the programming ($V_{bg} = +34$ V, 60 ns) and erasing ($V_{bg} = -34$ V, 60 ns) operations, demonstrating a switching ratio exceeding 10⁹. (f) Endurance performance of the memory device by alternating 60 ns width voltage pulse of $V_{bg} = \pm 34$ V, showing the robustness of the floating-gate memory.

Figure 2d shows the trade-off between pulse amplitude and width of a given on/off ratio.^[29] Figure 2e shows the time-evolution of current states after programming and erasing operations. Both states maintain a robust on/off ratio for over 10^4 s without notable degradation. Cyclic endurance testing with ± 34 V, 60 ns pulses (Figure 2f) shows no meaningful degradation after 1,800 cycles, maintaining a consistent on/off ratio of $\sim 10^8$.

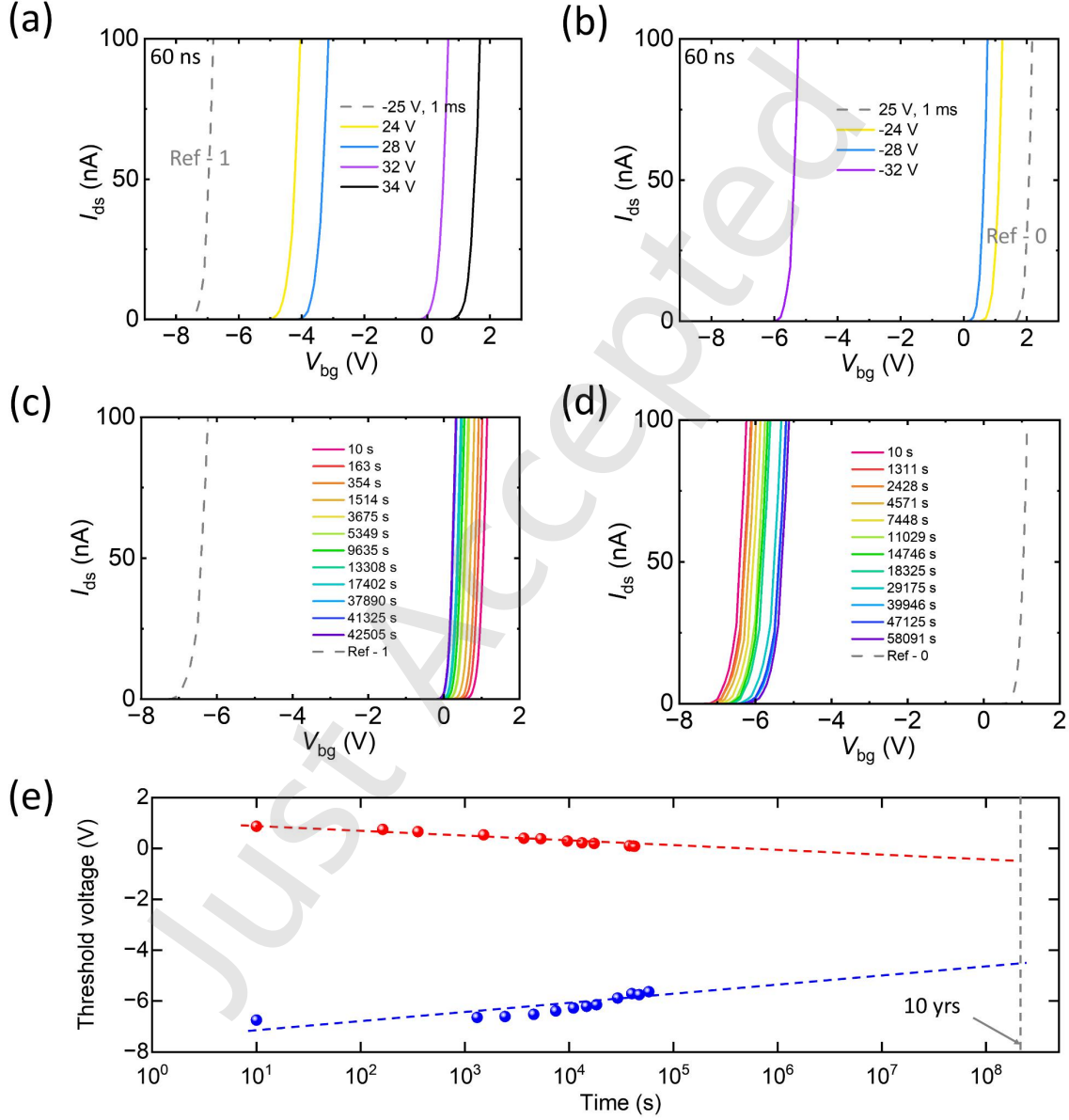


Figure 3. Threshold voltage shift of the floating-gate memory. (a) The transfer characteristics of the non-volatile memory. The original state-1 is achieved with a pulse of -25 V for 1 ms. By applying different positive pulses to program the memory to state-0, the device shows an obvious right shift in the threshold voltage. (b) The original state-0 was achieved with a pulse of $+25$ V for 1 ms. By applying different negative pulses to erase the memory to state-1, the device shows an obvious left shift in the threshold voltage. (c) Time-evolution of threshold voltage after applying a programming

pulse (+34 V, 60 ns). (d) Time-evolution of threshold voltage after applying an erase pulse (-34 V, 60 ns). (e) Threshold voltage trend of the storage state as a function of time, indicating it is feasible for the long-term data retention at room temperature.

We further characterized the threshold voltage shift under various programming and erasing pulses (Figure 3a-b). Programming pulses (60 ns) from 24 V to 34 V shift V_{th} positively by +2.66 V to +8.44 V, while erasing pulses (-24 V to -32 V; 60 ns width) induced negative V_{th} shifts of -0.99 V to -7.50 V. Figures 3c-e illustrates retention properties of the memory by tracking the evolution of V_{th} over time. V_{th} varies by only +0.8 V for the programmed state over 4.2×10^4 s and +1.1 V for the erased state over 5.8×10^4 s. Extrapolating this relationship suggests a V_{th} retention window persisting over 10 years. Figure S6 shows the evolution of the erased state V_{th} over 210,000 s with no discernible changes. The threshold voltage trends under varying pulse parameters are shown in Figure S7-10.

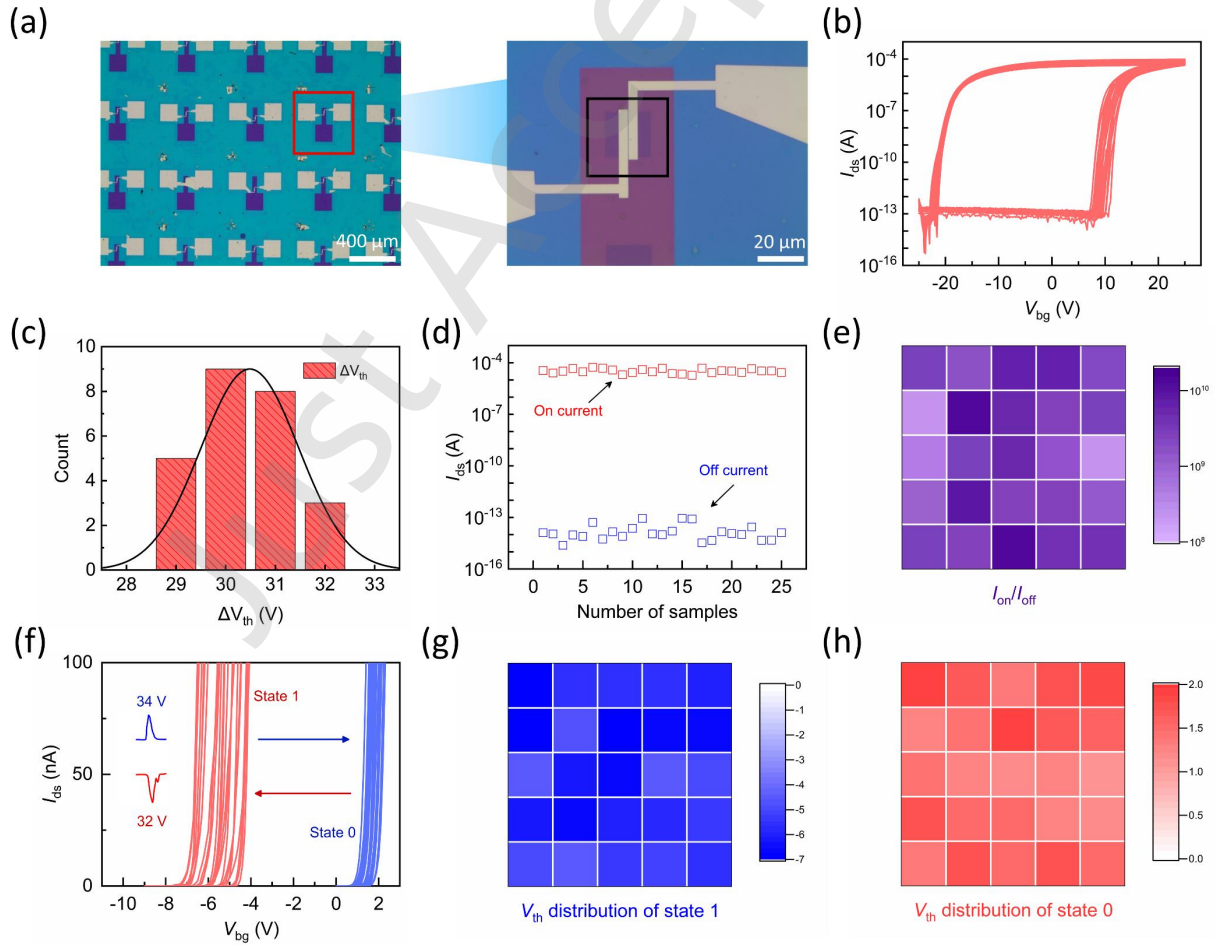


Figure 4. Statistical performance of the ultrafast floating-gate memory array. (a) Optical micrograph of the 5x5 floating-gate memory array. The left panel is an overview of the full array, and

the right panel highlights an individual cell with a 1 μm channel length and a 20 μm channel width. (b) Dual-sweep transfer curves of the 25 devices under a sweep voltage of ± 25 V, demonstrating large and stable memory windows. (c), (d) Statistical results of the memory window test, showing the distributions of the threshold voltage difference (ΔV_{th}) of states 0 and 1 (c) and the on and off currents (d). (e) Switching ratio distribution across the 25 devices. (f) Threshold voltage distribution of the programmed and erased states across the 25 devices. (g), (h) Distribution of threshold voltages of states 0 (g) and states 1 (h) across the 25 devices.

The high-quality $\text{Y}_2\text{O}_3/\text{HfO}_2$ hybrid dielectric layer enables the scalable integration of floating-gate memories. A 5×5 memory array was fabricated to demonstrate the scalability of this approach and the high performance of the memory array, as shown in Figure 4a. Figure 4b-e shows statistics for the memory window based on the d.c. test. All 25 devices in the 5×5 memory array operate successfully (100% yield), with a memory window of 30.5 ± 1.5 V. Figure 4d displays the programmed state and erased state currents for the 25 devices. The erased state currents consistently range between 10^{-5} A and 10^{-4} A, and the programmed state currents remain in the range of 10^{-15} A to 10^{-13} A, yielding an average on/off ratio of up to 10^9 . To switch between the states, a 34 V (60 ns) pulse was used to program the devices to state 0, whereas a -32 V (60 ns) pulse was used to erase them to state 1. Figure 4e displays the distribution of the on/off current ratio across the array, with the maximum ratio up to 10^{10} . Figure 4f-h shows statistics for the ultrafast programming test. Figure 4f presents the V_{th} outcomes for both states. The erased state V_{th} varies over a range of about 2.5 V, whereas the programmed state V_{th} exhibits a much narrower spread of less than 1 V. Notably, all programmed state V_{th} values are above 0 V, satisfying the requirements for practical applications. Figures 4g and 4h illustrate the spatial distributions of these V_{th} . The highly uniform V_{th} distribution across the memory array demonstrates the robust reliability for larger-scale integration.^[32] A quantitative comparison table among recent works is shown in Table S1^[19,21,24,26,29,32,37,38,49-53], and it shows that this work achieves a high level of performance in key metrics, including single-device memory characteristics and device yield, thereby realizing a process-compatible balance of overall device performance.

Benefiting from the outstanding photoresponse of 2D materials, the floating-gate memory device demonstrates efficient optical erasure capability.^[54-56] Figure 5a-b show the energy band diagram during programming and under optical illumination. Here, to simplify the physical picture, the energy bands of the hybrid dielectric layer are merged in the illustration. After programming, electrons stored in the floating gate induce band bending in the structure, electrostatically attracting holes within the MoS_2 channel.^[57] Tunneling

probability is heavily dependent on both the barrier height and the incident photon energy, which is dictated by the light wavelength and intensity.^[58,59] Figure 5c demonstrates the change in source–drain current (I_{ds}) of a programmed floating–gate memory device after 30 s of 447 nm blue light illumination at various power intensities. Figure 5d shows the I_{ds} evolution under a constant power density of $33.9 \text{ mW}\cdot\text{cm}^{-2}$ over varying durations. Complete erasure is realized after 2 minutes of $33.9 \text{ mW}\cdot\text{cm}^{-2}$ blue light, enabling voltage-free erasure of large–area floating–gate arrays.

In summary, utilizing the $\text{Y}_2\text{O}_3/\text{HfO}_2$ hybrid dielectric layer, we successfully realizes a high–performance, ultrafast floating–gate memory array. This hybrid dielectric exhibits excellent leakage–current suppression and capacitive characteristics. The floating–gate memory achieves programming/erasing operations using ultrashort 60 ns pulses, achieving a current on/off ratio of $\sim 10^9$, data retention exceeding 10^4 s , and endurance over 1,800 cycles. The device also demonstrates outstanding performance in threshold–voltage evolution, array–level uniformity and efficient optical erasure. These results establish a viable path toward large-scale integration of ultrafast non-volatile 2D memory arrays.

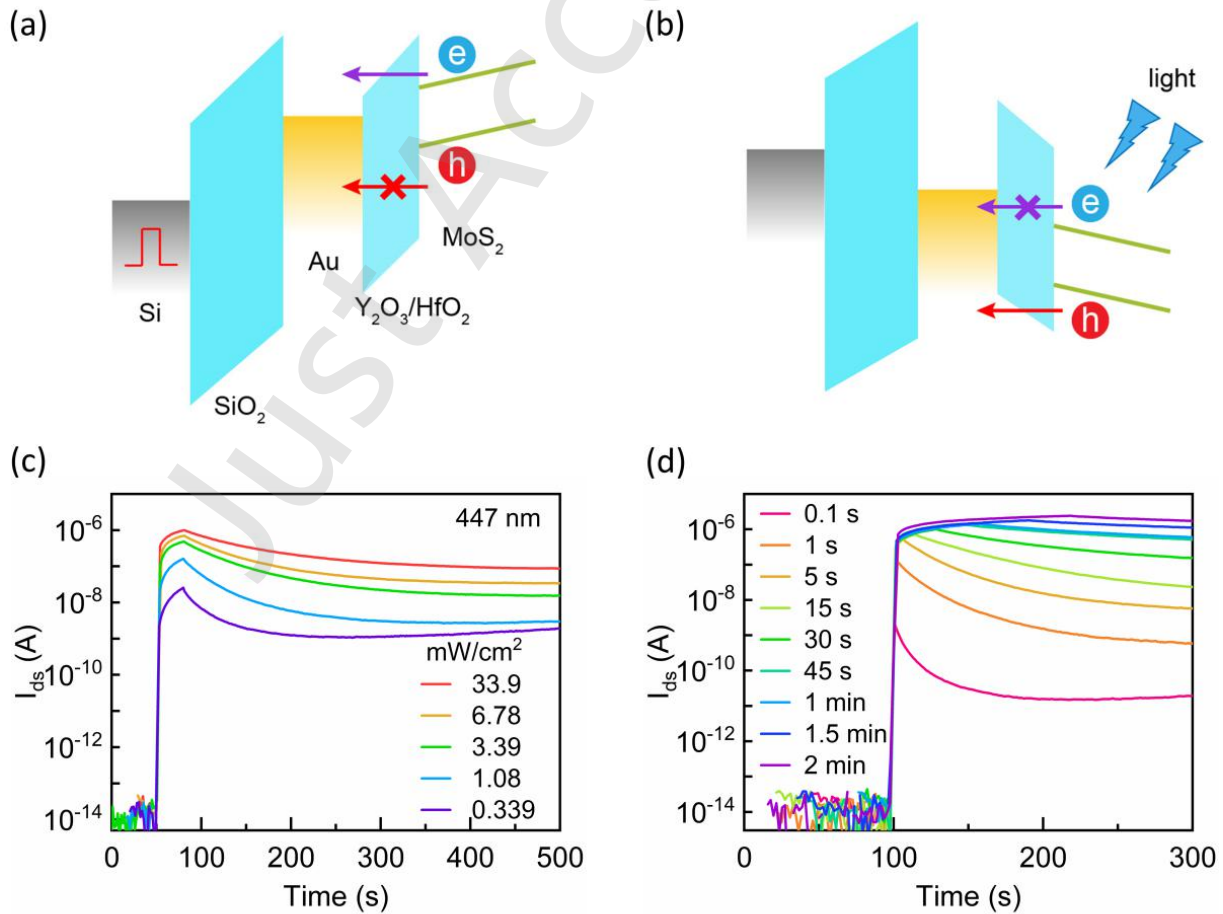


Figure 5. Optical erasing characteristics of the floating-gate memory. (a) Schematic illustration of the energy band diagram during the application of a positive programming pulse. (b) Schematic illustration of the energy band diagram under light illumination. (c) Current variation of the floating-gate device after 30 s of blue light illumination at different optical power densities. (d) Current variation of the floating-gate device under blue light illumination at a fixed power density of 33.9 mW/cm² for varying illumination times.

Experimental Section

Device Fabrication: EBL was utilized to define the floating gate electrode patterns. Cr (2 nm)/Au (10 nm) was deposited via thermal evaporation and lift-off process. Y was evaporated and oxidized in air for 12h (room temperature) to form 4-nm Y₂O₃ seed layer. 12-nm HfO₂ was deposited by ALD at 110°C for 100 cycles. CVD-grown large-area monolayer MoS₂ was transferred via water-assisted transfer method and patterned into a 5×5 array of 20×20 μm² channel regions via SF₆ plasma etching (20 W, 10 s). Finally, Cr (6 nm)/Au (60 nm) source/drain electrodes were deposited by thermal evaporation and lift-off process.

Sample Characterization: The surface morphology and thickness of the Y₂O₃/HfO₂ hybrid dielectric layer were characterized by AFM (Asylum Research Cypher S) under the atmospheric environment. Transmission electron microscopy images and SAED patterns were obtained on JEM ARM200F with a cold-field emission gun. SEM image and EDS mapping were performed using a HITACHI SU5000 with an energy dispersive analysis system Bruker XFlash 6|60.

Electrical measurement: The electrical characteristics of the capacitor, back-gated transistor and floating-gate memory array were determined on Keithley 4200 semiconductor characterization system (4200-SCS, Keithley) equipped with a micromanipulator vacuum probe system (TTPX, Lake Shore Cryotronics, Inc.) under a vacuum of 10⁻⁴ Pa.

Acknowledgements

This work was supported by the National Key Research & Development Projects of China (Grant No. 2022YFA1204100), National Natural Science Foundation of China (Grant Nos. 62488201), CAS Project for Young Scientists in Basic Research (YSBR-003), and Quantum Science and Technology-National Science and Technology Major Project (2021ZD0302700).

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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**Scalable ultrafast non-volatile two-dimensional floating-gate
memory arrays based on HfO₂/Y₂O₃ hybrid dielectrics**

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Supplementary Note

Capacitance Matching and Device Architecture Optimization

To quantify the electrostatic coupling efficiency between the control gate (Si substrate) and the floating gate (Au), the gate-coupling ratio (GCR, α) of the memory device was determined. The potential of the floating gate (V_{FG}) is primarily governed by the control gate voltage (V_{CG}) through a capacitive voltage divider, expressed as:

$$V_{FG} = \alpha \cdot V_{CG} = \frac{C_b}{C_b + C_t} \cdot V_{CG} \quad (1)$$

where C_b and C_t represent the capacitances of the blocking layer (300-nm SiO₂) and the hybrid tunneling layer (16-nm Y₂O₃/HfO₂), respectively.

1. Capacitance of the Blocking Layer C_b :

The blocking capacitance is defined by the geometry of the engineered large-area capacitor pads ($150 \times 150 \mu m^2$). Using the permittivity of SiO₂ ($\epsilon_r \sim 3.9$), the capacitance per unit area c_b is calculated as:

$$c_b = \frac{\epsilon_0 \epsilon_{SiO_2}}{d_{SiO_2}} \approx \frac{8.854 \times 10^{-12} \frac{F}{m} \cdot 3.9}{300 \times 10^{-9} m} \approx 0.115 fF/\mu m^2$$

Thus, the total blocking capacitance is:

$$C_b = c_b \cdot A_{pad} \approx 0.115 \frac{fF}{\mu m^2} \cdot 22500 \mu m^2 \approx 2.59 pF$$

2. Capacitance of the Tunneling Layer (C_t):

The effective tunneling capacitance is determined by the overlap area between the MoS₂ channel ($20 \times 20 \mu m^2$) and the floating gate. Based on experimental measurements of a test structure ($100 \times 100 \mu m^2$) as shown in Figure S2, the tunneling layer exhibits a capacitance of approximately 39 pF, corresponding to a capacitance per unit area (c_t) of:

$$c_t = \frac{39 pF}{10000 \mu m^2} = 3.9 fF/\mu m^2$$

The effective capacitance in the device region is therefore:

$$C_t = c_t \cdot A_{channel} = 3.9 fF/\mu m^2 \cdot 400 \mu m^2 \approx 1.56 pF$$

3. Resultant Coupling Ratio (α):

Substituting these values into the coupling equation yields:

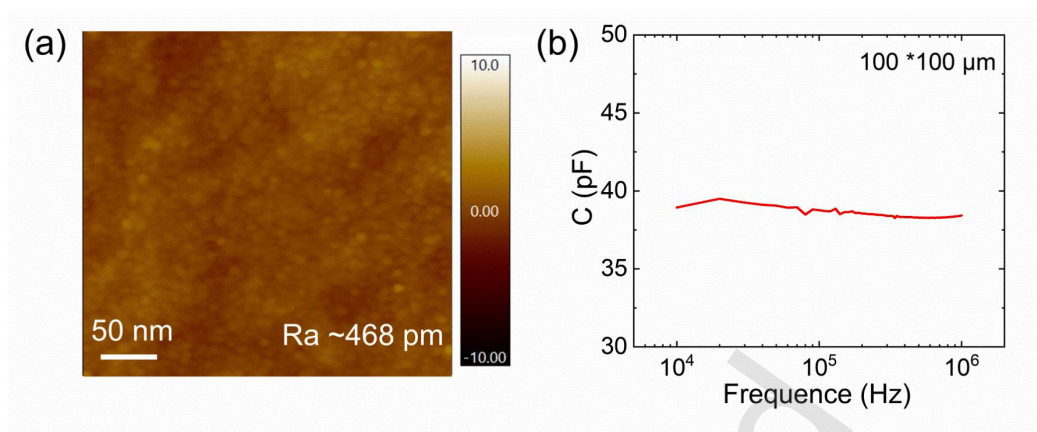
$$\alpha = \frac{2.59 pF}{2.59 pF + 1.56 pF} \approx 0.624$$

This high coupling ratio of approximately 62.4% confirms that a significant portion of the applied gate voltage is effectively dropped across the tunneling dielectric. This strategic

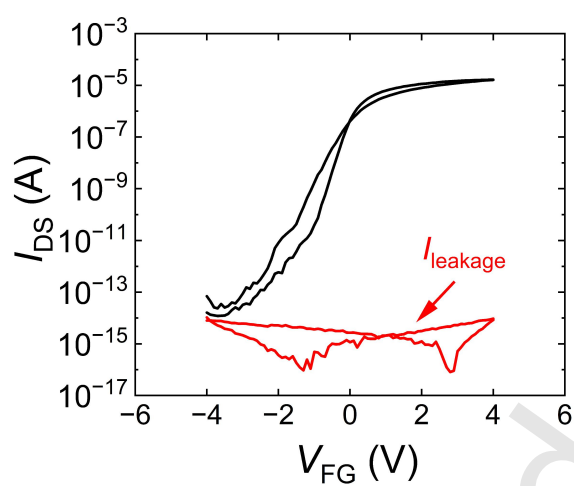
area-ratio engineering compensates for the thickness and permittivity mismatch between the SiO_2 and high- κ layers, facilitating the ultra-strong electric fields necessary for 60-ns ultrafast programming and erasing operations.

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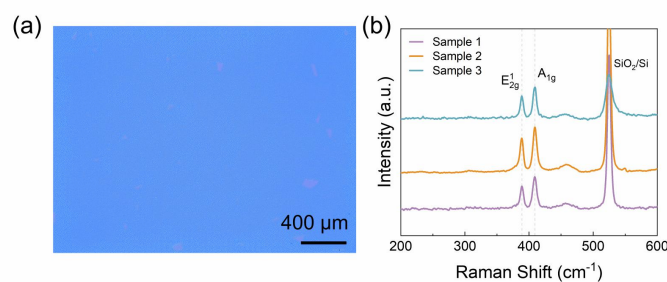
Supplementary Figures



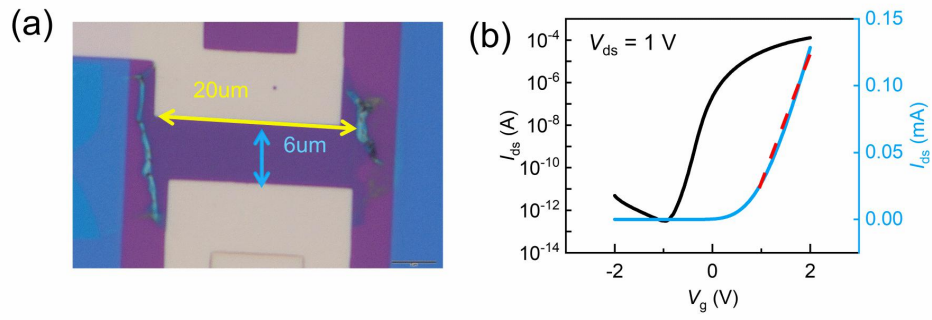
Supplementary Figure S1 | Surface and capacitance analysis of $\text{Y}_2\text{O}_3/\text{HfO}_2$ hybrid dielectric layers. (a) AFM image of the $\text{Y}_2\text{O}_3/\text{HfO}_2$ hybrid dielectric layers. (b) Capacitance characteristics of the $\text{Y}_2\text{O}_3/\text{HfO}_2$ hybrid dielectric layers.



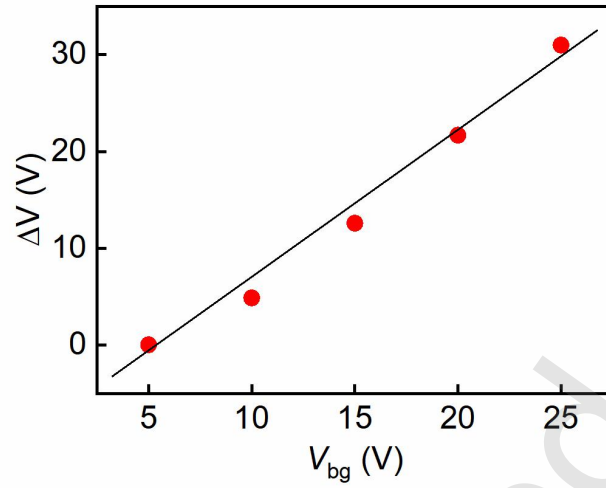
Supplementary Figure S2 | Dual-sweep transfer curve and the corresponding leakage current of a MoS2 transistor with Y₂O₃/HfO₂ hybrid dielectric layers.



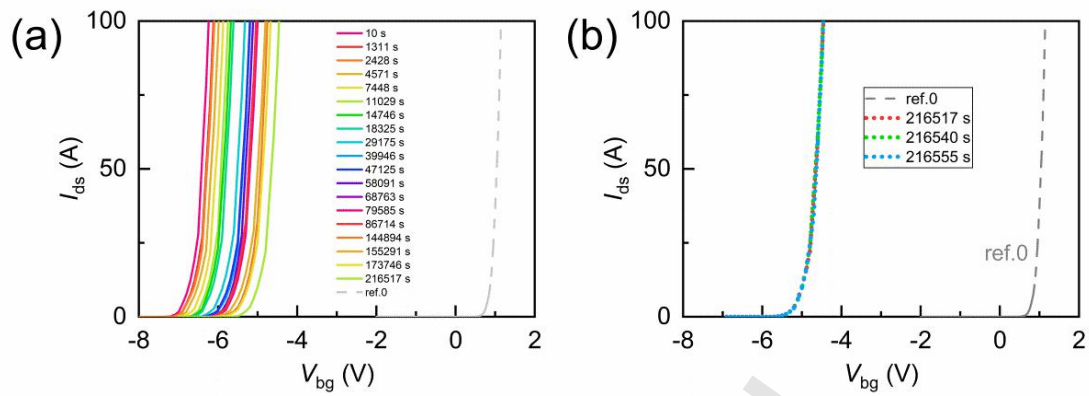
Supplementary Figure S3 | Characterization of the as-grown monolayer MoS₂. (a) A typical optical microscopy image of the monolayer MoS₂ grown on SiO₂/Si, which shows high coverage and uniformity. (b) Raman spectra of three samples, which shows good uniformity. The differences of A_{1g} and E_{2g}¹ are in the range of 20.1 to 20.4 cm⁻¹, suggesting a single layer characteristic.



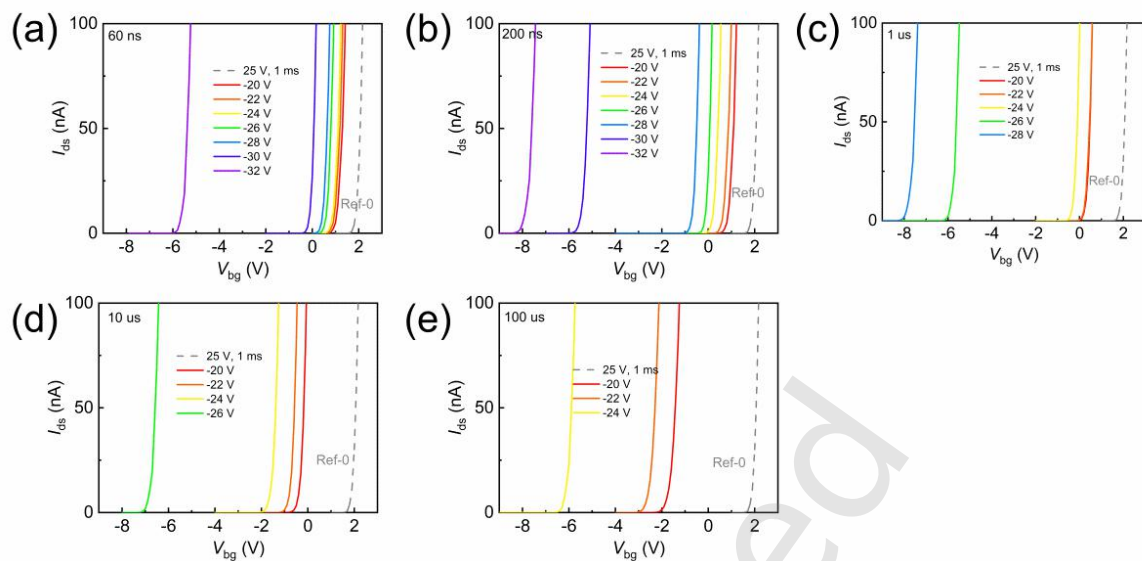
Supplementary Figure S4 | Mobility of monolayer MoS₂. (a) Optical microscopy image of a MoS₂ FET with a channel length of 6 μm and width of 20 μm . (b) Transfer characteristics of the MoS₂ FET. The mobility of the monolayer MoS₂ is $\sim 76 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$.



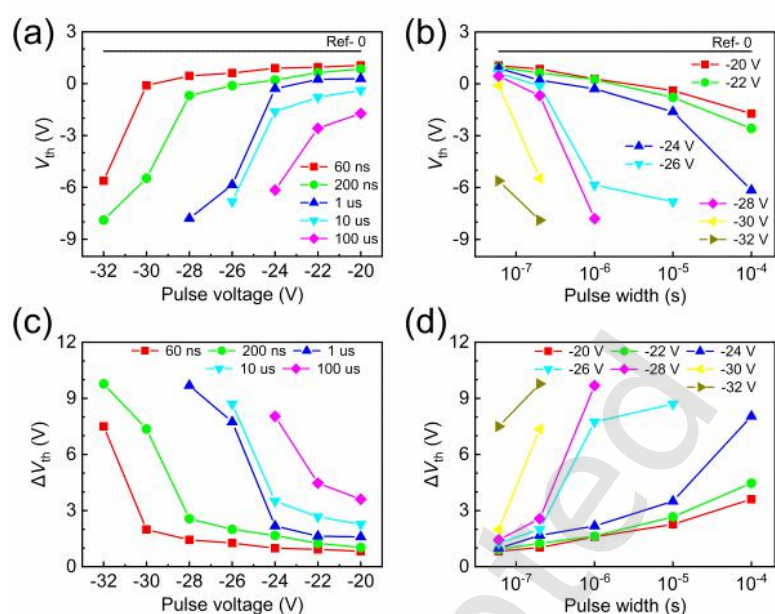
Supplementary Figure S5 | The floating-gate memory device with large memory window. Red dots are the extraction of the memory window as a function of maximum value of V_{bg} ; the solid line is the linear fitting curve, indicating a large storage window at each fixed control-gate voltage.



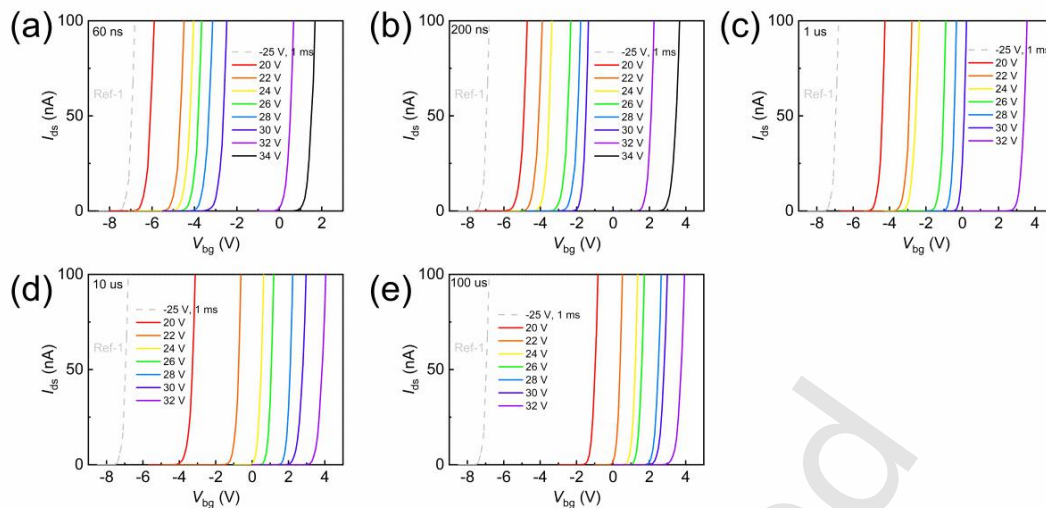
Supplementary Figure S6 | Long-term retention analysis of the $\text{Y}_2\text{O}_3/\text{HfO}_2$ hybrid dielectric-based floating-gate memory. (a) Threshold voltage variation over time after applying a -32 V, 60 ns erase pulse within a 220,000 s timeframe. (b) Impact of testing methodology on the reliability of the retention study.



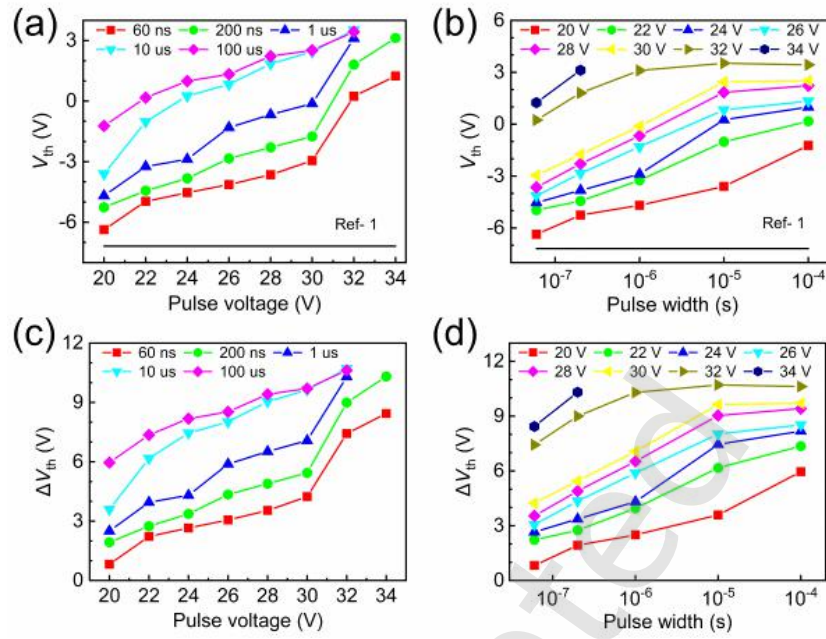
Supplementary Figure S7 | Transfer curves under erasing pulses with varying widths and amplitudes. Transfer curves under erasing pulses with varying amplitudes at pulse widths of (a) 60 ns, (b) 200 ns, (c) 1 μ s, (d) 10 μ s, and (e) 100 μ s.



Supplementary Figure S8 | Summary of threshold voltages under erasing pulses with varying pulse widths and amplitudes. (a) Threshold voltage as a function of pulse amplitude. (b) Threshold voltage as a function of pulse width. (c) Threshold voltage difference as a function of pulse amplitude. (d) Threshold voltage difference as a function of pulse width.



Supplementary Figure S9 | Transfer curves under programming pulses with varying widths and amplitudes. Transfer curves under programming pulses with varying amplitudes at pulse widths of (a) 60 ns, (b) 200 ns, (c) 1 μ s, (d) 10 μ s, and (e) 100 μ s.



Supplementary Figure S10 | Summary of threshold voltage trends under programming pulses with varying widths and amplitudes. (a) Threshold voltage as a function of pulse amplitude. (b) Threshold voltage as a function of pulse width. (c) Threshold voltage difference as a function of pulse amplitude. (d) Threshold voltage difference as a function of pulse width.

Table S1 Device parameters in short channel transistor research. Considering the influence of the source-drain voltage on the performance, data obtained at $V_{ds} = 0.1$ V are used wherever possible. For parameters not directly reported in the literature (especially I_{on} and I_{off}), they are estimated from the provided transfer characteristics. Here the contact and channel materials (Cr/Au-MoS₂ (this work), Y-InSe, Gr-MoS₂, Cr/Au-MoS₂ and 1T'-2H MoS₂) are used to refer to each study.^{1–13}

Type	Reference	Channel / memory stack	P/E speed	Extinction ratio	Retention	Endurance	Array yield
	This work	MoS ₂ / Y ₂ O ₃ /HfO ₂ / Au	60 ns	~10 ⁹	>10 yr	>1.8×10 ³	25 cells; 100%
Memory array	1	MoS ₂ /HfO ₂ /Pt/HfO ₂	20 ns	>10 ⁹	>10 yr	>10 ⁵	1024 cells; 98.4%
	2	MoS ₂ /HfO ₂ /Pt/HfO ₂ /Pt	n/a	>10 ⁵	>1 h	500	1024 cells; 83.1%
Memory chip	3	MoS ₂ /HfO ₂ /Pt/HfO ₂ /Pt	20 ns	>10 ⁷	>10 yr	>10 ⁴	94.34%
Transistor array	4	MoS ₂ /Al ₂ O ₃ /ITO	n/a	10 ¹⁰	n/a	n/a	1518 transistors per cm ² ; 98.4%
	5	MoS ₂ /MnO ₃ /HfO ₂	n/a	3.2×10 ⁸	n/a	n/a	1024 cells; 92.2%
Transistor (Seed layer)	6	MoS ₂ /Si/HfO ₂ /Pd	n/a	10 ⁸	n/a	n/a	n/a
Memory device	7	InSe/hBN/MLG	20 ns	10 ¹⁰	>10 yr	>2.0×10 ³	n/a
	8	MoS ₂ /hBN/MLG/hBN/MLG	20 ns	10 ⁸	>10 yr	~4.2×10 ³	n/a
	9	MoS ₂ /Al ₂ O ₃ /Pt	230 ns	10 ⁸	>10 ⁴ s	>10 ⁵	n/a
	10	Graphene/hBN/HfO ₂ /Al ₂ O ₃	0.4 ns	n/a	>10 yr	5.5×10 ⁶	n/a
	11	ReS ₂ /hBN/graphene	2 ms	>10 ⁵	>10 ³ s	>10 ³	n/a
	12	ReS ₂ /hBN/graphene	4 ms	>10 ⁴	>10 ³ s	>3×10 ³	n/a
	13	MoTe ₂ /hBN/graphene	4 ms	>10 ⁴	>10 ³ s	>10 ³	n/a

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