

Realization of monolayer black phosphorus transistors via van der Waals metal lamination

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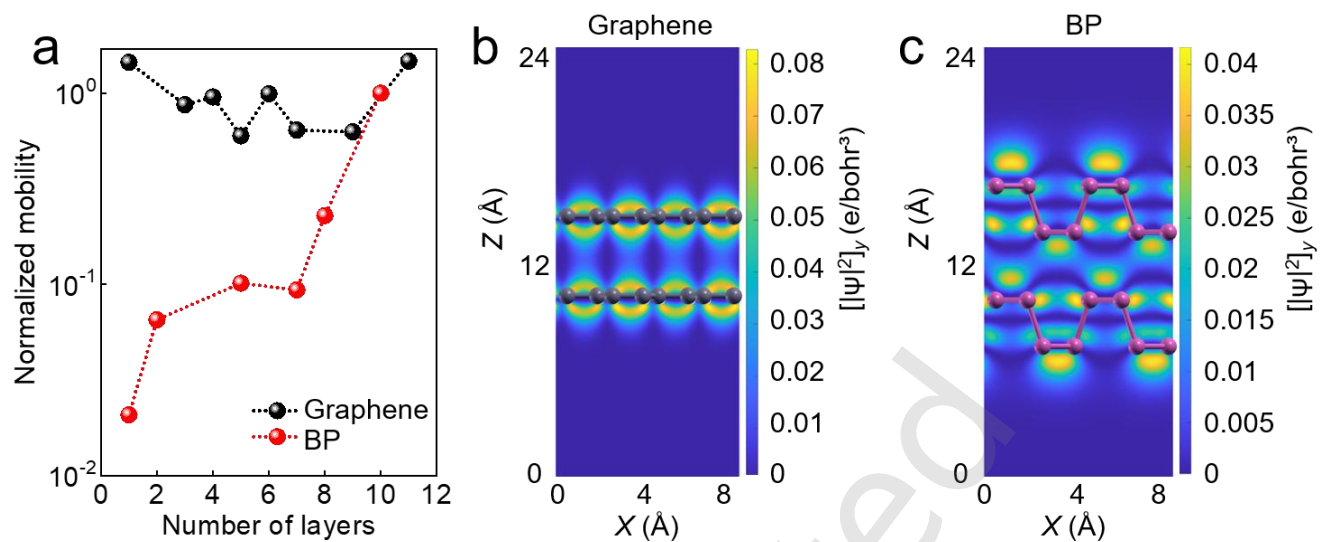
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ABSTRACT: Black phosphorus (BP) is a promising 2D material that has attracted tremendous attention owing to its high carrier mobility and large tunable bandgap from the visible to mid-infrared range. However, due to the unstable lattice structure, monolayer BP is highly sensitive to oxygen and water, and its delicate monolayer channel could be totally destroyed during conventional fabrication process (involving multiple solution steps). Therefore, even after a decade of intense input, the monolayer BP transistor has yet to be realized, and its fundamental electrical and optoelectronic properties remain largely unknown. Here, we report a van der Waals integration method to realize pure monolayer BP devices and investigate its electrical and optical properties. We found the carrier mobility of BP drops sharply with channel thickness down to monolayer, which is more like a conventional bulk semiconductor rather than a layered vdW semiconductor. Furthermore, the optoelectronic performance of the monolayer black phosphorus transistor has also been investigated, exhibiting a large photoresponsivity of 17 A/W and a detectivity of 3.1×10^8 Jones. Our work first realized pure monolayer BP devices and investigated their intrinsic electrical and optoelectronic properties, which could open new possibilities for the exploration of rich physics within monolayer BP as well as other unstable semiconductors.

KEYWORDS: van der Waals integration, black phosphorus, monolayer black phosphorus (BP) transistor, photodetector

1 Introduction

Black phosphorus (BP) is a promising 2D material that has attracted tremendous attention owing to its high carrier mobility [1-3], unique anisotropic properties [1, 4, 5], and tunable band gaps [2, 6]. In particular, black phosphorus has a tunable and direct bandgap that ranges from ~ 0.3 eV (bulk) to ~ 2 eV (monolayer) [6]. This is in great contrast to many 2D semiconductors (such as MoS₂ or WSe₂), which typically display a direct-to-indirect bandgap transition with increasing layer thickness. The large tunable direct bandgap and high carrier mobility make BP an appealing semiconductor for light detection, emission, and communication over a very broad energy spectrum from the visible to mid-infrared range [5, 7-9]. However, although the high carrier mobility at monolayer thickness is the primary motivation for BP research, previous studies are largely focused on the devices using relatively thick flakes (over 3 nm or 5 layers). In contrast, monolayer BP devices are seldom fabricated and investigated, greatly limiting the exploration of rich physics within monolayer BP as well as its practical device applications.

The key challenge in fabricating monolayer BP devices is the difficulty in producing monolayer channel material and forming robust metal contacts. First, from the material point of view, BP

exhibits relatively smaller Young's modules compared to other 2D semiconductors such as MoS₂ (41.3 GPa vs 262 GPa, ref. [10, 11]). Therefore, when directly exfoliating BP bulk crystals onto conventional SiO₂ substrate, the achieved flakes are largely multilayer with thickness > 3 nm. The possibility to find monolayer flake is very low, and its size is typically too small ($< 1 \mu\text{m}$) for device fabrication and characterization. Second, from device fabrication point of view, black phosphorus has a fragile lattice and degrades rapidly when exposed to oxygen or water environment, particularly for monolayer devices. Unfortunately, conventional metallization methods involve aggressive processes such as solution spin-coating and development, high-energy photolithography/electron radiation, as well as hot metal atom/cluster bombardment during contact metal deposition. Therefore, when these fabrication processes are directly conducted on BP surface, monolayer BP is totally open-circuit without measurable electrical signals (Fig. S1 in the Electronic Supplementary Material (ESM)). To overcome this problem, 3D raised contact geometry [12] was recently reported by thinning the multilayer channel layer-by-layer into a monolayer, while contact region is still multilayer to maintain its robust metal contacts. However, this method only produces a partial monolayer channel, while the real channel is mixed multilayer/monolayer and the contact region is much thicker

multilayer BP. Therefore, even after a decade of intense input, the real monolayer BP transistor has yet to be realized, and its fundamental electrical and optoelectronic properties remain largely unknown.

Here, we report a simple method to realize pure monolayer BP devices and investigate its electrical and optical properties. By functionalizing the standard SiO₂ substrate, the adhesion force between BP and substrate is effectively increased, leading to the exfoliation of large enough BP monolayer with lateral size over 100 μm . On the other hand, low-energy van der Waals (vdW) integration technique is adopted to contact the monolayer channel. By pre-fabricating metal electrode pairs on a sacrificial substrate and then physically laminating them onto monolayer black phosphorus surface, all aggressive fabrication processes are not directly conducted on the delicate BP lattice. Together, we first realized monolayer BP transistors and measured their electrical properties. Interestingly, we found the carrier mobility of BP drops sharply with channel thickness down to monolayer, which is more like a conventional bulk semiconductor rather than a layered vdW semiconductor. Furthermore, the optoelectronic performance of the monolayer black phosphorus transistor has also been investigated, exhibiting a large photoresponsivity of 17 A/W and a detectivity of 3.1×10^8 Jones. Our work first realized a pure monolayer BP device and investigate its intrinsic electrical and optoelectrical properties, which could open new possibilities for the exploration of rich physics within monolayer BP as well as its practical device applications. It could also provide exciting implications for other emerging semiconductors (such as molecular monolayers, organic thin films/crystals, and the halide perovskite materials), which are typically not stable under ambient conditions and are not compatible with traditional micro-fabrication processes.

2 Results

2.1 Fabrication of pure monolayer BP transistor

Figure 1 schematically illustrates the fabrication process for monolayer BP transistors. To fabricate the device, a thin layer of PVA (poly(vinyl alcohol), 9.3 nm thick, root-mean-square (RMS) roughness of 0.29 nm) is first spin-coated onto a standard silicon substrate with 300 nm thick SiO₂, as detailed in Methods section. Next, BP flakes are exfoliated onto the functionalized substrate using Scotch tapes. We note that the inclusion of PVA layer is essential to improve the substrate adhesion force, leading to the exfoliation of large enough BP monolayer (with lateral size over 100 μm) and high exfoliation yield, as shown in the optical image in Fig. 1(a) and Fig. S2 in the ESM. In contrast, when directly exfoliating BP bulk crystals to conventional SiO₂ substrate (without PVA layer) using same method, the achieved flakes are largely multilayer with thickness exceeding 4 nm (Fig. S2(b) in the ESM), limiting the realization of monolayer device.

The thicknesses of exfoliated BP flakes are measured by atomic force microscopy (AFM), photoluminescence (PL) spectroscopy, and Raman spectra. Figure 1(a) shows the optical images of exfoliated BP flakes with three different thicknesses of monolayer, bilayer and trilayer, and its AFM height profile is illustrated in Fig. 1(b), showing a step change of 0.55 nm and corresponding to the thickness of monolayer BP [12, 13]. The Raman spectra of monolayer, bilayer, and trilayer BP are presented in Fig. 1(c), demonstrating a clear thickness dependence with the A_g^1 and A_g^2 modes shifting toward each other as the thickness increases, consistent with previous reports [14]. The measured PL peaks of monolayer, bilayer, trilayer BP are located at 745 nm, 946 nm, and 1275 nm, respectively, corresponding to a direct band gap of 1.66 eV, 1.31 eV, and 0.97 eV for monolayer, bilayer and trilayer BP (Fig. 1(d)), also matching well with previous reports [15, 16].

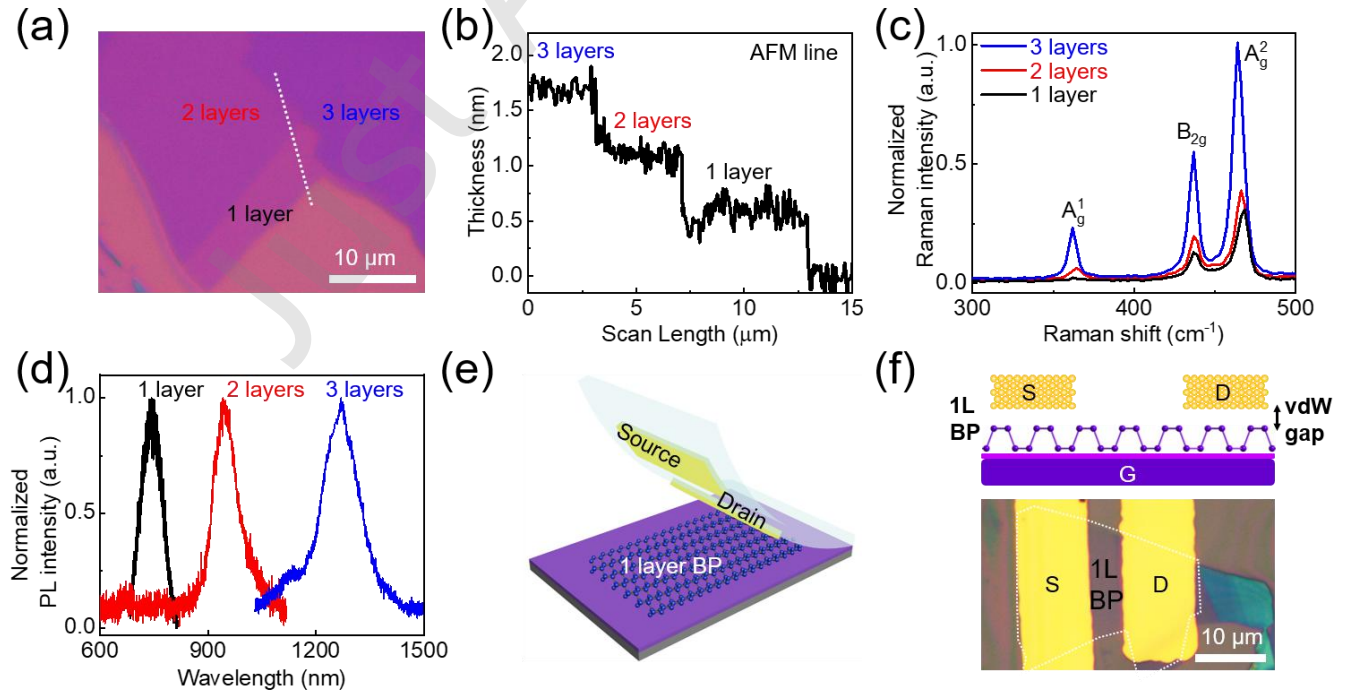


Figure 1 Fabrication and characterization of pure monolayer BP transistor. (a) Optical images of the exfoliated black phosphorus flake with monolayer, bilayer and trilayer thicknesses, and its corresponding AFM height profile at white dashed line location. ((b)-(d)) Corresponding AFM height profile (b) Raman spectra (c) and PL spectra (d) of monolayer, bilayer, and trilayer black phosphorus. (e) Schematic of the fabrication process for monolayer BP transistor using vdW metal electrodes. (f) Cross-section schematic (top) and optical image (bottom) of a representative monolayer device.

With the successful exfoliation of large enough BP monolayers, field effect transistors can be fabricated by laminating pre-patterned metal electrodes onto monolayers. As shown in Fig. 1(e), the Au electrode pair (50 nm thick) is prefabricated on a sacrifice Si wafer and then mechanically released using a previously developed method [17], demonstrating an atomically flat bottom surface that replicates silicon surface. Furthermore, the Au electrode pair is physically laminated on BP surface using vdW integration technique (detailed in Methods). To avoid the impact of oxygen and water, all the BP exfoliation and metal transfer process are conducted within a nitrogen filled glovebox. The cross-section schematic and optical image of a typical fabricated device are shown in Fig. 1(f). We note our vdW metal lamination technique is essential to fabricate monolayer BP transistors. Using conventional microelectronic fabrication process, the high energy process would damage the contact region of monolayer BP and a development step (alkali solution based) could introduce defects in the channel region. These impacts have already been demonstrated in MoS₂ but could be even more detrimental to the unstable BP lattice. To confirm this, we have also fabricated monolayer/bilayer BP transistors using conventional metal evaporation process. As shown in Fig. S1 in the ESM, the monolayer/bilayer samples are open-circuit without any measurable current.

2.2 Electrical properties of BP transistors with different thicknesses

The electrical properties of resulting vdW BP transistors are measured using a probe station at room temperature under vacuum (10⁻⁴ Torr). Within the device, 50 nm thick gold electrode pairs are used as the source/drain electrodes, and 300 nm thick SiO₂ is used as the back-gate dielectric. As shown in Fig. 2(a), the monolayer BP transistor exhibits clear n-type semiconductor behavior from I_{ds} - V_{gs} transfer behavior with on/off ratio over 10⁶, representing the first realization of true

monolayer BP transistors. Furthermore, the two-terminal carrier mobility is extracted from the transfer curves using equation $\mu = (L/WC_g V_{ds}) \times (dI_{ds}/dV_g)$, where μ is the field-effect mobility, L and W are the channel length and width, respectively, and C_g is the capacitance of back-gate dielectric. The extracted two-terminal mobility of the monolayer BP transistor is 5.1 cm² V⁻¹ s⁻¹, similarly to previous theoretical predictions [18]. This mobility value is several orders of magnitude smaller than that of multilayer BP, which could be largely attributed to several reasons of monolayer BP [18], including the increased effective mass, stronger carrier confinement, increased deformation potential, and reduced stiffening of the interlayer optical modes. Importantly, the device

also exhibits good stability, as shown in Fig. S3 in the ESM, indicating the improved contact quality of our approach. We further applied this method to monolayer GeAs transistors (Fig. S4 in the ESM), demonstrating its effectiveness for other unstable 2D semiconductors beyond BP.

Interestingly, the monolayer BP device exhibits robust n-type transfer behavior, in great contrast to conventional p-type behavior of multilayer BP devices [14, 19]. This electrical behavior is consistent with the theoretical calculations [20], where Au forms an n-type Schottky contact with monolayer BP due to the small electron barrier (compared to large hole barrier). As the thickness increased to multilayer, the BP bandgap reduced quickly from ~2 eV to 0.3 eV, and the Schottky barrier is relatively small for both electron and holes [21, 22], hence the device is totally dominated by the intrinsic p-type defects and p-type Fermi level pinning within BP. This thickness-dependent n-type to p-type transition is beneficial for CMOS integration, but has not been observed in other 2D semiconductors (such as MoS₂, WSe₂) using vdW contacts, which could be largely attributed to the relatively small bandgap change from monolayer to multilayer (for example, ~1.8 eV to 1.2 eV for MoS₂). To further confirm this, we have measured the electrical properties of vdW BP device

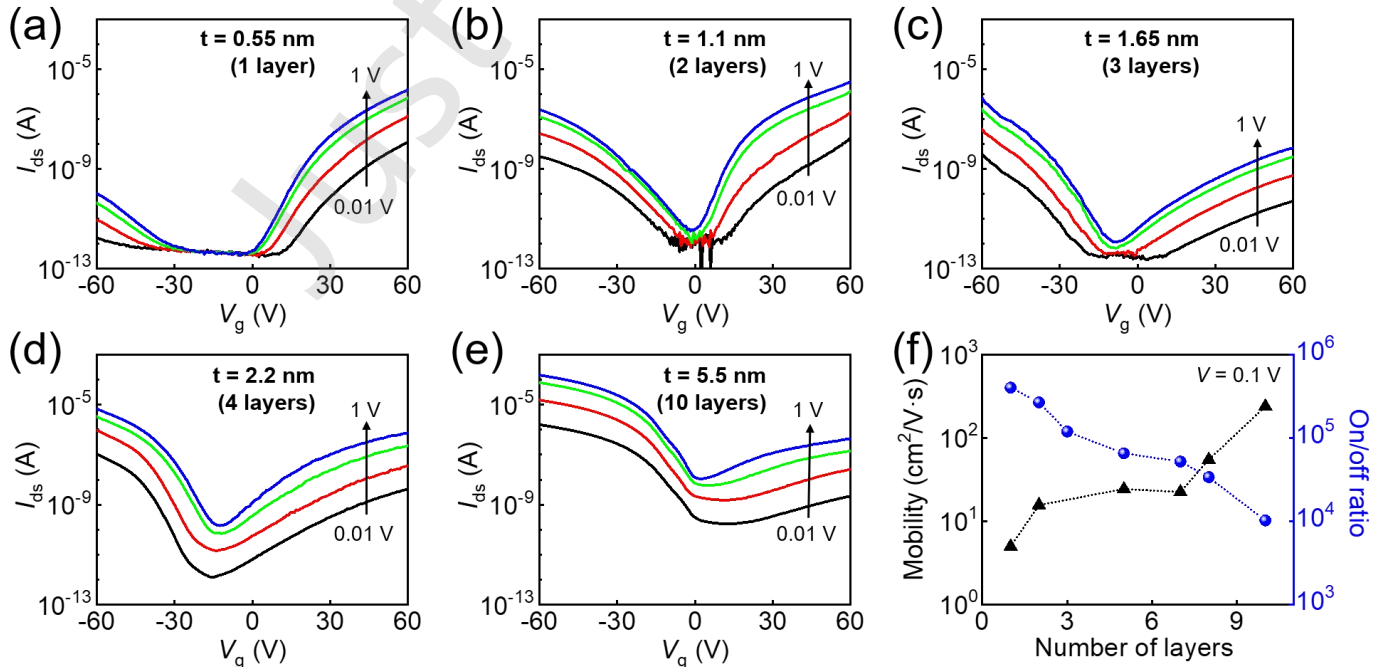


Figure 2 Electrical properties of vdW BP transistors with different channel thicknesses. ((a)-(e)) I_{ds} - V_{gs} transfer characteristics of BP transistors with varying thicknesses: (a) 1 layer, (b) 2 layers, (c) 3 layers, (d) 4 layers, and (e) 10 layers. (f) The extracted on/off ratio and field-effect mobility as functions of the BP

thickness.

with different thicknesses (Fig. 2(a-e)). In general, as the layer thickness increases, the electron transport of BP transistor weakens, while hole transport is enhanced. When the channel thickness is larger than 3 layers (1.65 nm thick, Fig. 2(c)), p-type transport is more obvious in BP transistor; and as the

channel thickness further increased to 10 layers (5.5 nm thick, Fig. 2(e)), p-type behavior eventually dominates whole device transport. At this stage, the ten-layer BP transistor exhibits a hole mobility of $250 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with on/off ratio 10^4 , which is in line with multilayer BP transistor [12, 23].

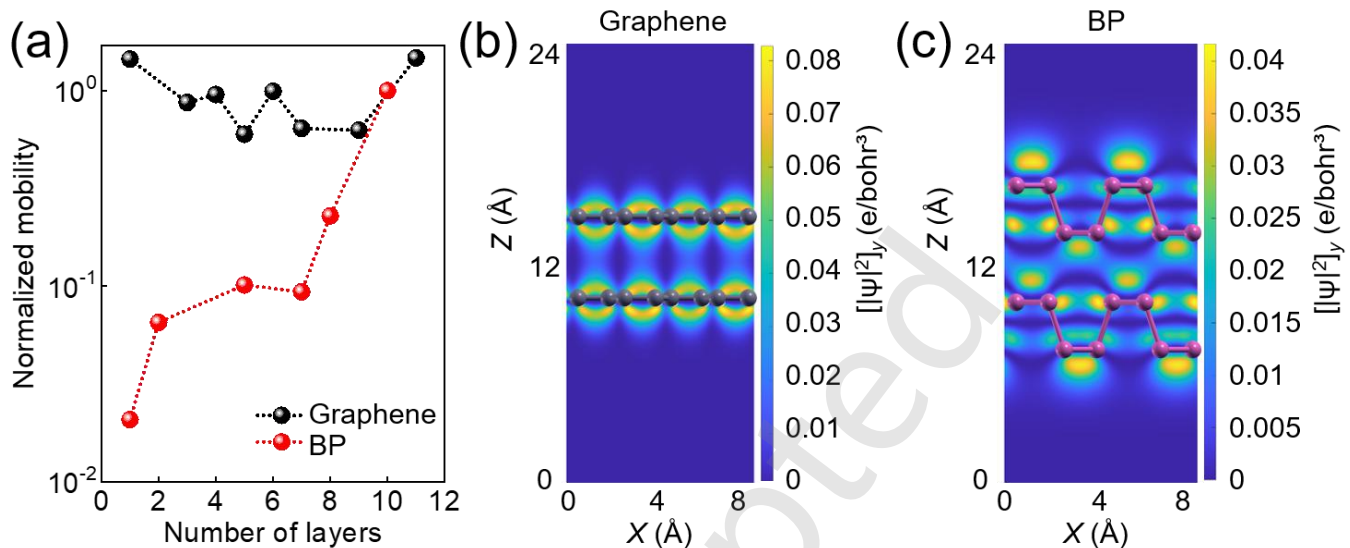


Figure 3 Thickness-dependent carrier transport within BP and graphene systems. (a) The normalized carrier mobility of BP transistors and graphene transistors as a function of their layer number. ((b)-(c)) Squared amplitude of the wave function for the lowest-energy conduction band for bilayer graphene and bilayer BP.

2.3 Quasi vdW transport behavior of BP transistor

With the ability to successfully fabricate monolayer BP transistor, we could further investigate the thickness-dependent performance of BP transistors. As shown in Fig. 2(f) and Fig. 3(a), the on-off ratio of BP transistors gradually increases with decreasing thickness; while on the other hand, the carrier mobility decreases quickly with channel thickness. At monolayer limit, the carrier mobility is only $5.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, roughly 2% of the mobility value in ten layers device ($250 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). Such large mobility degradation is in great contrast to conventional 2D materials such as graphene, MoS_2 , and WSe_2 [24-26]. To confirm this, we have also fabricated graphene transistors as controls with different thicknesses, using same fabrication process. As shown in Fig. 3(a) and detailed in Fig. S5 in the ESM, the carrier mobility of graphene transistors remains relative stable with channel thickness reduced from eleven layers down to monolayer. It is well known that 2D semiconductors such as MoS_2 and WSe_2 [26, 27], with their dangling-bond-free surfaces, exhibit little mobility degradation upon thickness reduction. In conventional covalent bulk semiconductors (such as Si), the carrier mobility μ sharply decreases with decreasing body thickness ($\mu \sim t^6$, refs. [28, 29]). This channel-thickness scaling limitation actually intrigues the development of 2D transistors such as graphene and MoS_2 , where the mobility varies little with body thickness and decent mobility values could be achieved even at monolayer limit. From this point of view, the large mobility degradation in BP suggests that it is markedly different from 2D materials, which is an interesting phenomenon and deserve deeper understanding. In addition to intrinsic properties, the relatively poor stability of BP may also cause its mobility to decrease sharply as the thickness decreases. However, we believe that stability is not a

key factor, as BP devices are fabricated using dry processes in a nitrogen atmosphere, and the measurements are carried out on a high-vacuum probe station.

To explain this unique behavior, we have applied density functional theory (DFT) to simulate the wave functions of both BP and conventional graphene systems. As shown in Fig. 3(b), in the graphene system, the vdW coupling energy between adjacent layers is very small and therefore does not significantly alter the bonding properties or the out-of-plane localization of the wave functions. Consequently, each layer is largely independent between each other, and the carrier mobility remains relatively stable with reducing body thickness. In contrast, the interlayer coupling force in BP system is an order of magnitude stronger than that graphene system, indicating that the interlayer interactions in BP possess a partial covalent character rather than pure vdW forces, as shown in Fig. 3(c). Hence, the lone-pair p-orbitals of BP hybridize into bonding and antibonding orbitals, weakly localized or even delocalized along the out-of-plane direction. This leads to a sharp reduction in carrier mobility as the body thickness decreases. From this point of view, BP behaves more like a conventional covalent bulk semiconductor (or a quasi-vdW semiconductor) than a pure vdW semiconductor, which is consistent with theoretical predication and our previous experiment in mixed multilayer-monolayer BP system [12, 18].

2.4 Optoelectronic properties of monolayer BP device

BP has attracted lots of attention these years, and one primary motivation is its tunable direct bandgap that can be tuned from $\sim 2 \text{ eV}$ in monolayer to $\sim 0.3 \text{ eV}$ in bulk state, holding promising potential for 2D based light emission and detection from visible

to middle-infrared regime. However, due to the fabrication challenges, the optoelectronic properties of monolayer BP devices have yet to be measured. With the ability to realize high quality and pure monolayer BP device using vdW lamination, we can further investigate its optoelectronic properties. The electrical measurements were performed in a vacuum probe station under global laser illumination. First, 520 nm laser (with intensity of 0.4 mW/mm²) is used as the light source, which has an excitation energy of 2.38 eV and is larger than the bandgap of monolayer BP. Figure 4(a) shows the corresponding I_{ds} - V_{ds} output curves of monolayer BP transistor under both dark and

illuminated conditions. In general, the I_{ds} increases with light illumination, confirming the generation of photocarriers within monolayer BP device. Furthermore, the photocurrent I_{ph} is also calculated (equals to $I_{light}-I_{dark}$), showing a linear increase with bias voltage V_{ds} (Fig. 4(b)), due to the increased carrier drift velocity and the corresponding reduction in the carrier transit time [30]. We also explored the time-dependent photocurrent in monolayer BP phototransistors under gate voltage $V_g = 60$ V, at which state the photocurrent is maximized due to the strong gate doping effect.

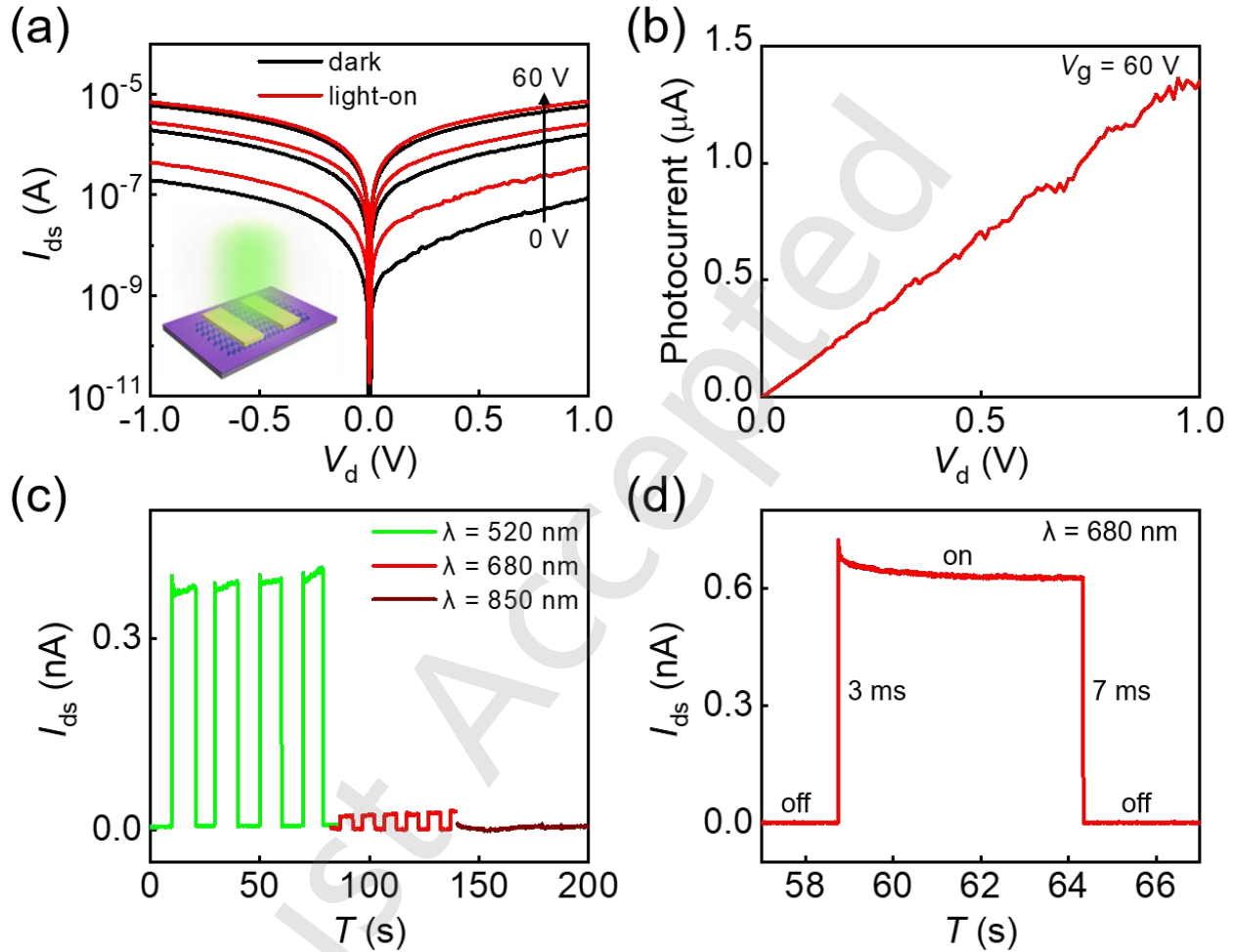


Figure 4 Optoelectronic properties of monolayer BP device. (a) I_{ds} - V_{ds} output curves of monolayer BP transistor under both dark and illuminated conditions, and the corresponding device schematics is shown in the inset. (b) The calculated pure photocurrent ($I_{light}-I_{dark}$) under different bias voltage. (c) Photoswitching (current versus time) behavior of a monolayer BP transistor measured under periodic on/off light illumination ($V_g = 0$ V, $V_d = 1$ V). (d) A single response cycle of the device under 680 nm illumination, exhibiting $T_{rise} \sim 3$ ms and $T_{fall} \sim 7$ ms.

As shown in Fig. S6 in the ESM, although the I_{ds} current is not stable under such high gate voltage, clear photocurrent of ~ 150 nA could still be observed during light-on and light-off switching, corresponding to a high photoresponsivity of 17 A/W and a detectivity of 3.1×10^8 Jones. Furthermore, light sources with different wavelengths are applied to study the broadband photodetection of monolayer BP. Under 680 nm illumination (photon energy of 1.82 eV, 6.5 mW/mm²), the photoresponse is significantly weaker compared to 520 nm illumination, but it can still be observed in Fig. 4(c). However, when the photon energy is further reduced to 1.46 eV (850 nm light source), photocurrent cannot be detected even with much higher light intensity of 16 mW/mm², due to the smaller photon energy compared to large

bandgap of monolayer BP, indicating the observed photocurrent is originated from the photo-generated carriers rather than photo-thermal effect. Finally, we also characterized the response speed of the monolayer BP device. As shown in Fig. 4(d), the device exhibits a photoresponse in the visible spectrum with switching dynamics of $T_{rise} \sim 3$ ms and $T_{fall} \sim 7$ ms (see the zoomed-in views in Fig. S7 in the ESM), comparable to those of previously reported multilayer BP transistors [31, 32].

3 Conclusion

In summary, our work has overcome a critical preparation challenge in exploring the intrinsic properties of monolayer black phosphorus. By employing non-destructive van der Waals

metal integration techniques, the true monolayer black phosphorus transistor has been successfully fabricated. The work has also revealed that strong interface coupling between the metal electrode and the monolayer black phosphorus can induce carrier-type inversion, resulting in unique n-type transport characteristics. This is in stark contrast to the p-type behavior typically observed in multilayer black phosphorus transistors. In addition, we observed a sharp decrease of carrier mobility with decreasing BP thickness and explained this behavior using DFT calculation, suggesting BP is more like a conventional bulk semiconductor rather than a layered vdW semiconductor. Finally, we also investigated the optoelectronic performance of monolayer BP transistors with a photoresponsivity of 17 A/W and a detectivity D^* of 3.1×10^8 Jones. It could also provide exciting implications for other emerging unexplored 2D materials or emerging semiconductors (such as molecular monolayers, organic thin films/crystals, and the halide perovskite materials), which are typically not stable under ambient conditions and are not compatible with traditional micro-fabrication processes.

4 Methods

4.1 Device fabrication processes

Au electrode pairs is deposited on an atomically flat silicon substrate by using standard photolithography or electron-beam lithography, followed by high-vacuum evaporation. Next, a hexamethyldisilazane (HMDS) layer is applied to functionalize the whole wafer at 100 °C for 3 min, and the poly(methyl methacrylate) (PMMA) layer is then spin-coated on top of the metal electrodes with a speed of 2500 rpm. Finally, the PMMA layer with array electrodes is mechanically peeled and laminated to the target substrate under the optical microscope assisted by an aligned transfer platform. Before exfoliation of BP flakes, a poly(vinyl alcohol) (PVA) (1 wt%, from Alfa Aesar, 98–99% hydrolyzed, molecular weight 130,000 g/mol) layer is first spin-coated onto highly doped Si substrates (with 300 nm thick SiO₂) to functionalize their surface and to enhance their interaction with 2D semiconductors. The spin-coating of PVA layer is conducted at 8000 rpm for 30 s, followed by 70 °C baking for 2 mins. Monolayer BP is mechanically exfoliated from commercial bulk crystals (Shanghai Onway Technology Co., Ltd.).

4.2 Electrical measurements and materials characterizations

Atomic force microscope (Bioscope system, Bruker) is used to characterize the morphology and thickness. The electrical characterizations of the BP devices are performed in a Lakeshore PS-100 cryogenic probe station using a semiconductor device parameter analyzer (Agilent, B1500). The total exposure time to atmosphere is controlled within 2 mins to minimize device degradation. The Raman and PL measurement are conducted using Renishaw inVia-reflex, under a 488 nm laser excitation. During the Raman and PL measurements, a pre-fabricated PMMA film is laminated onto the BP flake to protect it from air exposure. For few-layer phosphorene (2L to 3L), the PL measurements were conducted using a T64000 micro-Raman system equipped with a InGaAs detector.

4.3 DFT Method

The density functional theory (DFT) calculation is carried out by the open-source package QUANTUM ESPRESSO [33]. The

Perdew-Burke-Ernzerhof (PBE) exchange-correlation functionals from PSLibrary.1.0.0 are used, with the semi-empirical DFT-D3 vdW correction and the plane-wave cut-off energy of 34 (P) and 40 (C) Ry. To the few-layer models, vacuum spaces of more than 15 Å are added at the thickness direction [34]. The Brillouin zone k -point sampling is $5 \times 5 \times 1$ at the electronic ground-state computations. The crystals are optimized until the force and energy criteria of 1×10^{-4} eV/Å and 1×10^{-4} eV [35].

Electronic Supplementary Material: Supplementary material (please provide the brief detail of the ESM) is available in the online version of this article at <https://doi.org/10.26599/NR.2026.94909088>.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

The authors declare no competing interests.

Author contribution statement

Y.L. conceived the research. Y.L. and W.L. designed the experiments. W.L., and Yunxin.L. performed the sample fabrication and device measurement. Q.T., L.K., S.D., Z.L., C.L., Z.Lu., X.L., M.H., H.C., X.T., and L.M. contributed to data analysis. Yawei.L., Y.W., Lei.L., D.L., and Liting.L. contributed to AFM and optical characterization. Y.L. and W.L. co-wrote the paper. All authors discussed the results and commented on the paper.

Use of AI statement

None.

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Realization of monolayer black phosphorus transistors via van der Waals metal lamination

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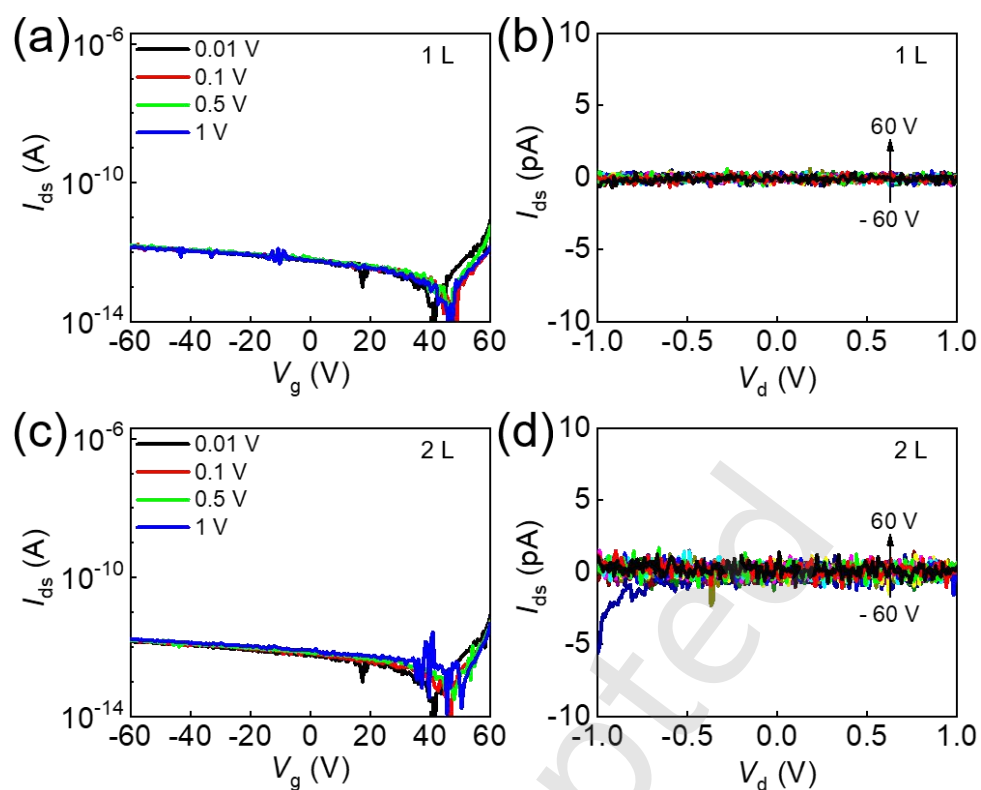


Figure S1 Electrical properties of BP transistors using e-beam lithography and contact evaporation process directly on BP surface. ((a)-(b)) I_{ds} - V_{gs} transfer characteristics and the I_{ds} - V_{ds} output curves of monolayer BP FET, where only noise current was measured. ((c)-(d)) I_{ds} - V_{gs} transfer characteristics and the I_{ds} - V_{ds} output curves of bilayer BP FET, where only noise current was measured.

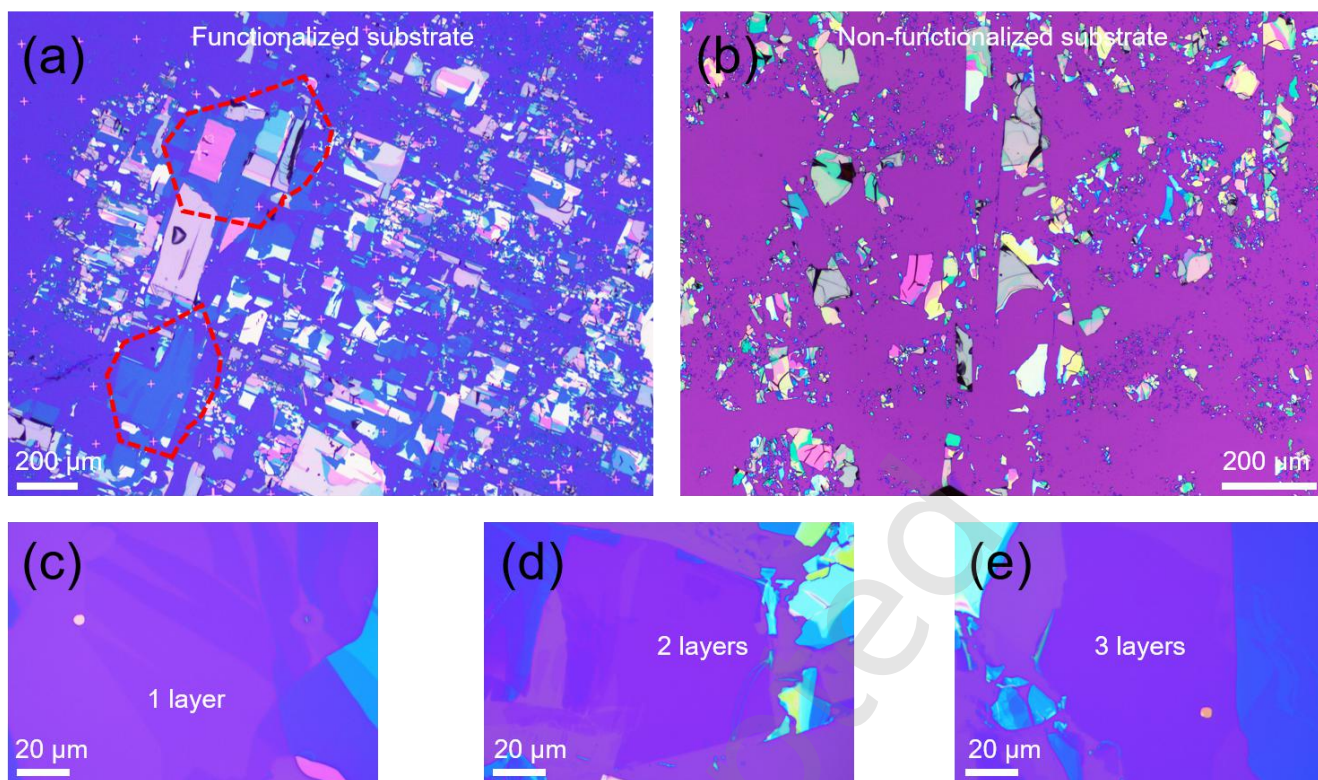


Figure S2 Optical images of black phosphorus with different thicknesses. ((a)-(b)) Exfoliation of black phosphorus with different layer numbers on functionalized substrates (a) versus on non-functionalized original substrates (b), where the surface functionalization can enhance the exfoliation yield of monolayer BP. ((c)-(e)) 1 layer, 2 layers, and 3 layers of large-area materials on functionalized substrates, with lateral size over 100 micrometers.

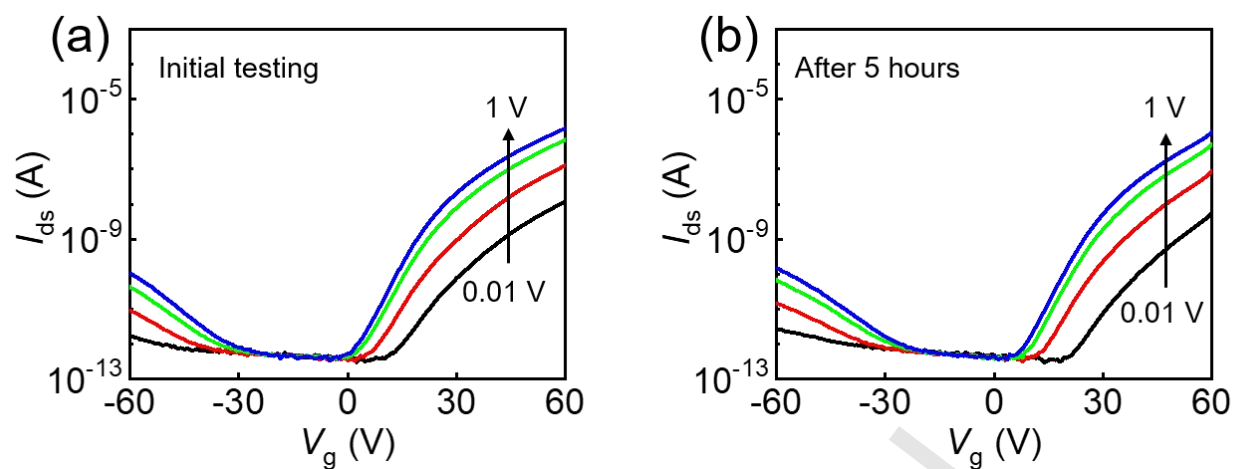


Figure S3 Stability of monolayer BP transistor. ((a)-(b)) I_{ds} - V_g transfer characteristics of monolayer BP transistor measured in vacuum probe station for different storage times.

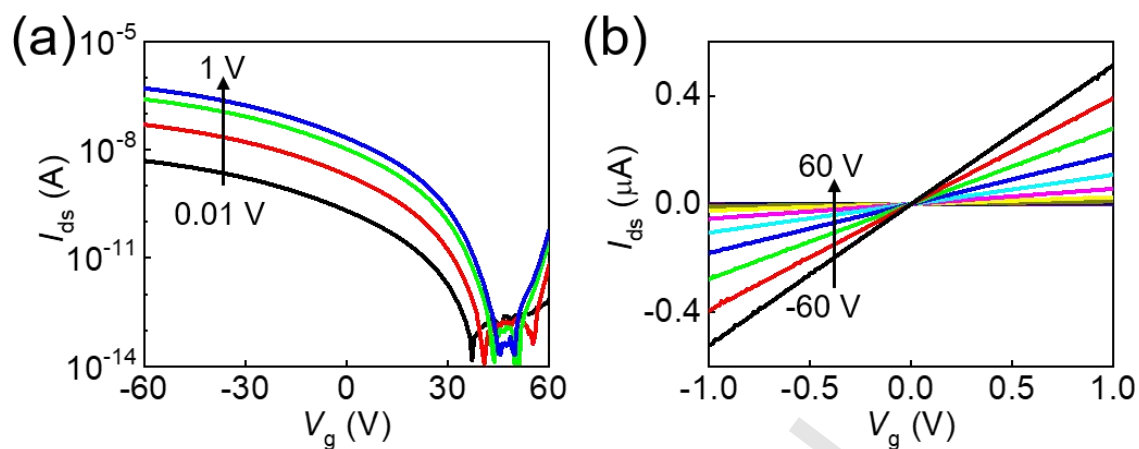


Figure S4 Electrical properties of monolayer GeAs transistor. ((a)-(b)) I_{ds} - V_g transfer characteristics and I_{ds} - V_d output curves of monolayer GeAs transistor measured in vacuum probe station. The mobility is approximately $0.9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an on/off ratio is exceeding 10^7 at a bias of 1 V.

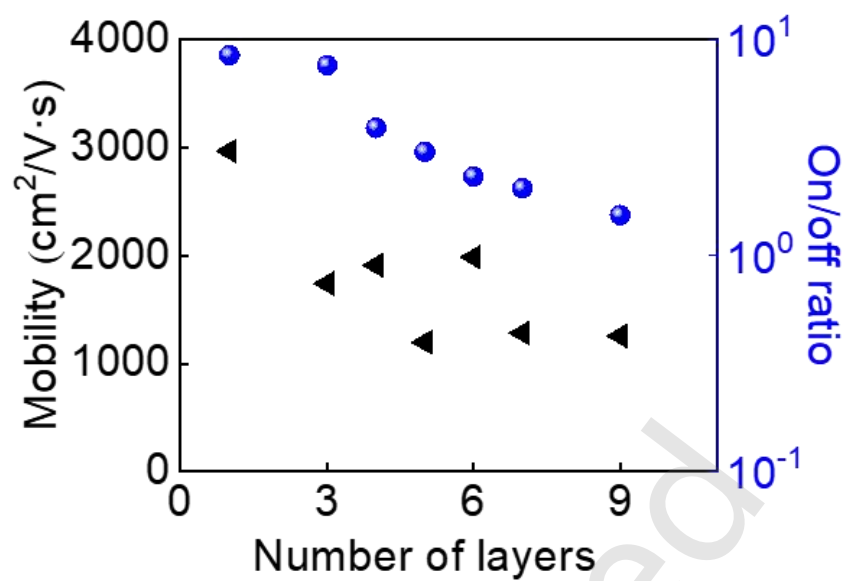


Figure S5 Field effect mobility values as a function of graphene thickness, showing weak thickness dependence.

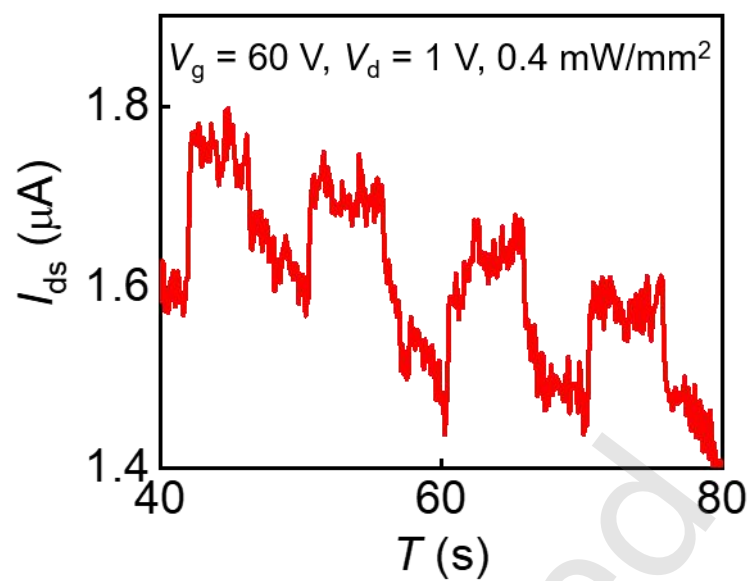


Figure S6 Photo-switching responses of monolayer BP field-effect transistor. Time-dependent photocurrent measured at $V_g = 60 \text{ V}$.

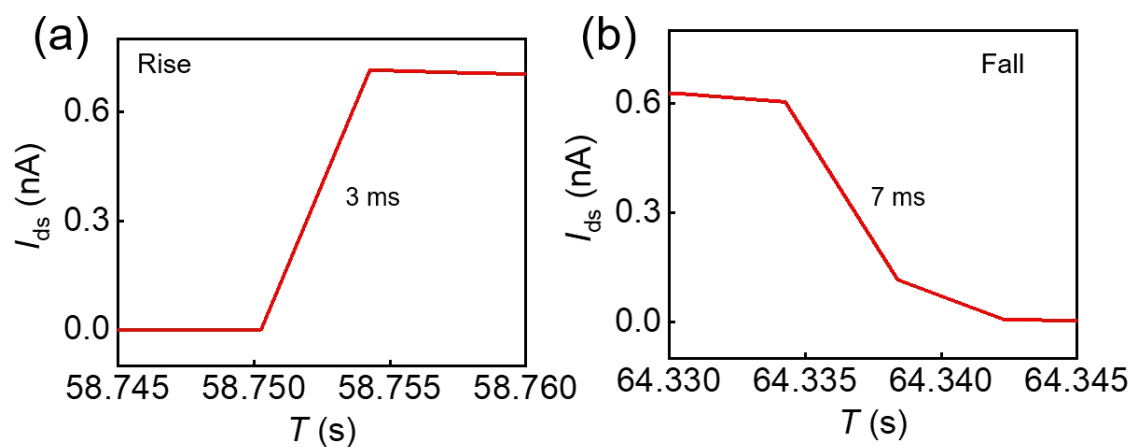


Figure S7 ((a)-(b)) Zoomed-in views of the rise (a) and decay (b) edges of the time-resolved photoresponse.