

Suppressing trap density in carbon nanotube transistors via atomically smooth amorphous metal gates

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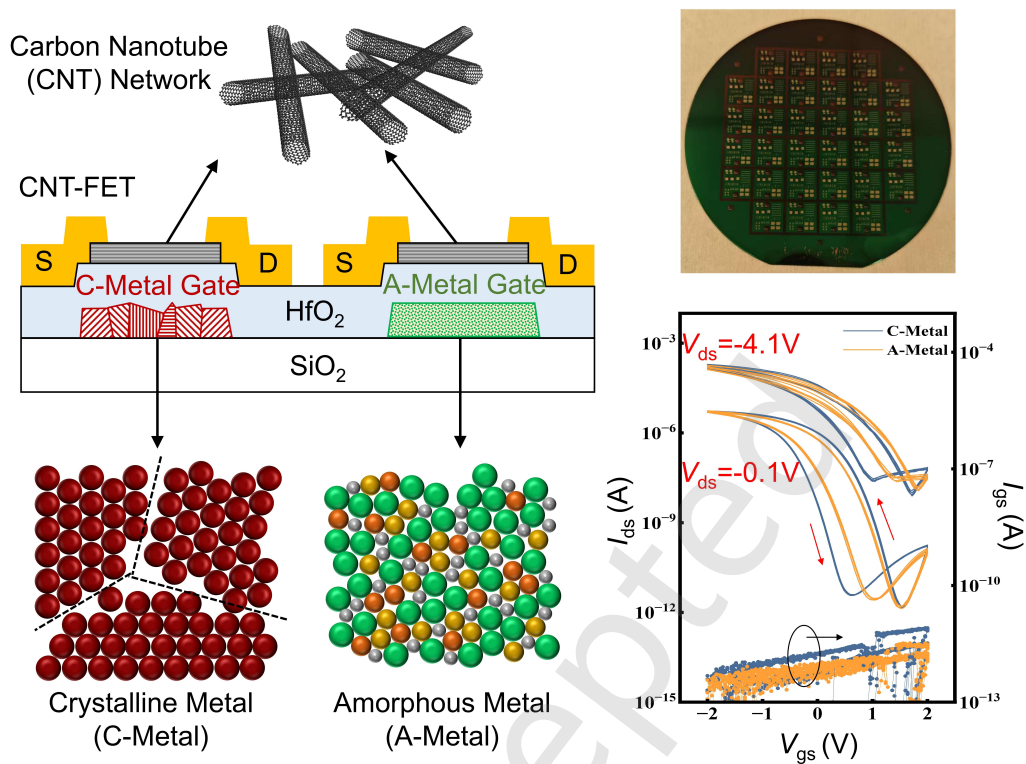
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This work reveals gate topography as a critical factor governing interface trap dynamics in carbon nanotube transistors. By introducing an atomically smooth amorphous metal gate, the interface trap density is reduced by 39.27%, leading to significantly suppressed hysteresis and improved device performance.

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ABSTRACT: Carbon nanotube-based (CNT-based) transistors are promising devices for next-generation electronic devices owing to their extraordinary electrostatics, high carrier mobility, and compatibility with low-temperature processing. However, in the widely used bottom-gate configuration, gate topography as a nanoscale physical parameter and its role in governing interfacial states and charge dynamics in carbon nanotube transistors remains insufficiently studied, despite its significant influence on interface charge trapping, hysteresis, bias-stress stability, and overall device performances. This work systematically investigates the role of gate topography by introducing an atomically smooth amorphous metal (ZrCuAlNi) as bottom-gate electrode, and comparing it with conventional polycrystalline metal gate. Owing to its homogeneous, grain-boundary-free microstructure, the amorphous metal gate enables the formation of a high-quality gate dielectric interface, which reduces the interface trap density by 39.27% in average and consequently lowers the device hysteresis voltage by about 50%, accompanied by improved carrier mobility, on-state current and bias stress stabilities, while maintaining the on/off ratio ($>10^6$). These results reveal that nanoscale gate surface morphology plays a critical role in regulating interfacial trap dynamics and charge transport in CNT transistors. The interface de-pinning mechanism demonstrated here with ultrasmooth gates is expected to be broadly applicable to other semiconductors. Consequently, this work provides both a specific material solution for stable CNT transistors and new insights into interface engineering strategies for carbon nanotube electronics and other carbon-based electronic devices.

KEYWORDS: carbon nanotubes (CNTs), thin-film transistors (TFTs), gate topography, amorphous metal, interface traps, carbon-based electronics

1. Introduction

Carbon nanotubes (CNTs) are one-dimensional carbon nanomaterials that have attracted extensive interest for next-generation electronic devices due to their exceptional carrier mobility, electrostatics, mechanical flexibility, and compatibility with low-temperature processing. The advancement of high-resolution displays and advanced integrated circuits imposes increasingly stringent requirements on transistor performance. For display applications, devices require high carrier mobility, high driving current, mechanical flexibility, and compatibility with low-temperature processing[1]. For chip applications, the pursuit of higher speed, lower power consumption, and greater integration density necessitates channel materials with excellent mobility, superior electrical controllability, and compatibility with modern fabrication processes.

Among emerging channel materials, semiconducting single-walled CNT networks exhibit significant advantages for both rigid and flexible electronics. In the flat-panel display (FPD)

field, CNTs exhibit strong potential for display backplanes [2-4], compared to mainstream thin-film materials, such as amorphous silicon (a-Si), low-temperature polycrystalline silicon (LTPS)[5, 6], and metal-oxide semiconductors (e.g., IGZO), due to their high mobility, strong current drive capability, flexibility, and low-temperature process compatibility[3, 5, 7-11]. In addition, CNTs are regarded as a promising channel material for building high-speed, low-power logic and radio-frequency integrated circuits (ICs), owing to their extremely high intrinsic mobility and ideal electrostatic properties. Their potential has been demonstrated in device scaling[12], circuit integration[13], and three-dimensional architectures[14].

However, CNT-based transistors still face interface challenges especially the significant hysteresis voltage caused by interface defects and charge trapping[15]. This issue not only affects the uniformity and stability of display driving but also constrains the performance and reliability of chip circuits[5, 10, 16-20]. Therefore, understanding and engineering the interfaces in CNT devices are essential for

achieving stable and high-performance carbon-based electronics.

Gate topography refers to the nanoscale surface morphology of the bottom-gate electrode, which encompasses surface roughness, edge profile, and three-dimensional geometry. Among these, surface roughness determines the quality of the gate dielectric layer itself in bottom-gate devices, which in turn dictates the interface state between the dielectric-channel. In bottom-gate transistor manufacturing, the quality of dielectric and its surface roughness are critical interfacial factors influencing device performance. For example, in amorphous indium-gallium-zinc oxide (a-IGZO) TFTs, the rough dielectric surface increases interface scattering and trap density, thereby reduces the on-state current and field-effect mobility[21-23]. In organic TFTs, rough surface leads to higher grain boundary density and localized trap states in the semiconductor layer, resulting in 98% degraded carrier mobility and increased 302% subthreshold swing[24]. For CNTs, the existing literature have indicated that the substrate roughness affects the uniformity of the CNT film, thus limiting the top-gate device performance[25]. In contrast, for bottom-gate architectures, the influence of bottom gate surface roughness and dielectric surface roughness on the performance of CNT transistors remains ambiguous, and the underlying mechanism by which they exert such influence has yet to be thoroughly investigated.

Therefore, to investigate the impact of gate topography on the performance of CNT transistors, this study employs amorphous metal as the bottom gate material. Amorphous metal, also known as metallic glass, is characterized by a disordered, non-crystalline atomic structure. This unique arrangement results in a material that is inherently free from crystalline defects such as grain boundaries and dislocations. Their smooth and chemically uniform surface enables high-quality interface formation with the gate dielectric, which is expected to suppress interface states, reduce leakage current, and improve electrical stability[26]. Furthermore, amorphous metals possess good corrosion resistance, high flexibility, strength, surface smoothness and

strong compatibility with conventional deposition processes such as sputtering and evaporation. These properties make them a reliable gate material suitable for advanced micro- and nanofabrication processes [27-34].

Given this theoretical premise, we fabricated and systematically compared bottom-gate CNT transistors with conventional polycrystalline metal (C-Metal) gates and amorphous metal (A-Metal) gates. Compared to C-Metal, the A-Metal exhibits significantly reduced surface roughness. Moreover, A-Metal leads to an overall enhancement in device performance, specifically, 50% lower hysteresis voltage, 16.8% higher carrier mobility while maintaining excellent switching characteristics (with an on/off ratio $> 10^6$). Further analysis of interfacial states reveals the operational mechanism in CNT-TFTs. For CNT-TFTs, gate topography does not alter the CNT layer's morphology; its effect is dominated by interface trap states and their scattering to carrier transport.

2. Results and discussion

2.1 Device Fabrication

A schematic of the fabricated transistors with a local bottom-gate top-contact structure is shown in Figure 1(a). In this experiment, polycrystalline Au (Figure 1(b)) and amorphous metal $Zr_{55}Cu_{30}Al_{10}Ni_5$ (Figure 1(c)) were deposited by the same magnetron sputtering tool on the same wafer as C-Metal and A-Metal for comparison. As shown in Figure S1, the elements of both A-Metal and C-Metal are uniformly distributed throughout the region. The amorphous ZrAlCuNi provides atomically smooth surface and bias stress stability[35, 36], as well as compatibility with a broad range of gate dielectric materials[37]. The crystalline structures of C-Metal and A-Metal are illustrated in Figures 1(b), and 1(c), respectively. The corresponding device structures are illustrated in Figure 1d. Both types of devices were designed and fabricated on the same wafer to mitigate processing variations, with identical channel dimensions ($W_{ch} = 100 \mu m$, $L_{ch} = 10 \mu m$). Fabrication of the devices proceeded as follows. First, C-Metal and A-Metal were deposited by sputtering and patterned by lifting-off in sequence on a SiO_2/Si substrate.

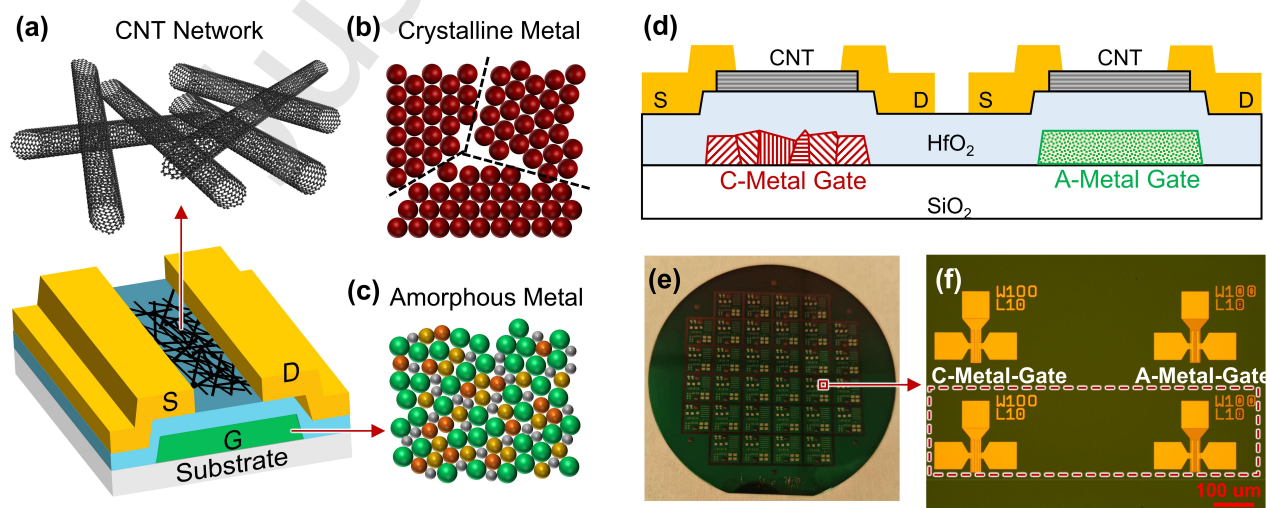


Figure 1. (a) Design and structure of bottom-gate transistors based on semiconducting CNT networks. (b,c) The crystalline structure of (b) C-Metal and (c) A-Metal. (d) Schematic cross-sections of devices with C-Metal and A-Metal. (e) Photo and (f) microscopic image of C-Metal and A-Metal device: on the same 4-inch wafer.

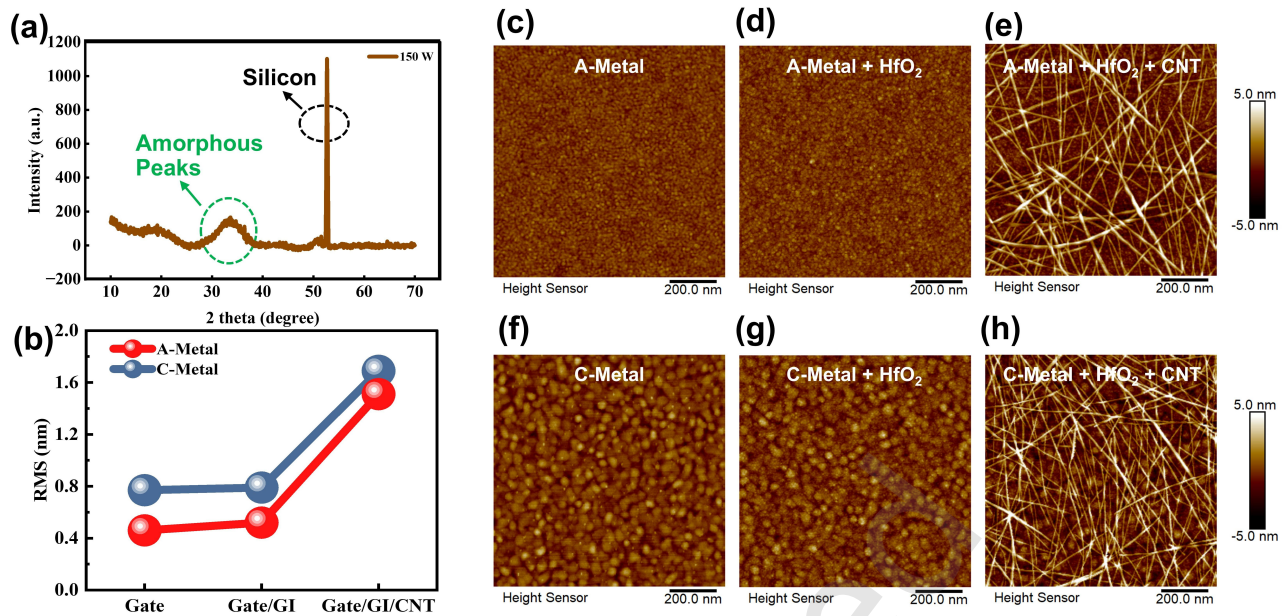


Figure 2. (a) Crystalline phase state of the A-Metal thin film. (b) Evolution of RMS roughness across the different stacks for both gate metals. Interfacial morphology of CNT-TFTs with two gate metals and structural characterization of A-Metal. (c-e, f-h) AFM topographies of the gate, HfO₂ dielectric deposited on the gate, and CNT network on the gate/dielectric for the A-Metal (c-e) and C-Metal (f-h) stacks.

Subsequently, a hafnium oxide (HfO₂) layer was uniformly deposited as the gate dielectric over both gate electrodes by the same atomic layer deposition (ALD) process with identical thickness – 13.19 nm on C-Metal and 12.79 nm on A-Metal, as measured by high-resolution transmission electron microscopy (HRTEM) in Figure S2. The semiconducting CNT networks were then deposited as the channel material on the HfO₂ surface by a solution dipping process, followed by oxygen plasma etching to pattern the channel region. Contact vias were opened in the gate dielectric layer by wet etching to allow electrical access to

the underlying gate metals. The fabrication was completed by patterning and depositing the source and drain electrodes (Ti/Pd) via electron-beam evaporation (EBE). The fabricated devices are shown in Figures 1(e), (f).

2.2 Quantitative Analysis of Surface Topography

The amorphous nature of the magnetron-sputtered ZrCuAlNi film was verified by X-ray diffraction (XRD). As shown in Figure 2(a), its XRD pattern exhibits only a broad diffuse peak at approximately 33° two-theta, which is a characteristic signature of its long-range disordered

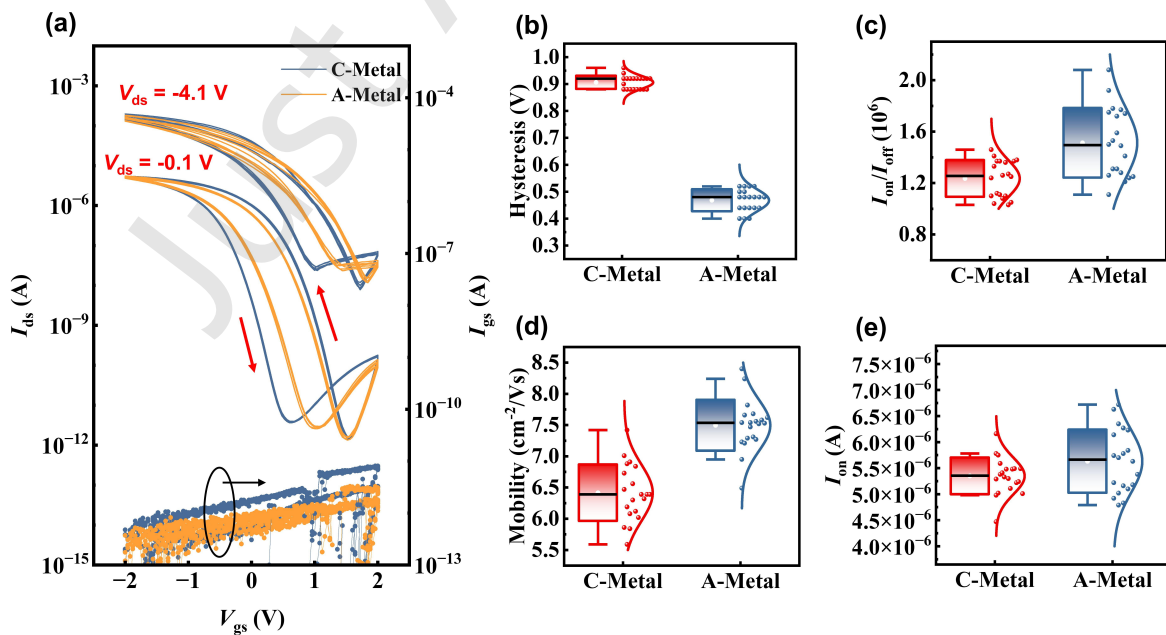


Figure 3. (a) Transfer characteristics of the C-Metal and A-Metal devices (5 devices each, with size of $W_{ch}/L_{ch} = 100/10 \mu\text{m}$). (b-e) Box-and-whisker plots showing the performance variability of devices with C-Metal and A-Metal gates. The parameters correspond to (b) hysteresis, (c) on/off ratio (I_{on}/I_{off}), (d) field-effect mobility (μ), and (e) on-state current (I_{on}), respectively. Gaussian fits are included as solid lines. The mean and the median values are indicated by the white dots and the black line, respectively.

amorphous structure. As shown in Figure 2(b), the surface roughness of the gate, gate dielectric, and CNT layer in both the A-Metal and C-Metal devices was characterized using atomic force microscopy (AFM). The results show that the root-mean-square roughness (R_q) values for the gate, gate dielectric, and CNT layer in the A-Metal devices are 0.46 nm, 0.52 nm, and 1.51 nm, respectively (Figures 2(c-e)), compared with 0.77, 0.79, and 1.69 nm for the C-Metal devices (Figures 2(f-h)). These data confirm that the A-Metal gate possesses superior surface smoothness. Moreover, the HfO_2 surface roughness inherits the initial gate morphology, indicating a geometric morphology transfer effect, and the ~ 13 nm layer cannot fully planarize the larger roughness of the C-Metal gate.

2.3 Electrical Characterization of CNT-TFTs

As shown in Figure 3(a), the transfer characteristics of both A-Metal and C-Metal devices at $V_{ds} = -0.1$ V and -4.1 V are presented. We characterized the electrical parameters of 20 randomly sampled devices each for the C-Metal and A-Metal structures, from a $35 \text{ mm} \times 35 \text{ mm}$ area. The resulting histograms, which illustrate the performance variability, are presented in Figures 3(b-e).

The hysteresis voltage, a direct indicator of device stability and interface trap density, is defined as the difference in gate voltage at a fixed drain current of 10^{-8} A between the forward and reverse gate voltage sweeps. The curves in Figure 3(a) clearly reveal significantly smaller hysteresis in the A-Metal device compared to its C-Metal counterpart. The results in Figure 3b show that the hysteresis voltage of the A-Metal device (0.46 ± 0.04 V) is significantly reduced by approximately 50% compared to that of the C-Metal device (0.91 ± 0.02 V). The substantial reduction in hysteresis voltage demonstrates that charge trapping is markedly reduced in the amorphous metal gate device, which underpins its superior performance compared to the C-Metal device.

Although both devices achieve high on/off ratios ($>10^6$), the A-Metal device nonetheless exhibits superior performance in key metrics compared to the C-Metal control (Figures 3(b-e)). In particular, the A-Metal devices achieve higher field-effect mobility (7.48 ± 0.42) compared to (6.40 ± 0.45) $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ for the C-metal at $V_{ds} = -0.1$ V. A-Metal devices also demonstrate superior on/off ratio and on-state current.

Furthermore, as the surface roughness of the dielectric film

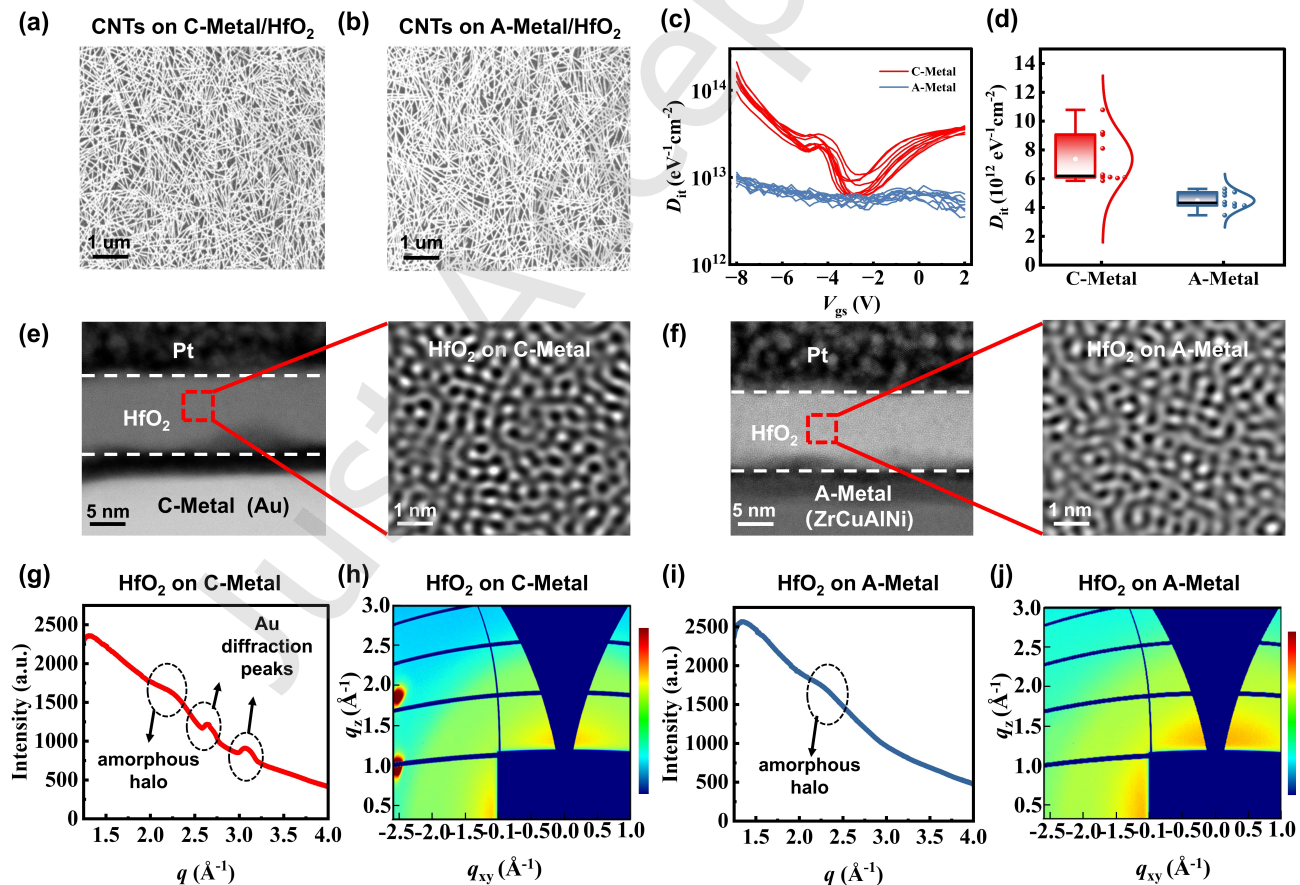


Figure 4. Microstructural characterization of CNT-TFTs with C-Metal and A-Metal gates. (a, b) SEM images showing carbon nanotube density for C Metal and A-Metal devices, respectively. (c) Interface trap density vs. gate voltage for C-Metal and A-Metal devices, extracted from 10 devices per group (d) The distribution of minimum interface defect density on each curve in (c). (e, f) Corresponding spherical aberration-corrected TEM images for C Metal and A-Metal devices, respectively. (g) One-dimensional GIWAXS integration profile for the C-Metal device. (h) Two-dimensional GIWAXS pattern for the C-Metal device plotted against the scattering vector q . The color bar represents the signal intensity, ranging from blue (weak) to red (strong). (i) One-dimensional GIWAXS integration profile for the A-Metal device. (j) Two-dimensional GIWAXS pattern for the A-Metal device plotted against the scattering vector q . The color bar represents the signal intensity, ranging from blue (weak) to red (strong).

critically affects leakage current[38], a comparison of the transfer characteristics in Figure 3(a) reveals a lower gate leakage current (I_{gs}) for the A-Metal device relative to the C-Metal device, indicating a superior quality of the gate dielectric film.

2.4 Analysis of Interface Traps

To elucidate the physical origin of the reduced hysteresis voltage, a thorough interface analysis was conducted. In top-gate devices, the roughness of the substrate is known to affect the uniformity of the deposited carbon nanotube film and consequently the performance of CNT-TFTs[25]. The corresponding characterization results are shown in Figures 4(a, b). To exclude the potential influence of channel material variations, we first investigated the density of CNT film. Scanning electron microscopy (SEM) images revealed a similar carbon nanotube density of approximately 20 tubes/ μm for both devices. In contrast to the previous report showing that substrate roughness affects carbon nanotube film uniformity in top-gate devices, we found that gate roughness does not influence the density of the carbon nanotube layer. Therefore, the observed electrical performance variations cannot be attributed to differences in CNT film density.

Subsequently, metal-oxide-semiconductor capacitor (MOSCAP) based on the identical HfO_2/CNT structure were fabricated as shown in Figure S3. Interface trap densities (D_{it}) were quantitatively extracted using high-low frequency capacitance-voltage ($C-V$) measurements[39]. Figure 4(c) demonstrates the extracted interface trap densities (D_{it}) from 10 devices for each group, using the method described therein. The statistical distribution of minimum D_{it} values on each curve is shown in Figure 4(d). The average minimum D_{it} for the A-Metal devices is $4.47 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$, representing a 39.27% reduction compared to the value of

$7.36 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ for the C-Metal devices.

The subthreshold swing (SS) values of devices with A-Metal and C-Metal gate electrodes are also extracted, as SS is a sensitive indicator of interfacial quality. The average SS values are 239.4 mV/dec for A-Metal devices, and 233.5 mV/dec for C-Metal devices, as shown in Figure S4. The negligible change in SS despite a significant reduction in D_{it} suggests that SS in the present CNT-TFTs is not solely determined by interface traps, but is dominated by other effects, for example, percolation-based transport and Schottky contacts. Nevertheless, the reduced hysteresis and D_{it} of the A-metal device still indicate a substantial improvement in interface quality.

Furthermore, we employed spherical aberration-corrected Transmission Electron Microscopy (TEM) to characterize the microstructure of the HfO_2 dielectric layers. The analysis confirms that the HfO_2 layers in both device (C-Metal and A-Metal) types retain an amorphous structure, as shown in Figures 4(e, f), the amorphous nature of the hafnium oxide (HfO_2) was also confirmed by high-resolution transmission electron microscopy (HRTEM), as shown in Figure S2. Regarding the metal electrodes, given the limited field of view in TEM imaging, we observed that the C-Metal film consists of large grains with a strong (111) texture. Large-area GIWAXS scanning reveals the presence of different crystallographic planes in C-Metal and confirms its polycrystalline nature. The grazing-incidence wide-angle X-ray scattering (GIWAXS) characterization further elucidates the structural differences between the C-Metal and A-Metal devices. As shown in Figures 4(g-j), the HfO_2 layer serving as the gate dielectric in both devices exhibits an amorphous state, consistent with prior TEM analysis. The absence of structural differences in the HfO_2 layer between the two device types confirms that contact with different gate metals

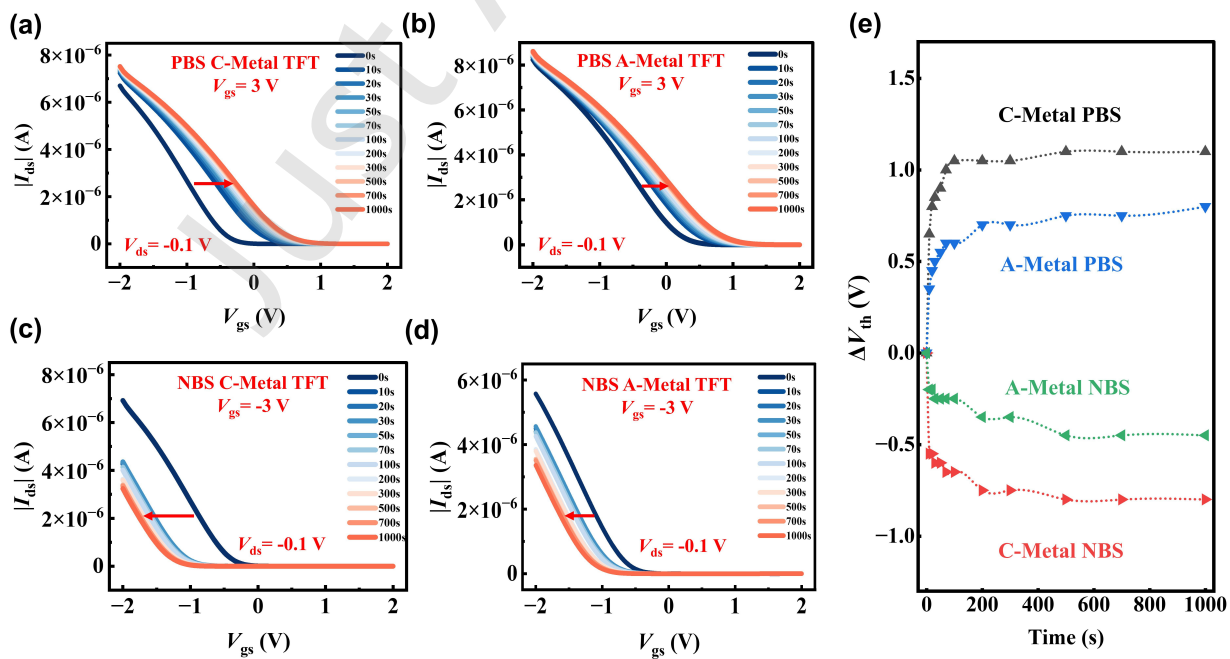


Figure 5. Bias stress instability of C-Metal and A-metal devices. (a, b) The transfer curves of C-Metal and A-Metal devices under PBS, respectively. (c, d) The transfer curves of C-Metal and A-Metal devices under NBS, respectively. (e) Threshold voltage shift with time for A-Metal and C-Metal device under NBS and PBS conditions.

does not induce crystallization or grain formation in HfO_2 , thereby excluding this as a contributing factor to the performance disparity.

Based on all the analysis above, we propose that the improvement in HfO_2/CNT interface quality achieved with the amorphous metal gate results from the combined effect of the geometric morphology transfer effect and the chemical nucleation kinetics improvement effect. Our devices employ a bottom-gate configuration. In this structure, the initial ALD nucleation of HfO_2 takes place at the metal/ HfO_2 bottom interface, while the D_{it} extracted from transistor characteristics mainly reflects trap states electrically coupled to the CNT channel, particularly those located at or near the CNT/HfO_2 top interface.

1) Regarding the geometric morphology-transfer effect, even without considering possible differences in the microscopic quality of the HfO_2 film, a smoother HfO_2 top surface may reduce the effective trap density sensed by the CNT channel. A rough HfO_2 surface may lead to non-uniform physical contact between the CNT network and the dielectric, together with a larger effective surface area, more nanoscale valleys, and more adsorption sites. These features can more readily retain moisture, oxygen, hydroxyl groups, or processing residues, which are particularly important for CNT channels and can serve as charge trapping/detrapping centers[40, 41]. Therefore, the smoother HfO_2 top surface inherited from the amorphous metal gate can reduce the trap-assisted charge storage at the CNT/HfO_2 interface.

2) For the ALD nucleation effect, its influence on D_{it} is expected to be more indirect in bottom-gate devices. Previous studies have shown that the spatial uniformity of adsorption sites governs the uniformity of the adsorbate layer and the subsequent film morphology[42, 43]. Therefore, more uniform initial growth on the amorphous metal gate may improve the overall dielectric quality, reducing bulk traps, border traps, density variations, and local thickness non-uniformity. These dielectric imperfections can contribute to charge trapping responses sensed by the CNT channel and thus affect the extracted D_{it} .

2.5 Analysis of Stability

Negative bias instability (NBI) and Positive bias instability (PBI) are key reliability concerns for transistors. The stability of the threshold voltage (V_{th}) is critical to the reliable operation of transistors in both flat-panel displays and integrated circuit chips, as significant V_{th} drift can lead to circuit timing failures and increased power consumption. This phenomenon is physically associated with mechanisms including: carrier trapping/de-trapping, interface state generation, and, in certain dielectric systems, mobile ion migration. Consequently, pronounced V_{th} drift represents a multi-mechanism reliability challenge that necessitates a coordinated analysis of PBI and NBI, alongside the intrinsic material and structural properties of the device.

We extracted the V_{th} by using the constant current method from the turn-on branch (from off-state to on-state). The statistical results show that the average V_{th} of the C-Metal devices and A-Metal devices are 0.84 V and 0.80 V, respectively (as shown in the Figure S5). Therefore, both device types have similar starting points for V_{th} shift.

Subsequently, we evaluated the NBI and PBI of C-Metal and A-Metal devices. As shown in Figures 5(a-d), representative transfer curves of the driving CNT-TFTs are presented under negative ($V_{gs} = -3$ V) and positive ($V_{gs} = +3$ V) bias stress (NBS and PBS) for over 1000 s. The transfer curves were measured intermittently at $V_{ds} = -0.1$ V using a semiconductor parameter analyzer in fast I-V mode to minimize interruption of the bias. As illustrated in Figure 5(e), under PBS, V_{th} shifts positively, whereas under NBS, V_{th} shifts negatively, reflecting electron trapping and detrapping, respectively. The relative V_{th} shifts ($\Delta V_{th} = V_{th}(T) - V_{th}(0)$) for the C-Metal devices are -0.8 V and 1.1 V (Figures 5(a, c)), respectively, while those for the A-Metal devices are -0.45 V and 0.8 V (Figures 5(b, d)). The smaller threshold voltage shift under bias stress in devices with A-Metal gates highlights its superior bias-stress stability compared to those with C-Metal gates.

Furthermore, to verify the thermal stability of the A-metal film, we performed an annealing experiment: a 50 nm thick ZrCuAlNi amorphous film was deposited on a blank silicon wafer and subsequently annealed at 300 °C in Ar using a rapid thermal processing (RTP) system. XRD measurements were conducted before and after annealing. As shown in Figure S6 in the Supplementary Information, for the A-metal film before and after annealing, the XRD pattern remains essentially unchanged, with a broad amorphous peak with minimal shift, and no detectable crystalline diffraction peaks. This indicates that the ZrCuAlNi film retains its amorphous structure after 300 °C annealing, confirming its good thermal stability.

It is worth noting that the A-metal devices show a broader distribution in V_{th} than the C-metal devices. For the device size in this work ($W_{ch}/L_{ch} = 100 \mu\text{m}/10 \mu\text{m}$), work-function variations associated with locally different grain orientations in μm -scale should be averaged over the gate electrode. Therefore, the C-metal devices exhibit similar V_{th} across the wafer. In contrast, the effective work function of the quaternary ZrCuAlNi amorphous alloy can be more sensitive to wafer-scale compositional non-uniformity and surface-state variations introduced during sputtering. Such macroscopic variations may broaden the device-to-device V_{th} distribution. This variability is not expected to arise from the amorphous structure itself, but rather from the current deposition uniformity of the multicomponent alloy film[44-46]. In future work, further optimization of the amorphous metal deposition process is needed in order to improve wafer-scale compositional and surface uniformity, thereby reducing V_{th} variation.

3. Conclusions

In summary, this work establishes gate topography as a decisive physical parameter governing interfacial trap formation and electrostatic response in CNT transistors. By employing an ultrasMOOTH amorphous metal gate, we demonstrate that suppressing nanoscale roughness at the gate/dielectric interface effectively reduces hysteresis and bias stress instability while simultaneously enhancing carrier transport. These improvements are directly attributed to a substantial reduction in interface trap density enabled by the formation of a high-quality gate dielectric

interface.

Beyond the specific material system studied here, the physical mechanism revealed provides a general design principle for developing high-performance, high-stability CNT-based electronics and other carbon-based electronic devices. Future studies may extend this gate topography-driven interface engineering strategy to a broader range of materials systems and device architectures, including heterogeneous integration platforms and emerging thin-film electronics.

4. Method

4.1 Preparation of High-Purity Semiconducting Single-Walled CNT Solution

Using the polymer wrapping and extraction method, we prepared a high-purity semiconducting SWCNT solution. Specifically, arc-discharge SWCNTs (Carbon Solutions Inc.) and Poly[9-(1-octyloxy)-9H-carbazole-2,7-diyl] (PC₂) were combined at a 1:1 mass ratio in toluene (1 mg/mL). After thorough sonication to achieve a uniform dispersion, the solution underwent two rounds of centrifugation. The high-purity semiconducting CNT solution was obtained by collecting the final supernatant for subsequent experiments.

4.2 Fabrication of Bottom-Gate CNT-TFTs with A-Metal and C-Metal Gates

The CNT-TFTs were fabricated with a bottom-gate architecture. The process began with patterning the bottom gate and scan electrode on a Si/SiO₂ wafer using either direct laser writing (for micron-scale channel lengths, L_{ch}). Magnetron sputtering deposition was selected to fabricate high-quality metal gate layers. This technique enables the formation of dense, uniform films with smoother surfaces, finer grains, and lower roughness. Additionally, it allows for precise composition control, thereby facilitating the attainment of homogeneous film structures[47, 48]. A 10/50 nm Ti/Au bilayer was deposited via magnetron sputtering to form the conventional metal (C-Metal) gate, while a 10/50 nm Ti/Zr₅₅Cu₃₀Al₁₀Ni₅ bilayer was deposited via magnetron sputtering to form the amorphous metal (A-Metal) gate. Both metal stacks were patterned using a standard lift-off process. Followed by the uniform deposition of a hafnium oxide (HfO₂) gate dielectric layer by atomic layer deposition (ALD) in the same process on A-Metal and C-Metal, resulting in very similar physical thicknesses of 12.79 nm and 13.19 nm, respectively, as measured from high-resolution transmission electron microscopy (HRTEM) images, as shown in the Figure S2. A carbon nanotube network film was formed by immersing the substrate in the prepared high-purity semiconducting SWCNT solution for 30 minutes. The substrate was subsequently rinsed with toluene and isopropyl alcohol (IPA), followed by thermal annealing at 200 °C for 1 hour under a nitrogen atmosphere. To define the active channel region, oxygen plasma etching (100 W, 100 sccm) was employed to remove CNTs outside the designated areas, while the channel region was protected by photoresist. The photoresist was then stripped using an NMP-based remover. Contact holes (vias) were patterned and etched using a 6:1 buffered oxide etch (BOE) solution for 90 seconds to expose the underlying gate metal electrodes.

Finally, the source/drain contacts were patterned via direct laser writing (DLW). A 0.3/100 nm Ti/Pd bilayer was deposited as the contact metal by EBE and defined by lift-off, completing the fabrication of the CNT-TFTs.

Electronic Supplementary Material: Supplementary material (Supplementary Figure 1 showing the elemental mapping results obtained using EDS; Supplementary Figure 2 showing the schematic MOSCAP structures for two devices of the C-Metal and A-Metal devices; Supplementary Figure 3 showing the HRTEM analysis of the C-Metal and A-Metal devices.) is available in the online version of this article at <https://doi.org/10.26599/NR.2026.94909014>.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and/or the Electronic SupplementaryMaterial. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

All the contributing author(s) report(s) no conflict of interests in this work.

Author contribution statement

J.K. conceived the idea and supervised the research. Y.Y. fabricated the devices, performed topography and electrical measurements, and analyzed the data. A.Z. provided process guidance. S.Y. and Y.X. characterized the crystalline phase of the dielectric layer. Y.Z. (Zhou), Y.G., Y.K., K.H., and Y.L. assisted with the electrical characterization of the devices. Y.Z. (Zhang) designed the wafer layouts. The manuscript was written with contributions from all authors, and all authors approved the final version of the manuscript.

Informed consent

Not applicable.

Ethics statement

Not applicable.

Use of AI statement

None.

References

- [1] Liang, X.;Xia, J.;Dong, G.;Tian, B.; Peng, I. Carbon Nanotube Thin Film Transistors for Flat Panel Display Application. *Topics in Current Chemistry* **2016**, *374*, 80.
- [2] Dong, G.;Zhao, J.;Shen, L.;Xia, J.;Meng, H.;Yu, W.;Huang, Q.;Han, H.;Liang, X.; Peng, L. Large-area and highly uniform carbon nanotube film for high-performance thin film transistors. *Nano Research* **2018**, *11*, 4356-4367.
- [3] Yang, Y.;Ding, L.;Han, J.;Zhang, Z.; Peng, L.-M. High-Performance Complementary Transistors and Medium-Scale Integrated Circuits Based on Carbon Nanotube Thin Films. *ACS Nano* **2017**, *11*, 4124-4132.
- [4] Peng, L.-M. High-Performance Carbon Nanotube Thin-Film Transistor Technology. *ACS Nano* **2023**, *17*, 22156-22166.

- [5] Li, S.; Yin, Z.; Li, Y.; Dong, X.; Luo, T.; Xi, M.; Bai, L.; Cao, X.; Liang, X.; Cao, Y. Dielectric and passivation layer optimization in carbon nanotube thin-film transistors for display driving applications. *Carbon* **2025**, *237*, 120154.
- [6] Zhang, J.; Fu, Y.; Wang, C.; Chen, P.-C.; Liu, Z.; Wei, W.; Wu, C.; Thompson, M. E.; Zhou, C. Separated Carbon Nanotube Macroelectronics for Active Matrix Organic Light-Emitting Diode Displays. *Nano Letters* **2011**, *11*, 4852-4858.
- [7] Li, Y.; Guo, Y.; Li, J.; Xi, M.; Bai, L.; Zhang, J.; Li, S.; Zhu, X.; He, Y.; He, B.; Chen, X.; Zhang, Y.; Gong, Y.; Yin, Z.; Kang, J.; Peng, L.-M.; Zhang, R.; Zhou, Y.; Cao, Y.; Liang, X. Micro-LED Microdisplays Driven by Carbon Nanotube Active-Matrix Backplanes. *ACS Nano* **2025**, *19*, 22837-22848.
- [8] Xi, M.; Liu, F.; Zhu, X.; Li, Y.; Bai, L.; Chen, X.; Gong, Y.; Guo, Y.; Zhou, Y.; Peng, L.; Kang, J.; Cao, Y.; Liang, X. High-performance thin-film transistors based on aligned carbon nanotubes for mini- and micro-LED displays. *Carbon* **2024**, *218*, 118718.
- [9] Hirotani, J.; Ohno, Y. Carbon Nanotube Thin Films for High-Performance Flexible Electronics Applications. *Topics in Current Chemistry* **2019**, *377*, 3.
- [10] Huang, Q.; Xi, M.; Liu, F.; Lu, T.; Liang, X. Charge trapping in carbon nanotube thin film transistors and its suppression. *Carbon* **2026**, *247*, 121035.
- [11] Zheng, A.; Gong, Y.; Liu, D.; He, K.; Zhang, Y.; Wang, T.; Kai, Y.; Lin, P.; Lyu, L.; Liang, X.; Cao, Y.; Hu, Y.; Peng, L.-M.; Kang, J. Wafer-Scale Heterogeneous Integration of High-Resolution Micro-LED Displays with Carbon Nanotube Thin-Film Transistors. *ACS Nano* **2026**, *20*, 5297-5308.
- [12] Han, S.-J.; Tang, J.; Kumar, B.; Falk, A.; Farmer, D.; Tulevski, G.; Jenkins, K.; Afzali, A.; Oida, S.; Ott, J.; Hannon, J.; Haensch, W. High-speed logic integrated circuits with solution-processed self-assembled carbon nanotubes. *Nature Nanotechnology* **2017**, *12*, 861-865.
- [13] Shulaker, M. M.; Hills, G.; Patil, N.; Wei, H.; Chen, H.-Y.; Wong, H. S. P.; Mitra, S. Carbon nanotube computer. *Nature* **2013**, *501*, 526-530.
- [14] Hills, G.; Lau, C.; Wright, A.; Fuller, S.; Bishop, M. D.; Srimani, T.; Kanhaiya, P.; Ho, R.; Amer, A.; Stein, Y.; Murphy, D.; Arvind; Chandrakasan, A.; Shulaker, M. M. Modern microprocessor built from complementary carbon nanotube transistors. *Nature* **2019**, *572*, 595-602.
- [15] Liu, Y.; Ding, S.; Li, W.; Zhang, Z.; Pan, Z.; Ze, Y.; Gao, B.; Zhang, Y.; Jin, C.; Peng, L.-M.; Zhang, Z. Interface States in Gate Stack of Carbon Nanotube Array Transistors. *ACS Nano* **2024**, *18*, 19086-19098.
- [16] Doherty, J. L.; Smith, B. N.; Albarghouthi, F. M.; Vazquez-Perez, R.; Franklin, A. D. Evaluating Uniformity, Contact Geometries, and Size Scaling in Carbon Nanotube Thin-Film Transistors. *ACS Nano* **2025**, *19*, 32335-32349.
- [17] Brown, A. R.; Idris, N. M.; Watling, J. R.; Asenov, A. Impact of Metal Gate Granularity on Threshold Voltage Variability: A Full-Scale Three-Dimensional Statistical Simulation Study. *IEEE Electron Device Letters* **2010**, *31*, 1199-1201.
- [18] Xia, J.; Dong, G.; Tian, B.; Yan, Q.; Zhang, H.; Liang, X.; Peng, L. Metal contact effect on the performance and scaling behavior of carbon nanotube thin film transistors. *Nanoscale* **2016**, *8*, 9988-9996.
- [19] Xiao, H.; Liu, Y.; Ding, S.; Gao, Y.; Zhai, M.; Liang, X.; Jin, C.; Liu, H.; Zhang, Z. Interface and Border Traps in the Gate Stack of Carbon Nanotube Film Transistors with an Yttria Dielectric. *ACS Applied Electronic Materials* **2023**, *5*, 3908-3916.
- [20] Zhao, Y.; Huo, Y.; Xiao, X.; Wang, Y.; Zhang, T.; Jiang, K.; Wang, J.; Fan, S.; Li, Q. Inverse Hysteresis and Ultrasmall Hysteresis Thin-Film Transistors Fabricated Using Sputtered Dielectrics. *Advanced Electronic Materials* **2017**, *3*, 1600483.
- [21] Qin, L.; Deng, X.; Tao, J.; Zhang, S. P-1.14: The Influence of Bottom gate Dielectric Roughness on the Performance of Double-Gate a-IGZO Thin Film Transistors. *SID Symposium Digest of Technical Papers* **2019**, *50*, 677-680.
- [22] Lin, X.; Jin, J.; Kim, J.; Xin, Q.; Zhang, J.; Song, A. Effects of gate roughness on low voltage InGaZnO thin-film transistors with ultra-thin anodized AlxOy dielectrics. *Semiconductor Science and Technology* **2023**, *38*, 035023.
- [23] Han, J. H.; Lee, S. Y.; Kim, H. E.; Jeon, J.-H.; Park, K.; Moon, K. C.; Im, H.; Kim, Y.-S. Solution-Processed Aluminum-Zirconium Oxide as a Gate Dielectric for InGaZnO Thin Film Transistors. *Journal of Electrical Engineering & Technology* **2024**, *19*, 567-575.
- [24] Geiger, M.; Acharya, R.; Reutter, E.; Ferschke, T.; Zschieschang, U.; Weis, J.; Pflaum, J.; Klauk, H.; Weitz, R. T. Effect of the Degree of the Gate-Dielectric Surface Roughness on the Performance of Bottom-Gate Organic Thin-Film Transistors. *Advanced Materials Interfaces* **2020**, *7*, 1902145.
- [25] Ye, H.; Wang, H.; Yu, X.; Yao, Y.; Xiang, L. Evaluation of Influence of Substrate Planarization on the Uniformity of Flexible Carbon Nanotube Thin Film Transistors. *IEEE Transactions on Electron Devices* **2023**, *70*, 5125-5132.
- [26] Zeumault, A.; Mendez, J. E.; Brewer, J. Innovations in thin-film electronics for the new generation of displays. *Journal of the Society for Information Display* **2024**, *32*, 121-135.
- [27] Park, E.-S.; Kim, D.-Y.; Lee, J.-H.; Hwang, J.-U.; Song, Y.-S.; Park, K.-H.; Choi, H.-J. Optical and electrical properties of amorphous alloy metal mesh for transparent flexible electrodes. *Applied Surface Science* **2021**, *547*, 149109.
- [28] Cowell, E. W., 3rd; Alimardani, N.; Knutson, C. C.; Conley, J. F., Jr.; Kesler, D. A.; Gibbons, B. J.; Wager, J. F. Advancing MIM electronics: amorphous metal electrodes. *Adv Mater* **2011**, *23*, 74-78.
- [29] Ouyang, J.; Wongpiya, R.; Deal, M. D.; Clemens, B. M.; Nishi, Y. Amorphized tantalum-nickel binary films for metal gate applications. *Applied Physics Letters* **2015**, *106*, 151903.
- [30] Wongpiya, R.; Ouyang, J.; Chung, C.-J.; Duong, D. T.; Deal, M.; Nishi, Y.; Clemens, B. Structural and electrical characterization of CoTiN metal gates. *Journal of Applied Physics* **2015**, *117*, 075304.
- [31] Matsukawa, T.; Liu, Y. X.; Mizubayashi, W.; Tsukada, J.; Yamauchi, H.; Endo, K.; Ishikawa, Y.; O'Uchi, S.; Ota, H.; Migita, S.; Morita, Y.; Masahara, M. Suppression of threshold voltage variability of double-gate fin field-effect transistors using amorphous metal gate with uniform work function. *Applied Physics Letters* **2013**, *102*, 162104.
- [32] Grubbs, M. E.; Zhang, X.; Deal, M.; Nishi, Y.; Clemens, B. M. Development and characterization of high temperature stable Ta-W-Si-C amorphous metal gates. *Applied Physics Letters* **2010**, *97*, 223505.
- [33] Liu, M.; Cao, C. R.; Lu, Y. M.; Wang, W. H.; Bai, H. Y. Flexible amorphous metal films with high stability. *Applied Physics Letters* **2017**, *110*, 031901.
- [34] Jung, M.; Lee, E.; Kim, D.; Kim, K.; Yun, C.; Lee, H.; Kim, H.; Rhie, K.; Jeon, S. Amorphous FeZr metal for multi-functional sensor in electronic skin. *npj Flexible Electronics* **2019**, *3*, 8.
- [35] Sharma, P.; Kaushik, N.; Kimura, H.; Saotome, Y.; Inoue, A. Nano-fabrication with metallic glass—an exotic material for nano-electromechanical systems. *Nanotechnology* **2007**, *18*, 035302.
- [36] Lee, J.; Duh, J.-G. Structural evolution of Zr-Cu-Ni-Al-N thin film metallic glass and its diffusion barrier performance in Cu-Si interconnect at elevated temperature. *Vacuum* **2017**, *142*, 81-86.
- [37] Jenkins, M. A.; Klarr, T.; Austin, D. Z.; Li, W.; Nguyen, N. V.; Conley Jr, J. F. Assessment of Energy Barriers Between ZrCuAlNi Amorphous Metal and Atomic Layer Deposition Insulators Using Internal Photoemission Spectroscopy. *physica status solidi (RRL) – Rapid Research Letters* **2018**, *12*, 1700437.
- [38] Kim, S.; Kim, W.-Y.; Im, H.; Kim, Y.-S. Effect of hydrochloric acid addition on dielectric properties of solution-processed aluminum titanium oxide thin film annealed at low temperature. *Thin Solid Films* **2022**, *753*, 139277.
- [39] Castagné, R.; Vapaille, A. Description of the SiO₂/Si interface properties by means of very low frequency MOS capacitance measurements. *Surface Science* **1971**, *28*, 157-193.
- [40] Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors. *Nano Letters* **2003**, *3*, 193-198.
- [41] Lu, Y.-X.; Lin, C.-T.; Tsai, M.-H.; Lin, K.-C. Review-Hysteresis in Carbon Nano-Structure Field Effect Transistor. In *Micromachines*, 2022; pp 509.

- [42] Premkumar, P. A.; Delabie, A.; Rodriguez, L. N. J.; Moussa, A.; Adelman, C. Roughness evolution during the atomic layer deposition of metal oxides. *Journal of Vacuum Science & Technology A* **2013**, *31*.
- [43] Ding, S.; Liu, Y.; Shang, Q.; Gao, B.; Yao, F.; Wang, B.; Ma, X.; Zhang, Z.; Jin, C. Morphological Evolution of Atomic Layer Deposited Hafnium Oxide on Aligned Carbon Nanotube Arrays. *Nano Letters* **2024**, *24*, 13631-13637.
- [44] Ouyang, J.; Wongpiya, R.; Grubbs, M. E.; Deal, M. D.; Clemens, B. M.; Nishi, Y. Effect of Composition on Structural and Electrical Properties of Amorphous Ta-W-Si-C Metal Thin Films. *ECS Solid State Letters* **2013**, *2*, P86.
- [45] Oleksak, R. P.; Hostetler, E. B.; Flynn, B. T.; McGlone, J. M.; Landau, N. P.; Wager, J. F.; Stickle, W. F.; Herman, G. S. Thermal oxidation of Zr-Cu-Al-Ni amorphous metal thin films. *Thin Solid Films* **2015**, *595*, 209-213.
- [46] Zhu, F.; Zhou, J.; Huang, H.; Wen, W.; Ye, J.; Yan, Z. Microstructure of metallic glasses on a mesoscopic scale: spatial heterogeneity in correlating atomic configurations with macroscopic properties. *Acta Physica Sinica* **2025**, *74*, 166102-166101-166102-166113.
- [47] Zeng, L.; Helgren, E.; Hellman, F.; Islam, R.; Smith, D. J. Growth and microstructure dependence of electronic and magnetic properties in magnetically doped Gd-Si amorphous semiconductors. *Physical Review B* **2007**, *75*, 184404.
- [48] Zheng, W.; Yuan, B.; Villena, M. A.; Zhu, K.; Pazos, S.; Shen, Y.; Yuan, Y.; Ping, Y.; Liu, C.; Zhang, X.; Zhang, X.; Lanza, M. The origin and mitigation of defects induced by metal evaporation in 2D materials. *Materials Science and Engineering: R: Reports* **2024**, *160*, 100831.

Electronic Supplementary Material

Suppressing trap density in carbon nanotube transistors via atomically smooth amorphous metal gates

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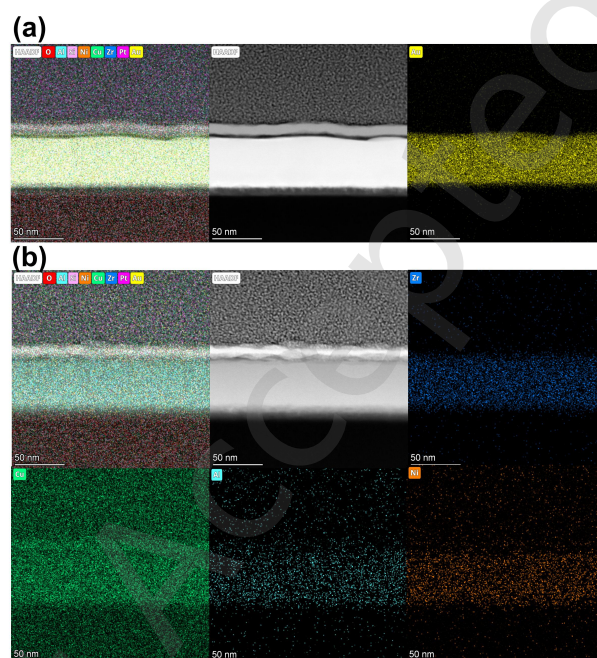


Figure S1. Cross-sectional EDS elemental maps of the C-Metal and A-Metal devices. (a) C-Metal device. (b) A-Metal device. The uniform signal intensity of the elements in the corresponding regions of both devices, as shown in figures (a) and (b), confirms their homogeneous distribution within layer.

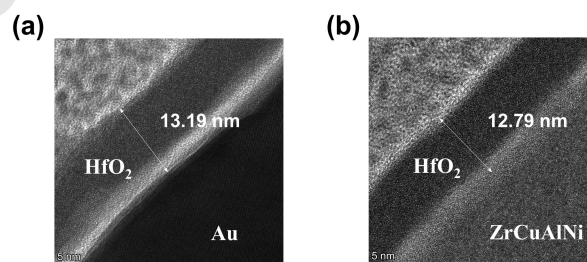


Figure S2. Cross-sectional high-resolution transmission electron microscopy (HRTEM) images: (a) C-Metal device. (b) A-Metal device. The HRTEM images reveal that the hafnium oxide is in an amorphous state in both devices.

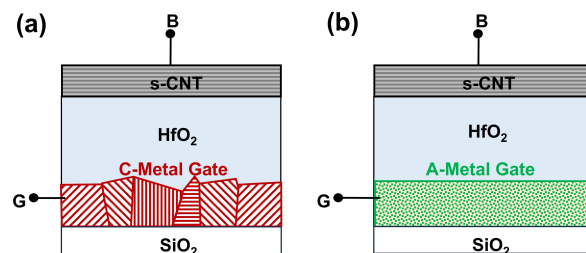


Figure S3. Schematic MOSCAP structures for two devices. (a) C-Metal device. (b) A-Metal device.

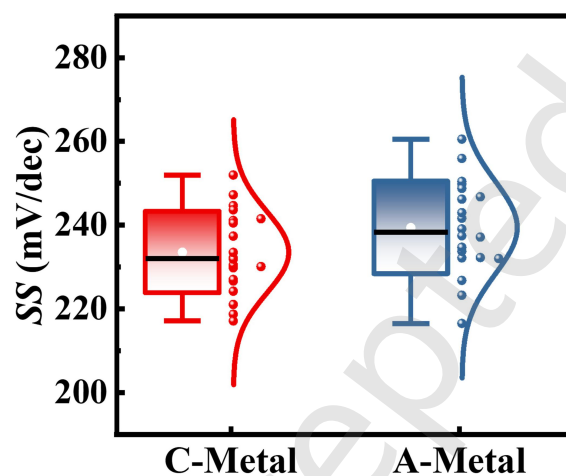


Figure S4. Subthreshold swing (SS) of C-metal and A-metal gate devices.

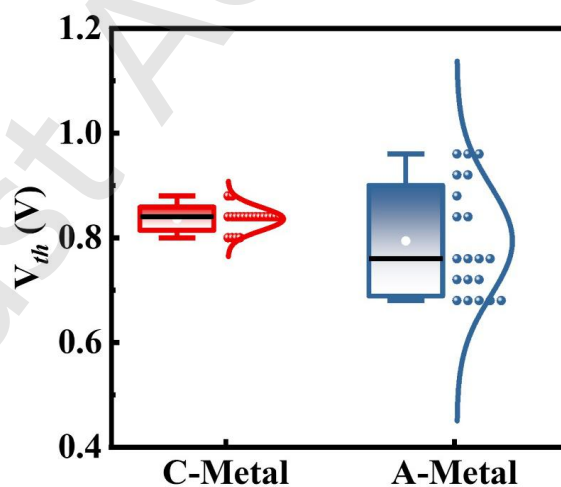


Figure S5. Threshold voltages (V_{th}) of C-metal and A-metal gate devices. V_{th} was extracted using the constant current method normalized by the channel width-to-length ratio (W_{ch}/L_{ch}), specifically defined as the gate voltage at which the drain current (I_{ds}) reaches $(W/L) \times 1$ nA in the transfer characteristic curve (I - V) from off-state to on-state.

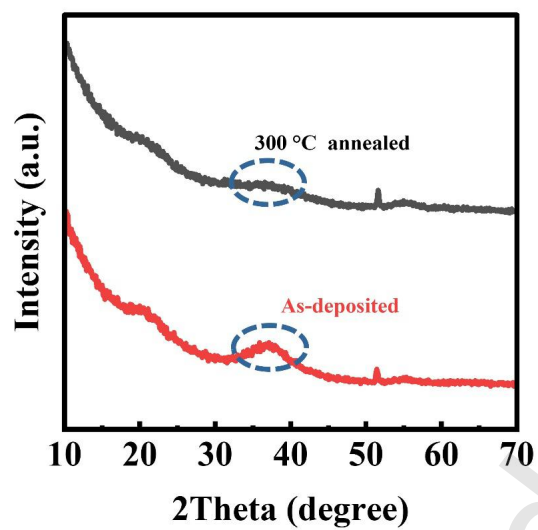


Figure S6. X-ray diffraction (XRD) patterns of A-metal before and after annealing at 300 °C.