

Machine learning-guided process co-optimization of flexible carbon nanotube thin-film transistors for low-voltage digital logic circuits

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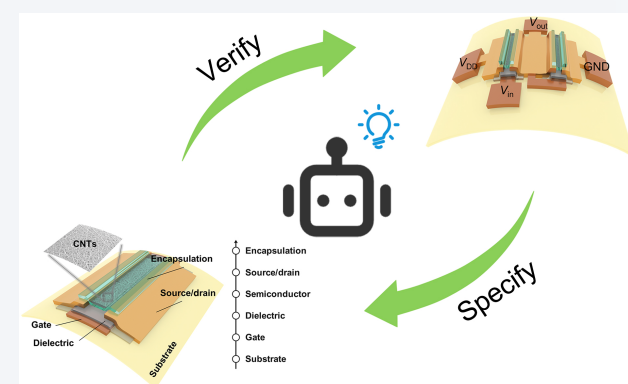
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ABSTRACT: Carbon nanotube thin-film transistors (CNT-TFTs) are promising for flexible electronics, but circuit-oriented optimization remains challenging because reliable logic operation requires a coordinated balance among multiple device metrics, and such a balance is difficult to achieve by one-factor-at-a-time tuning within a coupled multistep fabrication process. Accordingly, process optimization must be target-oriented rather than driven by any single device metric. Here, we develop a machine learning-guided process co-optimization framework for flexible CNT-TFTs and use low-voltage digital logic as a representative use case. A decision-tree model trained on more than 800 devices from 80 fabrication recipes employs a weighted evaluation score that jointly considers extracted field-effect mobility as a proxy for current-drive capability, threshold voltage, drain current at $V_{GS} = 0$ V, subthreshold swing, and on/off ratio. The optimized enhancement-mode CNT-TFTs exhibit extracted field-effect mobilities up to $71 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$, a width-normalized drain current at $V_{GS} = 0$ V as low as $0.2 \text{ pA} \cdot \mu\text{m}^{-1}$, and an on/off ratio of 10^6 . Using inverters as a sensitive unit-level benchmark, we realize 2 V pseudo-PMOS (PMOS = P-channel metal-oxide-semiconductor) inverters with a switching threshold near $V_{DD}/2$, a voltage gain of 60, and noise margins of 36%–42%. The same platform further supports a 5-stage ring oscillator operating at 60 kHz, as well as rail-to-rail basic logic gates and a 1-bit full adder, thereby verifying low-voltage dynamic and cascaded logic operation on flexible CNT-TFTs. These results show that machine learning-guided process co-optimization provides an efficient route for translating circuit requirements into fabrication strategies for flexible CNT logic circuits.

KEYWORDS: carbon nanotube thin-film transistors, machine learning, low-voltage logic, flexible electronics, process co-optimization

1 Introduction

Thin-film transistors (TFTs) are a key device platform for flexible integrated circuits, where low processing temperature and mechanical compliance must be combined with circuit-relevant electrical performance [1–4]. However, existing TFT technologies still involve substantial trade-offs among carrier transport, thermal budget, device stability, and integration complexity. Amorphous silicon TFTs are mature and uniform but mobility-limited [5, 6];



low-temperature polycrystalline silicon (LTPS) offers much higher current drive capability but generally requires a higher thermal budget and more complex integration [7–9]; oxide semiconductors such as indium-gallium-zinc oxide (IGZO) offer good uniformity and relatively low-temperature processing, yet threshold stability and complementary circuit implementation remain challenging [7, 10, 11]; and organic semiconductors are mechanically compliant and solution-processable, but still often sacrifice mobility, bias stability, and reproducibility [12, 13].

Within this landscape, semiconducting carbon nanotube (CNT) networks are particularly attractive because they combine relatively low-temperature processability with high carrier mobility, small parasitic capacitance, and compatibility with flexible substrates [14–16]. Other low-dimensional semiconductors, including MoS_2 and related two-dimensional (2D) materials, have also shown

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strong promise for flexible electronics [17, 18]. Even so, CNT networks remain especially appealing for circuit applications because they can be assembled as thin films [16, 19], incorporated into established fabrication flows, and have already enabled flexible digital [15, 16] and analog circuits [20, 21]. CNT electronics should therefore be viewed not as a speculative emerging concept, but as an increasingly mature thin-film platform whose current bottleneck lies in circuit-oriented process control.

The remaining challenge is not simply to maximize one transistor metric. For low-voltage logic, current-drive capability, threshold control, drain current at $V_{GS} = 0$ V ($I_{D|V_{GS}=0}$), subthreshold swing (SS), and on/off ratio must be balanced simultaneously. In CNT-TFTs, however, these electrical metrics are strongly coupled: Changes in gate-stack design, dielectric growth, CNT pretreatment, contact formation, encapsulation, and post-annealing can improve one aspect of device behavior while perturbing others. This makes conventional one-factor-at-a-time optimization inefficient for circuit-oriented process development. Machine learning (ML) is well suited to this problem because it can learn empirical relationships between multistep fabrication descriptors and multidimensional electrical responses from experimental datasets, enabling data-driven process co-optimization [22, 23].

Here, we develop an ML-guided process co-optimization framework for flexible CNT-TFTs and use low-voltage digital logic as a representative use case. A library of multistep fabrication recipes is combined with a weighted multi-metric evaluation scheme tailored to circuit requirements. The optimized devices are first examined at the inverter level, where switching threshold (V_m), gain, output swing, and noise margin provide a sensitive test of logic robustness, and are then extended to a 5-stage ring oscillator, basic logic gates, and a 1-bit full adder operated at 2 V. In this way, the present study establishes a practical process-to-circuit route for refining CNT-TFT fabrication toward CNT flexible logic.

2 Results and discussion

2.1 ML-assisted process co-optimization

Figure 1(a) shows the bottom-gate flexible CNT-TFT architecture used in this study. The devices were fabricated on polyimide (PI) substrates, and a 5 nm HfO_2 layer was introduced on the PI surface to improve adhesion before gate-stack formation. A randomly oriented semiconducting CNT network was deposited by dip coating on the flexible substrate (Fig. S1 in the Electronic Supplementary Material (ESM)), and the complete fabrication flow is illustrated in Fig. S2 in the ESM and described in

Section 4. Figure 1(b) outlines the general ML workflow used here. Rather than varying one parameter at a time, ML learns empirical relationships between multivariable process descriptors and device responses from data. The workflow comprises dataset construction, division into training and validation sets, model fitting, and prediction based on the learned mapping between input features and output targets. Because different algorithms are suited to different data structures, model selection should follow the characteristics of the dataset [24, 25].

Figure 2(a) details the study-specific ML training pipeline. We first defined a library of multistep fabrication recipes from the stepwise process descriptors summarized in Table S1 in the ESM. Each experimentally implemented recipe was then encoded by discrete process features and paired with the corresponding electrical labels that measured from the fabricated device to construct the dataset. The indicator labels, including extracted field-effect mobility (μ_{eff}), threshold voltage (V_{th}), $I_{D|V_{GS}=0}$, SS, and on/off ratio, serve as circuit-relevant electrical readouts of device response. The complete dataset comprised more than 800 devices fabricated using 80 recipes and was divided into training and test subsets in a ratio of 80%/20%. These recipes were constructed by systematically varying discrete process descriptors around a baseline process, and the complete recipe-construction matrices are provided in Tables S2–S7 in the ESM. Because the descriptors are predominantly discrete, a decision-tree (DT) model [22, 24] was adopted to learn the empirical relationship between fabrication recipes and circuit-relevant electrical metrics. In the original implementation, the decision-tree-based model was constructed as a random forest ensemble consisting of 50 individual decision trees, rather than a single decision tree, to improve prediction robustness and reduce overfitting risk. The model was trained using only the training subset, while the held-out test subset was used to evaluate prediction performance on unseen samples.

Figure 2(b) plots V_{th} versus extracted μ_{eff} for the CNT-TFTs. Unless otherwise stated, the device channel dimensions presented in this work are $W/L = 50/5$ μm , where W and L denote the channel width and channel length, respectively. Here, the extracted μ_{eff} is used not as an intrinsic material constant, but as a normalized device-level proxy for current-drive capability under fixed geometry. The data are bounded by a characteristic guide line, denoted here as the ambipolar boundary. This boundary is an experimentally observed envelope rather than a strict mathematical limit. It originates from the ambipolar transport behavior of CNT-TFTs. Owing to the narrow bandgap of the relatively large-diameter CNTs used in this work, approximately 0.41 eV, and the presence of electron-injection barriers associated with the Pd or Ti contact

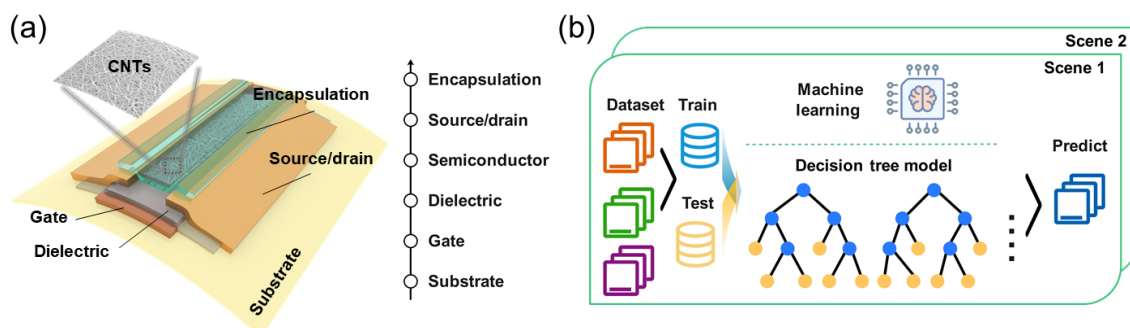


Figure 1 Schematic and machine-learning framework for flexible CNT-TFTs. (a) Schematic illustration of the bottom-gate flexible CNT-TFT architecture used in this work. (b) General workflow of the machine learning process used here.

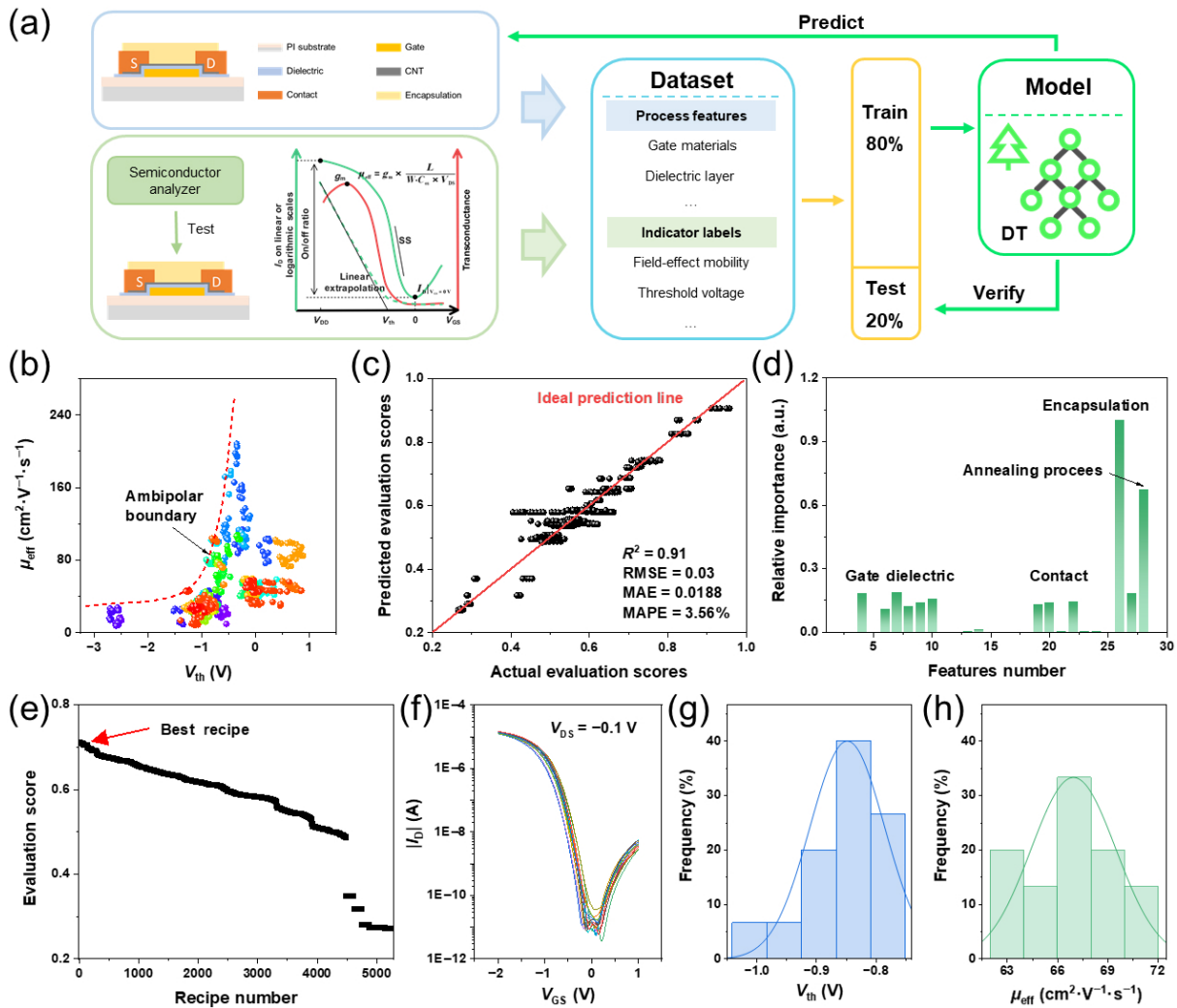


Figure 2 Machine learning-assisted optimization of flexible CNT-TFT fabrication processes. (a) Study-specific ML training workflow. (b) Plot of V_{th} versus μ_{eff} for over 800 CNT-TFT devices, where each color represents a distinct fabrication recipe. Unless otherwise stated, the device geometry is $W/L = 50/5 \mu m$. (c) Correlation between predicted and actual evaluation scores, with R^2 , RMSE, MAE, and MAPE labeled. (d) Process-feature relative importance plot of the trained DT model. (e) Evaluation score distribution of 5280 fabrication recipes obtained via grid search optimization. (f) Transfer characteristics, (g) V_{th} statistical histograms, and (h) μ_{eff} statistical histograms for 15 representative CNT-TFTs.

metals, electron injection becomes increasingly pronounced as V_{th} shifts towards more negative values. The resulting coexistence and competition between electron and hole transport limit the apparent increase in the extracted hole field-effect mobility, giving rise to the observed boundary. It should be emphasized that V_{th} and μ_{eff} do not share a direct causal relationship; instead, both are jointly determined by the fabrication recipe. Therefore, the V_{th} - μ_{eff} distribution identifies an optimum process window in which high extracted mobility is retained while V_{th} remains suitable for enhancement-mode pseudo-PMOS (PMOS = P-channel metal-oxide-semiconductor) operation. To reflect circuit requirements, we defined a weighted evaluation score as the ML training target: 40% for μ_{eff} , 20% for V_{th} , 20% for $I_{D|V_{GS}=0V}$, 10% for SS, and 10% for on/off ratio. μ_{eff} received the highest weight because, for devices with identical geometry, it provides a compact proxy for drive current and switching speed, whereas V_{th} and $I_{D|V_{GS}=0V}$ were emphasized because they directly affect switching-point placement and zero-bias residual conduction in pseudo-PMOS CNT logic. SS and on/off ratio were retained as complementary indicators of electrostatic control and off-state suppression.

As shown in Fig. 2(c), the predicted evaluation scores closely follow the actual values and cluster near the ideal prediction line, indicating that the DT model captures the relationship between fabrication descriptors and the circuit-oriented evaluation score with good fidelity. The model yields a coefficient of determination (R^2) = 0.91, root mean square error (RMSE) = 0.03, mean absolute error (MAE) = 0.0188, and mean absolute percentage error (MAPE) = 3.56%. In addition, 10-fold cross-validation was performed as part of the original model evaluation, yielding an average cross-validated R^2 of 0.89 and only a difference of 0.015 between the training RMSE and the cross-validated RMSE. These results, together with the learning curve analysis shown in Fig. S3 in the ESM, confirm the stable generalization capability of the model for unseen samples and alternative process combinations within the investigated process space. The feature-importance analysis in Fig. 2(d) identifies encapsulation and the subsequent annealing step as the most influential variables in the present model, highlighting post-fabrication steps as key factors in the optimization of CNT-TFT performance. Guided by the trained model, we then carried out grid-search-based co-optimization of

the entire process flow, as illustrated in Fig. 2(e). Here, the grid search refers to exhaustive recipe screening over the predefined discrete process space, rather than hyperparameter optimization of the machine-learning model. The optimized fabrication recipe identified by the weighted evaluation score provided a favorable balance of high extracted field-effect mobility and low $I_{\text{D}}|_{V_{\text{GS}}=0\text{ V}}$, together with a suitable threshold voltage for pseudo-PMOS inverter. More details about the determination of the evaluation score, grid-search enumeration, and recipe-screening procedure are provided in Note S1 in the ESM.

Enhancement-mode CNT-TFTs fabricated using the selected recipe, which is detailed in Table S1 in the ESM, exhibit the transfer characteristics shown in Fig. 2(f). The optimized devices display an on/off current ratio of 10^6 and a width-normalized $I_{\text{D}}|_{V_{\text{GS}}=0\text{ V}}$ as low as $0.2\text{ pA}\cdot\mu\text{m}^{-1}$. Statistical results from 15 representative devices show that V_{th} is centered at about $-0.84 \pm 0.062\text{ V}$ and that the extracted μ_{eff} follows a narrow Gaussian-like distribution with a mean value of $66.95 \pm 2.52\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and a maximum of $71\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, as summarized in Figs. 2(g) and 2(h). The extracted mobility was calculated from $\mu_{\text{eff}} = g_{\text{m}} \times (L/W) \times (1/C_{\text{ox}}) \times (1/V_{\text{DS}})$, where g_{m} is the transconductance, and the areal capacitance density $C_{\text{ox}} = 5.2 \times 10^{-3}\text{ F}\cdot\text{m}^{-2}$ was obtained from direct C-V measurements at 1 MHz (Fig. S4 in the ESM). The devices also maintained stable operation under bending, as shown in Fig. S5 in the ESM. These results establish the optimized enhancement-mode CNT-TFTs as the device platform for subsequent inverter and logic-circuit demonstrations.

2.2 CNT-TFT inverters for low-voltage logic

We first used the inverter as a unit-level benchmark to determine whether ML-guided process co-optimization could be translated from device metrics into circuit behavior. In digital logic, the rail-to-rail output capability and noise margin of an inverter directly determine the cascading capability and noise tolerance, while the voltage gain is also important for signal restoration. Figure 3(a)

shows the schematic of the pseudo-PMOS inverter with zero- V_{GS} load topology [26, 27] used in this work, in which the load transistor is biased at $V_{\text{GS}} = 0\text{ V}$. Before selecting the zero- V_{GS} -load configuration, we experimentally compared four representative unipolar inverter topologies: resistive-load, zero- V_{GS} -load, diode-connected-load, and AC-coupled-load inverters, under identical device dimensions ($W/L = 50/5\text{ }\mu\text{m}$ for both driving and load transistors; 2 pF coupling capacitor for AC-coupled load) (Fig. S6 in the ESM). From these comparisons, the zero- V_{GS} -load inverter provided the best compromise between output swing, voltage gain, and transient response while maintaining a compact layout. Although the load current is limited and asymmetric rise/fall time can occur in unoptimized devices, this topology offers the most suitable platform for benchmarking process-optimized CNT-TFTs. Figure 3(b) presents the optical micrograph and corresponding circuit topology of a representative inverter. Unless otherwise stated, the channel width and length of both CNT-TFTs are 50 and $5\text{ }\mu\text{m}$, respectively.

In conventional geometric regulation, the switching threshold voltage V_{m} of the pseudo-PMOS inverter is tuned by adjusting the effective driving strength, i.e., the current-driving capability, of the load transistor relative to that of the driving transistor. Here, this regulation is quantified by the geometric ratio $R = (W/L)_{\text{M2}}/(W/L)_{\text{M1}}$, where M2 is the load transistor and M1 is the driving transistor. In this work, R was tuned by scaling W of the load transistor while keeping L fixed. The mechanism can be understood from the schematic load-line analysis in Figs. 3(c) and 3(d). Under a fixed fabrication process, increasing R raises the load current and shifts V_{m} toward lower input voltage. As shown in Fig. 3(c), the load curves evolve from load I to load III as the load-transistor strength increases. The corresponding current-balance condition between M1 and M2 moves the inverter voltage transfer curves (VTCs) from curve I to curve III in Fig. 3(d). For CNT-TFTs fabricated using the unoptimized recipe, however, this geometry-regulation strategy causes a pronounced trade-off in output

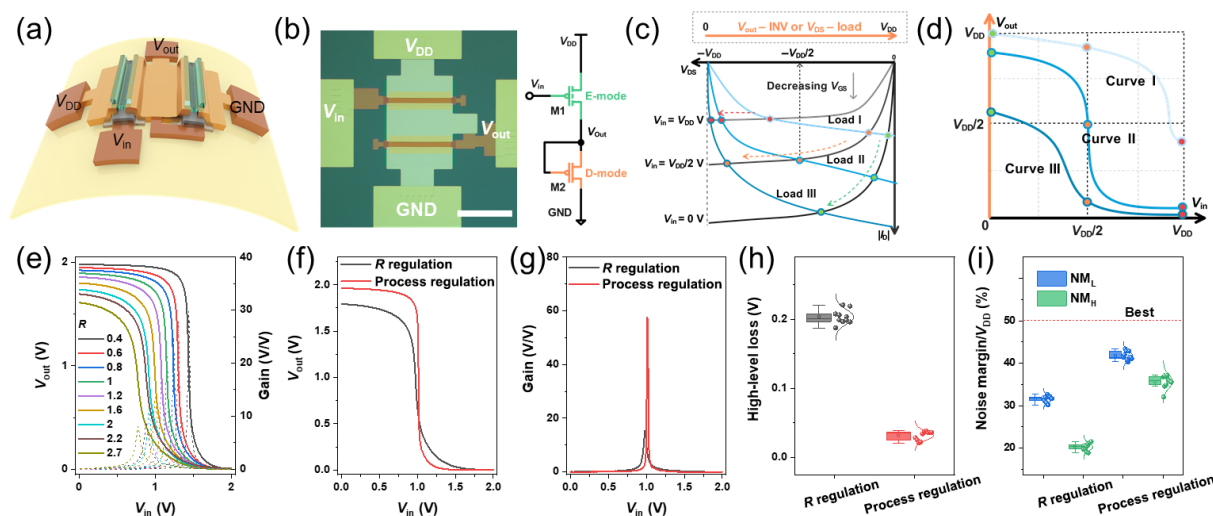


Figure 3 Optimization of inverters based on CNT-TFTs. (a) Schematic of the pseudo-PMOS inverter with the load transistor biased at $V_{\text{GS}} = 0\text{ V}$. (b) Optical micrograph (left) and corresponding circuit topology (right) of a representative inverter. The enhancement-mode and depletion-mode CNT-TFTs are represented by broken/dashed and continuous/solid channel symbols, respectively, with green and yellow colors used as visual guides. Scale bar: $50\text{ }\mu\text{m}$. (c) Schematic load-line illustration of the pseudo-PMOS inverter under increasing load-transistor strength. Loads I, II, and III represent progressively larger effective load currents. INV: inverter. (d) Corresponding schematic VTC shift from curve I to curve III, obtained from the intersection points between the current curves of driving transistor M1 and load transistor M2. (e) R regulation using the geometric ratio $R = (W/L)_{\text{M2}}/(W/L)_{\text{M1}}$ to tune the V_{m} of the VTC curve. (f) Comparison of representative voltage-gain curves for the two regulation strategies. (g) Comparison of representative voltage-gain curves for the two regulation strategies. (h) Statistical comparison of high-level output-voltage loss for 10 inverters under the two regulation strategies. (i) Statistical comparison of NM_{H} and NM_{L} for 10 inverters under the two regulation strategies.

performance. Here, “unoptimized” refers to devices fabricated with the depletion-mode recipe listed in Table S1 in the ESM. As shown in Fig. 3(e), when R is increased to 1.6, corresponding to a load-transistor width of 80 μm with M1 fixed at 50/5 μm , V_m can be tuned close to $V_{DD}/2$. The corresponding transient current characteristics of the R -regulated inverters are provided in Fig. S7 in the ESM. At the same time, the high-level output-voltage loss reaches about 0.2 V, which significantly degrades the noise margin and logic cascading capability. This degradation originates from the enhanced load current introduced by increasing R . Although a larger R helps shift V_m toward $V_{DD}/2$, the strengthened zero- V_{GS} load transistor causes stronger current competition at the high output state, so the output voltage is limited by the current balance rather than reaching the ideal V_{DD} . The resulting high-level output loss directly compresses high-level noise margin (NM_H). Moreover, in cascaded operation, a degraded high-level output of about 1.8 V leaves the next-stage p-type driving transistor with an effective V_{GS} of approximately -0.2 V, causing residual conduction and further degradation of the following low-level output. Moreover, the enlarged load transistor introduces a substantial area penalty, indicating that tuning V_m by adjusting W/L is not an optimal strategy for dense logic integration.

To avoid both the area overhead of an oversized load transistor and the output degradation introduced by geometry regulation, we next adopted the process-regulation strategy. In this scheme, the driving transistor M1 was fabricated using the ML-recommended enhancement-mode recipe detailed in Table S1 in the ESM, and the electrical characteristics of the optimized M1 devices are summarized in Figs. 2(f)–2(h). The load transistor M2 was a depletion-mode CNT-TFT fabricated using the unoptimized recipe. The representative depletion-mode load device used here has a V_{th} of 0.25 V and an extracted μ_{eff} of 30 $\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$, consistent with the characteristics of unoptimized devices summarized in Fig. S8 in the ESM. With the geometric ratio fixed at $R = 1$, representative VTCs for the two regulation strategies are compared in Fig. 3(f). To further clarify the origin of the centered switching threshold in the process-regulated inverter, a graphical load-line analysis based on the measured output characteristics of the driver transistor and the measured current–voltage curve of the zero- V_{GS} load transistor is provided in Fig. S9 in the ESM. An enhancement-mode driver and a depletion-mode zero- V_{GS} load with identical dimensions do not automatically yield $V_m \approx V_{DD}/2$; instead, V_m is determined by the current-balance condition between the two transistors. In the process-regulated inverter, the tailored electrical characteristics of the enhancement-mode driver and depletion-mode load allow their current curves to intersect near $V_{DD}/2$, thereby centering the switching threshold without changing the geometric ratio. Although both strategies can place V_m near $V_{DD}/2$, the process-regulated inverter shows a much more complete high-level output and a steeper transition region than the R -regulated inverter, indicating a more favorable transfer characteristic for logic cascading. This difference is further illustrated by the representative noise-margin constructions in Fig. S10 in the ESM, where the reduced output loss and sharper transition of the process-regulated inverter translate into enlarged high-level and low-level noise margins. The corresponding representative gain curves are shown in Fig. 3(g), where the peak gain increases from about 15 to 60.

To evaluate reproducibility, we fabricated and characterized 10 inverters under each regulation strategy. The full sets of VTC and gain curves are provided in Fig. S11 in the ESM, and the statistical

distributions of gain, V_m , and low-level output loss are summarized in Fig. S12 in the ESM. Figure 3(h) compares the statistical high-level output loss, which is reduced from 0.203 ± 0.01 V under R regulation to 0.031 ± 0.006 V under process regulation, corresponding to about 1% of the 2 V operating voltage. Figure 3(i) compares the statistical NM_H and low-level noise margin (NM_L), which are improved from $20\% \pm 0.9\%$ and $32\% \pm 0.7\%$ under R regulation to $36\% \pm 1.5\%$ and $42\% \pm 1.0\%$ under process regulation, respectively. Furthermore, the static power consumption of the two strategies was compared at $V_{DD} = 2$ V by calculating $P = I_{DD} \times V_{DD}$, where I_{DD} is the measured supply current. As shown in Fig. S13 in the ESM, the process-regulated inverters exhibit lower static power consumption than the R -regulated inverters. In particular, the power consumption at both the high-level output state and the switching threshold voltage V_m is reduced by approximately eightfold. These results demonstrate that process regulation centers V_m and improves gain, rail-to-rail output, noise tolerance, and static power performance without the area penalty imposed by W/L tuning.

2.3 Digital logic circuits

We next evaluated whether the optimized CNT-TFT inverter platform could support dynamic and cascaded digital circuits under low-voltage operation. For this purpose, we fabricated a 5-stage pseudo-PMOS ring oscillator (RO) based on zero- V_{GS} -load inverters. Each stage employed CNT-TFTs with $W/L = 50/3$ μm , and an additional inverter was used as the output buffer. To characterize the unit inverter used in the RO, ten representative standalone zero- V_{GS} -load inverters with the same channel dimensions of $W/L = 50/3$ μm were fabricated and measured at $V_{DD} = 2$ V. Their voltage transfer characteristics, voltage–gain curves, and transient current characteristics are provided in Fig. S14 in the ESM. The optical micrograph, circuit schematic, and oscillation waveform of the RO are shown in Figs. 4(a) and 4(b), respectively. At $V_{DD} = 2$ V, RO oscillates at 60 kHz, corresponding to a stage delay of 1.6 μs . Although the oscillation speed is moderate, this result confirms that the present CNT-TFT platform can sustain dynamic multistage switching at low supply voltage.

To further examine the transient response of a single optimized inverter, we measured its square-wave output under capacitive loading, as shown in Fig. 4(c). The inverter maintains a 60 kHz square-wave output with a load capacitance exceeding 150 pF. The transient response is asymmetric, with a rise time of 1 μs and a fall time of 5.2 μs , which is consistent with the finite current capability of the zero- V_{GS} -load transistor during one switching transition [28]. Even so, the stable operation under a relatively large capacitive load supports the use of the present inverter platform in low-voltage cascaded logic circuits.

We then constructed a set of basic logic gates using the same zero- V_{GS} load architecture, with CNT-TFTs with $W/L = 50/5$ μm . The circuit schematics of the NOT, NOR, NAND, AND, OR, and XOR gates are shown in Fig. 4(d); their optical micrographs are presented in Fig. S15 in the ESM, and their representative output waveforms are shown in Fig. 4(e). NAND and NOR gates were directly implemented using the zero- V_{GS} load topology. AND and OR gates were realized by cascading NAND or NOR gates with an inverter. The XOR gate was constructed from four NAND gates, for a total of 12 transistors. Square-wave inputs of 100 and 50 Hz were applied to verify the logic functions. All basic gates operate correctly at $V_{DD} = 2$ V and exhibit near rail-to-rail output behavior.

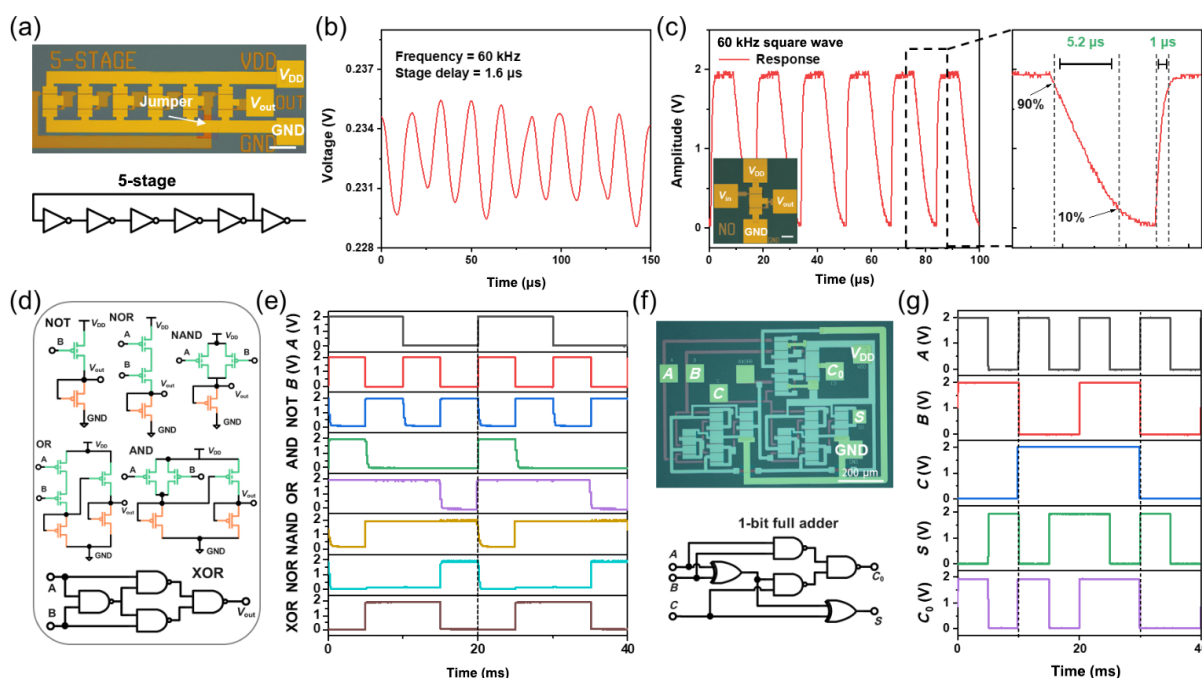


Figure 4 Digital logic circuits based on CNT-TFTs. (a) Optical micrograph (top) and circuit schematic (bottom) of a 5-stage cascaded RO consisting of zero- V_{GS} -load inverters. The jumper region used for interconnect crossing is labeled in the optical micrograph. Scale bar: 100 μm . (b) Oscillation waveform of the RO. (c) 60 kHz square-wave response of a single-stage optimized inverter under capacitive loading (> 150 pF); the inset shows the optical micrograph of the inverter. Scale bar: 50 μm . (d) Circuit schematics of basic logic gates. The enhancement-mode and depletion-mode CNT-TFTs are represented by broken/dashed and continuous/solid channel symbols, respectively, with green and yellow colors used as visual guides. (e) Measured output waveforms of the basic logic gates. (f) Optical micrograph (top) and logic diagram (bottom) of a 1-bit full adder. Scale bar: 200 μm . (g) Measured output waveforms of the 1-bit full adder with and without carry input.

To further examine cascading capability at a higher integration level, we fabricated a 1-bit full adder composed of 11 NAND gates. As shown in Fig. 4(f), the Sum output is formed from two XOR gates, whereas the Carry output is realized from one XOR gate and three NAND gates. The measured output waveforms in Fig. 4(g) confirm correct operation both with and without carry input. The logic levels remain stable at $V_{DD} = 2$ V, with high-level output around 1.95 V and voltage loss below 3%. Together with the RO results above, these data demonstrate low-voltage dynamic and cascaded logic operation on flexible substrates using the optimized CNT-TFT platform.

3 Conclusions

In summary, we developed a machine learning-guided process co-optimization framework for flexible CNT-TFTs and validated it using low-voltage digital logic as a representative application scenario. By combining multistep fabrication optimization with a circuit-oriented weighted evaluation scheme, we obtained enhancement-mode CNT-TFTs with extracted μ_{eff} up to $71 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ and width-normalized $I_{\text{D}}|_{V_{GS}=0 \text{ V}}$ as low as $0.2 \text{ pA} \cdot \mu\text{m}^{-1}$. These device improvements enabled 2 V pseudo-PMOS inverters with centered switching threshold, high gain, low output loss, and large noise margins. The same optimized platform further supported a 5-stage RO, near rail-to-rail basic logic gates, and a 1-bit full adder, demonstrating low-voltage dynamic and cascaded logic operation on flexible substrates. More broadly, this work establishes a practical route for translating circuit requirements into fabrication-process optimization in CNT-TFT technologies and provides a useful framework for application-specific development of flexible integrated electronics.

4 Methods

4.1 Deposition of randomly oriented carbon nanotube network films

The deposition of randomly oriented CNT network films mainly involves two steps: preparation of the semiconducting CNT dispersion and dip-coating deposition. First, 100 mg of raw arc-discharged CNTs (Carbon Solutions Inc.) and 200 mg of 9-(1-octynonyl)-9H-carbazole-2,7-diyl (PCz) were dispersed in 100 mL of chloroform, followed by ultrasonication for 30 min at 300 W using a tip sonicator (VC500, Sonics). The solution was then centrifuged at 20,000g for 1 h (Allegra X-22R, Beckman Coulter) to remove most CNT bundles and insoluble residues. The supernatant was collected and centrifuged again at 50,000g for 2 h to further reduce the metallic CNT fraction. The final supernatant was filtered, and the purified CNT solid was redispersed in chloroform to obtain the working CNT solution. For CNT film deposition, the CNT solution was ultrasonicated for 10 min and loaded into the dip-coating chamber. The flexible substrate was mounted on a holder and fully immersed into the solution without contacting the chamber wall. The number of dipping cycles and withdrawal speed were then set. In a single cycle, the substrate was immersed in the solution and slowly withdrawn to deposit CNTs onto the surface. After dip coating, the sample was cleaned with toluene at 75 $^{\circ}\text{C}$ for 30 min and then rinsed with isopropanol. Finally, the sample was dried with N_2 and heated on a hot plate at 150 $^{\circ}\text{C}$ for 30 min to stabilize the CNT film on the substrate.

4.2 Fabrication of flexible CNT-TFTs and circuits

All CNT-TFTs and integrated circuits were fabricated on flexible PI film substrates supported by low-resistivity silicon. The PI layer was

prepared by spin-coating a PI precursor onto the silicon wafer, followed by solvent evaporation at 250 °C for 30 min and subsequent thermal imidization at 350 °C for 1 h on a hot plate. To improve interfacial adhesion, a 5 nm HfO₂ layer was grown on the PI by atomic layer deposition (ALD) (TFS-200, Beneq). Bottom-gate CNT-TFTs and circuits were then fabricated on the PI/HfO₂ substrate. The gate electrodes were defined by photolithography (EVG610, EV Group), followed by electron-beam evaporation and lift-off. A second photolithography step was used to define the gate dielectric, and the HfO₂ dielectric layer was deposited at 90 °C by ALD. A randomly oriented CNT network was then deposited by dip coating. After photoresist protection of the channel region, unwanted CNT material was removed by reactive ion etching (Etchlab 200, Sentech). Source and drain contacts were subsequently patterned by photolithography, metal deposition, and lift-off. The channel region was encapsulated with photoresist (S1813, Kayaku Advanced Materials). For the jumper structures used in the integrated circuits, a 20 nm HfO₂ layer served as the dielectric. Finally, flexible electronic devices and circuits were delaminated from the silicon wafer using the capillary-assisted electrochemical delamination method [19, 29]. Additional process descriptors and representative fabrication recipes are summarized in Table S1 in the ESM.

4.3 Electrical characterization

The electrical characteristics of the fabricated devices and logic circuits were measured using a semiconductor parameter analyzer (Keithley 4200A-SCS, Tektronix), an oscilloscope (MSOS404A, Agilent Technologies), a function generator (81150A, Agilent Technologies), and a probe station (Summit 1100, Cascade). All measurements were performed in ambient air at room temperature.

Electronic Supplementary Material: Supplementary material (fabrication process optimization recipes, decision-tree model evaluation, mechanical and electrical characterization of CNT-TFTs, and comprehensive performance analyses (VTCs, noise margins, and power consumption) of the regulated inverters and logic gates) is available in the online version of this article at <https://doi.org/10.26599/NR.2026.94909009>.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

Q. B. G.: Data curation, project administration, validation, writing manuscript, experimental design. F. X., L. Y. G., and L. X.: Data

curation, validation. Y. F. H.: Project administration, funding acquisition, writing manuscript. All the authors have approved the final manuscript.

Use of AI statement

None.

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