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Mitigating Fermi-level pinning in 2D transistors via reactive phase-transformed contacts

Mengting Huang, Shuangquan Qu, Yiming Ding, Binbin Zhang, Shibo Wang, Xiaolong Xu(✉), Yeliang Wang(✉)
School of Integrated Circuits and Electronics, MIIT Key Laboratory for Low-Dimensional Quantum Structure and Devices, Beijing Institute of Technology, Beijing 100081, China

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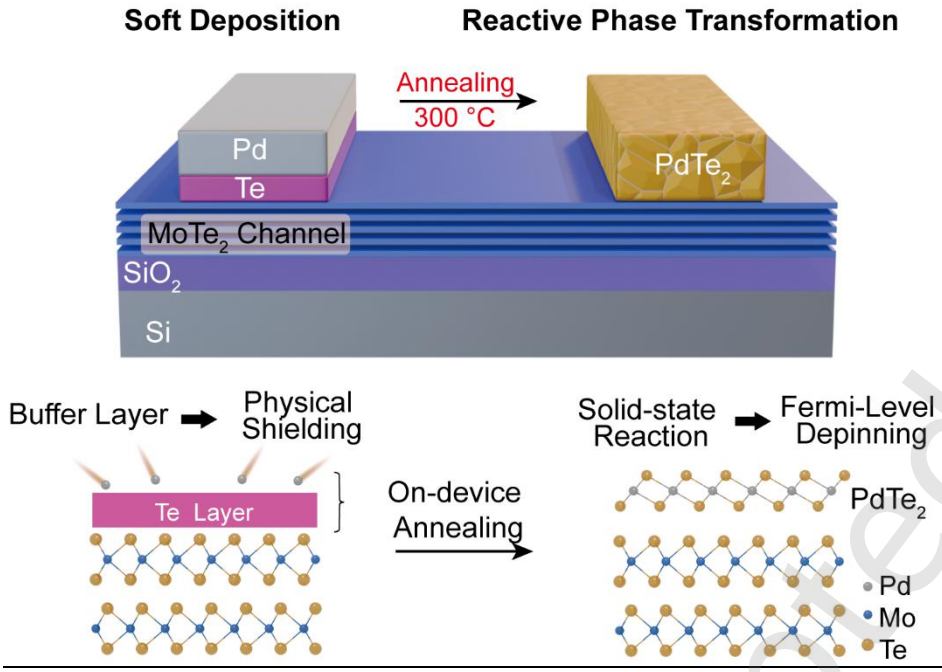

This paper presents a reactive phase-transformed contact strategy to mitigate Fermi-level pinning in 2D transistors, using a Te layer and low-temperature Pd–Te conversion to form conductive $PdTe_2$ contacts. The resulting contacts preserve the 2D semiconductor interface, weaken pinning, and enhance the electrical performance of $MoTe_2$ and WSe_2 FETs.

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School of Integrated Circuits and Electronics, MIIT Key Laboratory for Low-Dimensional Quantum Structure and Devices, Beijing Institute of Technology, Beijing 100081, China

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Address correspondence to Xiaolong Xu, xuxiaolong@bit.edu.cn; Yeliang Wang, yeliang.wang@bit.edu.cn

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ABSTRACT: The integration of high-performance two-dimensional (2D) semiconductor devices is fundamentally bottlenecked by severe Fermi-level pinning (FLP) at the metal-semiconductor interface. Direct deposition of high-work-function, high-melting-point metals typically inflicts structural damage on the 2D lattice, generating interfacial defects that strongly pin the Fermi level. Here, we report a damage-free metallization strategy utilizing low-temperature phase engineering to achieve highly conductive, weakly pinned contacts. We employ a low-energy evaporation of tellurium (Te) as a non-destructive buffer layer, which effectively shields the underlying 2D channel during the subsequent deposition of palladium (Pd). Through a precisely controlled low-temperature annealing process, the Te and Pd layers undergo a solid-state reaction, transforming into a highly conductive, high-work-function metallic $PdTe_2$ phase. We demonstrate that $PdTe_2$-contacted $MoTe_2$ field-effect transistors (FETs) exhibit significantly enhanced electrical performance compared to those with directly deposited Pd or unannealed Te/Pd contacts. Furthermore, applying this strategy to WSe_2 FETs shifts the transport from a strongly pinned n-type behavior—characteristic of direct Pd contacts—to a weakly pinned ambipolar characteristic with superior electrical properties. Crucially, the low thermal budget of this phase-transformation process offers a scalable pathway for integrating pristine, high-performance 2D electronics.

KEYWORDS: two-dimensional (2D) semiconductor devices, contact, Fermi-level pinning, $PdTe_2$

1 Introduction

Two-dimensional (2D) transition metal dichalcogenides (TMDCs) are highly promising candidates for next-generation[1-3], aggressively scaled logic devices due to their atomic thickness and excellent immunity to short-channel effects[4, 5]. However, unlocking the intrinsic performance of 2D semiconductors is severely hindered by the large contact resistance at the metal-semiconductor interface[6-9]. Ideally, the Schottky barrier height at this interface should be governed by the work function of the contact metal according to the Schottky-Mott rule[6, 10-12]. In practice, the interface is universally subjected to severe Fermi-level pinning (FLP), which drastically limits carrier injection efficiency and dictates the device polarity regardless of the chosen metal[11, 13, 14].

The physical origin of this FLP is inextricably linked to the conventional metallization process[15-17]. The direct physical vapor deposition (e.g., electron-beam evaporation) of high-work-function, high-melting-point metals, such as palladium (Pd) or platinum (Pt), involves high-kinetic-energy adatoms[6]. The bombardment of these energetic metal atoms onto the fragile 2D lattice inevitably causes catastrophic interfacial degradation, including the generation of chalcogen vacancies, atom interdiffusion, and the formation of disordered glassy states[15]. These process-induced interfacial defects create a high density of gap states that pin the Fermi level, masking the intrinsic band alignment and severely degrading the overall electrical transport properties[14]. While strategies such as transferred van der Waals (vdW) contacts or the insertion of tunneling buffer layers (e.g., graphene or h-BN) have been proposed to mitigate interfacial damage[18], they often face significant challenges regarding large-scale uniform fabrication or introduce additional tunneling resistance that limits current drive. Alternatively, phase-engineering strategies have been investigated to optimize 2D contacts, as highlighted by recent theoretical predictions[19]. However, experimental implementations often rely on specialized chemical treatments[20] or system-specific doping during synthesis[21], which pose challenges for standard, scalable device integration.

Here, we propose a CMOS-compatible, soft-deposition and reactive phase-transformation strategy to fabricate robust, pristine, and unpinned high-work-function contacts for 2D semiconductors. To decouple the energy of the impinging adatoms from the high melting point of the target contact metal, we introduce a low-melting-point Tellurium (Te) buffer layer. Because Te readily sublimates at low temperatures, the exceptionally low kinetic energy of the Te vapor prevents any structural damage to the pristine 2D channel. This semiconducting Te layer then serves as a robust physical shield during the subsequent deposition of the high-melting-point Pd. To eliminate the potential parasitic resistance introduced by the semiconducting Te buffer, we employ a mild, low-temperature thermal annealing process to trigger a solid-state reaction between the Te and Pd layers. This reaction selectively converts

the contact stack into $PdTe_2$, a metallic transition-metal ditelluride phase characterized by both a high work function and exceptional electrical conductivity.

2 Results and discussion

Figure 1 illustrates the conceptual framework and strategy of our reactive phase-transformed contacts. As schematically shown in Fig. 1a, the conventional direct deposition of high-work-function metals (e.g., Pd) onto 2D semiconductors involve high-kinetic-energy adatoms. This energetic bombardment catastrophically disrupts the fragile 2D lattice, causing severe atomic displacement and generating a high density of defect-mediated gap states[6, 8].

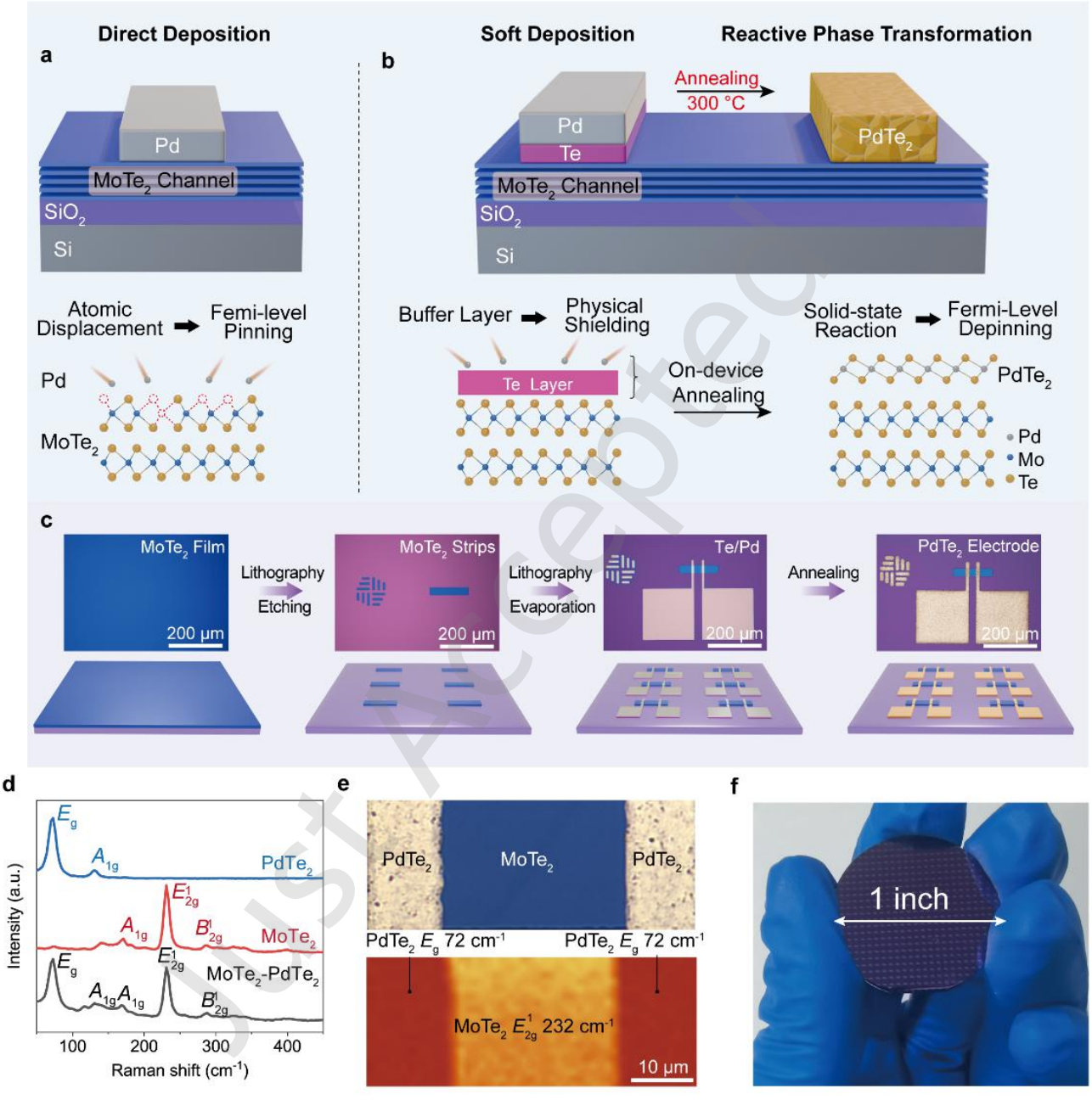

Figure 1. Reactive phase-transformed contact strategy and material characterizations. (a) Schematic of conventional direct Pd deposition, where high-energy metal atoms inflict structural damage and create defect-induced gap states, leading to severe FLP. (b) The proposed reactive phase-transformed strategy illustrating the soft deposition of a low-energy Te buffer layer to shield the 2D lattice from kinetic impact, followed by subsequent Pd deposition, and culminating in an on-device thermal transformation into metallic $PdTe_2$ electrode to realize a weakly pinned vdW interface. (c) Device fabrication workflow combining schematic illustrations and corresponding optical microscope images. (d) Raman spectra of the pristine $MoTe_2$ channel, the synthesized $PdTe_2$ electrode, and the vertically stacked $MoTe_2$ -$PdTe_2$ contact region, demonstrating the simultaneous coexistence of both crystal phases without structural degradation. (e) Optical microscope image and spatially resolved Raman mapping of the $PdTe_2$/$MoTe_2$ transistor. Raman intensity mapping of the characteristic $PdTe_2$ peak (E_g at 72 cm^{-1}) and $MoTe_2$ peak (E^1_{2g} at 232 cm^{-1}). (f) Optical photograph demonstrating the wafer-scale macroscopic uniformity of the $PdTe_2$-$MoTe_2$ devices.

Consequently, the interface is subjected to robust FLP, which limits carrier injection[6, 22]. In contrast, our reactive phase-transformed strategy (Fig. 1b) decouples physical interface protection from functional contact formation. Initially, a low-

melting-point Te layer is deposited via low-temperature thermal evaporation to serve as buffer layer. Due to its low sublimation temperature, the Te vapor condenses with minimal kinetic energy, acting as a kinetic shock absorber that preserves the underlying vdW interface. Following the deposition of Pd, a controlled thermal annealing process triggers a localized, stoichiometric solid-state reaction[23]. This process transforms the precursor stack into a highly crystalline, metallic $PdTe_2$ phase to achieve a high-performance contact.

Figure 1 illustrates the conceptual framework and strategy of our reactive phase-transformed contacts. As schematically shown in Fig. 1a, the conventional direct deposition of high-work-function metals (e.g., Pd) onto 2D semiconductors involve high-kinetic-energy adatoms. This energetic bombardment catastrophically disrupts the fragile 2D lattice, causing severe atomic displacement and generating a high density of defect-mediated gap states[6, 8]. Consequently, the interface is subjected to robust FLP, which limits carrier injection[6, 22]. In contrast, our reactive phase-transformed strategy (Fig. 1b) decouples physical interface protection from functional contact formation. Initially, a low-melting-point Te layer is deposited via low-temperature thermal evaporation to serve as buffer layer. Due to its low sublimation temperature, the Te vapor condenses with minimal kinetic energy, acting as a kinetic shock absorber that preserves the underlying vdW interface. Following the deposition of Pd, a controlled thermal annealing process triggers a localized, stoichiometric solid-state reaction[23]. This process transforms the precursor stack into a highly crystalline, metallic $PdTe_2$ phase to achieve a high-performance contact. The specific fabrication process is depicted in Fig. 1c, utilizing high-quality $MoTe_2$ films whose phase purity and uniform thickness (approximately 7 nm) are verified by Raman spectroscopy and atomic force microscopy (AFM) in Figs. S1 and S2. Initially, the process involves the channel patterning of the synthesized $MoTe_2$ film via large-area UV lithography and etching. This is followed by the electrode window definition for contact regions and subsequent deposition of Te/Pd bilayer precursor stack. A controlled on-device thermal transformation is performed at 300 °C. Instead of desorbing the buffer, this annealing process provides the necessary thermodynamic driving force for on-device reactive phase transformation into a highly crystalline $PdTe_2$ functional electrode. By integrating the protective phase directly into the final contact architecture, this approach ensures a pristine interface while eliminating the high-resistance barriers or complex removal steps associated with traditional sacrificial buffers.

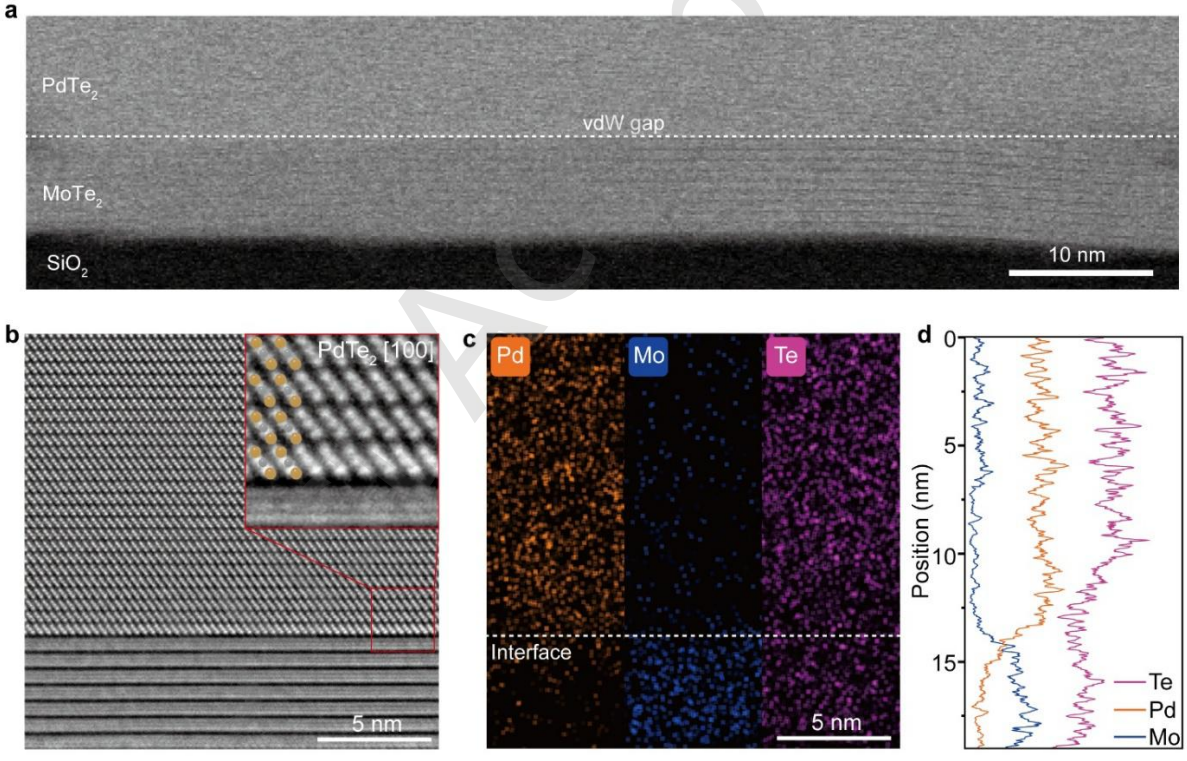

Figure 2 Cross-sectional STEM images of atomically abrupt $PdTe_2/MoTe_2$ interface. (a) Low-magnification cross-sectional HAADF-STEM image showing the overall conformal vdW contact. (b) High-resolution STEM image of the interface, seamlessly overlaid with theoretical crystal structure models, highlighting the well-preserved vdW gap. (c) EDX elemental mapping of Pd, Mo and Te showing their spatial distributions. (d) Quantitative EDX line-scan profile across the junction, confirming an abrupt chemical transition without metal interdiffusion.

The successful on-device synthesis of the $PdTe_2$ electrode and the preservation of the underlying $MoTe_2$ lattice are confirmed by Raman spectroscopy (Fig. 1d). The pristine $MoTe_2$ channel and the $PdTe_2$ electrode exhibit their respective characteristic vibrational modes. Crucially, in the vertically stacked contact region ($MoTe_2$-$PdTe_2$), the Raman spectrum simultaneously displays the distinct peaks of $PdTe_2$ alongside the intrinsic signals of the underlying $MoTe_2$. This coexistence verifies that the reactive phase transformation proceeds homogeneously to form highly crystalline $PdTe_2$ without structurally degrading the delicate 2D channel. Furthermore, spatially resolved Raman mapping (Fig. 1e) corroborates the macroscopic phase uniformity and the vertical stacking architecture. Importantly, this on-device transformation strategy is highly scalable. As demonstrated by the optical photograph in Fig. 1f, a continuous and macroscopically uniform $PdTe_2$-$MoTe_2$ device array can be successfully synthesized at the wafer scale. This exceptional large-area uniformity highlights the excellent compatibility of reactive phase-transformed strategy with standard semiconductor manufacturing and paves the way for

scalable integration of high-performance 2D electronics.

To elucidate the microscopic interfacial structure and verify the non-destructive nature of our strategy, cross-sectional scanning transmission electron microscopy (STEM) was performed. As shown in the low-magnification high-angle annular dark-field (HAADF) STEM image in Fig. 2a, the $PdTe_2$/$MoTe_2$ interface exhibits a highly uniform, continuous, and conformal vdW contact at larger scale. To profoundly investigate the atomic arrangements, a high-resolution STEM image is presented in Fig. 2b, seamlessly overlaid with the theoretical crystal structure models. Strikingly, an atomically sharp and pristine vdW gap is well-preserved between the synthesized $PdTe_2$ electrode and the top layer of the $MoTe_2$ channel. The preservation of this pristine vdW interface achieved through reactive phase-transformation strategy, confirming it shields the 2D lattice. Furthermore, energy-dispersive X-ray spectroscopy (EDX) elemental mapping (Fig. 2c) and the corresponding quantitative line-scan profile (Fig. 2d) were conducted to analyze the chemical composition across the junction. Both the mapping image and the line-scan spectra demonstrate an abrupt spatial transition of Pd, Mo and Te elements. The sharp chemical boundary and the complete absence of Pd interdiffusion into the $MoTe_2$ lattice explicitly confirm that the on-device reactive phase-transformation strategy is strictly confined to the deposited electrode region. This strategy successfully prevents unwanted chemical doping and the formation of MIGS within the semiconductor channel.

Having established the structural superiority of the vdW interface, we systematically evaluated the electronic properties of the synthesized $PdTe_2$ electrode and its corresponding device performance as shown in Figure 3. First, the intrinsic metallic nature of the fully converted $PdTe_2$ film is verified through its electrical characterization (Fig. 3a), which displays excellent conductivity. Specifically, $PdTe_2$ is a

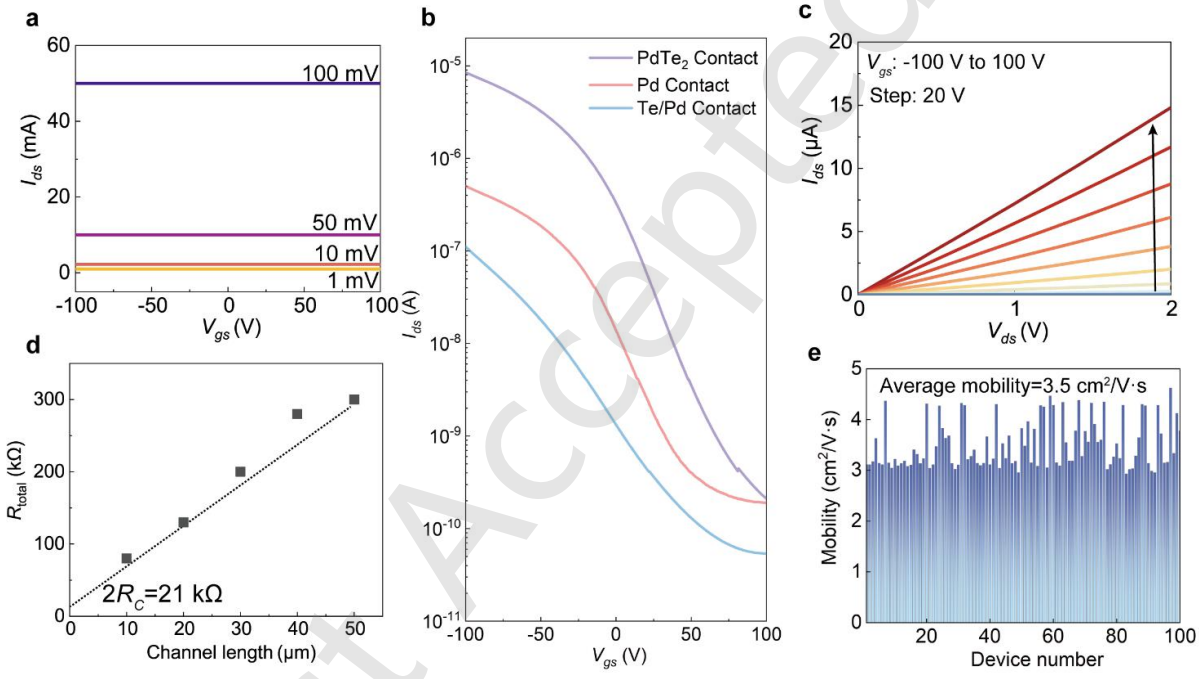

Figure 3. Electrical performance and statistical evaluation of $MoTe_2$ transistors. (a) Intrinsic electrical characterization of the synthesized $PdTe_2$ film. (b) Transfer characteristics of $MoTe_2$ FETs comparing directly evaporated Pd, the as-deposited Te/Pd precursor stack, and the fully synthesized $PdTe_2$ contacts. (c) Output characteristics of the $PdTe_2$ contacted $MoTe_2$ device, exhibiting excellent linearity. (d) Extraction of the contact resistance (R_c) using the TLM. (e) Statistical distribution of the extracted field-effect mobilities for the 100 fabricated devices.

Dirac semimetal, offering high electrical conductivity and a superior density of states for efficient carrier injection[24-26]. Combined with its high work function of ~5.12 eV[27], $PdTe_2$ serves as an ideal hole-injection contact for the valence band maximum (VBM) of $MoTe_2$. To explicitly isolate the impact of our strategy, the transfer characteristics of three distinctly contacted $MoTe_2$ devices were compared: directly evaporated Pd, unconverted Te/Pd buffer layer, and fully synthesized $PdTe_2$ (Fig. 3b). Dual-sweep transfer curves (Fig. S3) exhibit negligible hysteresis, further confirming the high-quality, damage-free interface. Devices with direct Pd contacts exhibit inferior current levels due to severe FLP and energetic interface damage (Fig. S4). Interestingly, the unannealed devices featuring the as-deposited Pd/Te precursor stack exhibit basic field-effect characteristics, but their on-current remains approximately two orders of magnitude lower than that of the optimized devices, accompanied by highly non-linear output curves (Fig. S5). While this disordered phase slightly improves interface coupling compared to a pure insulating barrier, it lacks the requisite metallic conductivity and work function alignment. Subsequent controlled thermal annealing supplies the critical thermodynamic driving force and kinetic conditions for complete atomic diffusion and ordered rearrangement[28, 29]. This thermal activation culminates in the formation of a highly crystalline, stoichiometric $PdTe_2$ phase. In stark contrast to the precursor devices, the FETs with the on-device synthesized $PdTe_2$ electrodes exhibit a robust p-type dominant transport with an on/off ratio exceeding 10^5 and substantially enhanced on-current. The corresponding output characteristics (Fig. 3c) present excellent linearity, suggesting the formation of a highly transparent, Ohmic-like contact. This combination of a damage-free vdW interface and optimized band alignment successfully recovers the intrinsic transport properties of the 2D channel.

To further clarify the role of reactive phase-transformed contacts, we performed Kelvin Probe Force Microscopy (KPFM) and Transfer Length Method (TLM) measurements to analyze

the band alignment and contact resistance of Pd/$MoTe_2$ and $PdTe_2$/$MoTe_2$ junctions. The KPFM results show that both Pd and $PdTe_2$ possess higher work functions than the $MoTe_2$ channel (Fig. S6). According to the ideal Schottky–Mott model, both high-work-function contacts should be favorable for hole injection into p-type $MoTe_2$ and are expected to form low-barrier or Ohmic-like contacts. However, direct Pd deposition can damage the atomically thin $MoTe_2$ surface and generate interfacial defects, chalcogen vacancies, and metal-induced gap states, which act as intermediate states within the bandgap and induce FLP[6, 30]. Consequently, this contact suffers from a larger effective Schottky barrier and inefficient carrier injection. In contrast, the Te layer protects the $MoTe_2$ surface from direct metal bombardment during metallization, and the subsequent low-temperature reaction converts the Te/Pd stack into conductive $PdTe_2$ while preserving a cleaner contact interface. The reduced density of defect-induced gap states weakens FLP and lowers the effective hole-injection barrier. Consistently, TLM measurements show that the contact resistance (R_c) decreases from approximately 62.5 kΩ for directly Pd-contacted $MoTe_2$ to 10.5 kΩ for $PdTe_2$-contacted $MoTe_2$ (Fig. 3d and Fig. S7). This reduced contact resistance provides quantitative evidence for a smaller effective Schottky barrier, which further contributes to the enhanced field-effect mobility of the $PdTe_2$-contacted $MoTe_2$ FETs. The corresponding energy band diagrams are shown in Fig. S8.

Furthermore, to demonstrate the process reliability and uniformity, a rigorous statistical analysis was conducted on an array of 100 devices across various channel lengths (L=10, 20, 30, 40, 50 μm, 20 devices each). The highly overlapping transfer curves (Fig. S9) and the narrow statistical distribution of the extracted field-effect mobilities (Fig. 3e) strongly underscore the exceptional reproducibility and scalability of the reactive phase-transformation strategy for large-scale 2D integration. Comparison with previous literature (Table S1) shows that our devices significantly outperform those using direct metal contacts[21, 31-33]. While material-specific 1T'-$MoTe_2$ phase contacts might exhibit slightly higher performance, they are less generalizable than our approach, which provides a general and CMOS-compatible solution for various 2D systems.

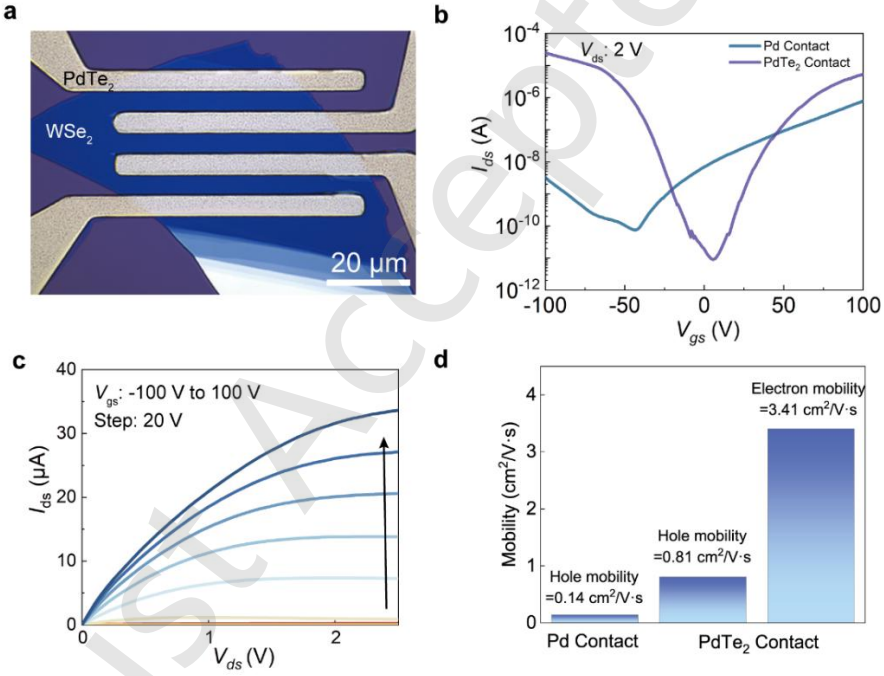

Figure 4. Universality and polarity modulation on WSe_2 transistors. (a) Optical microscope image of the fabricated WSe_2 device. (b) Transfer characteristics comparing WSe_2 FETs with direct Pd contacts (showing pinned, n-type dominant transport) and on-device $PdTe_2$ contacts (showing weakly pinned, robust ambipolar transport). (c) Output characteristics of the $PdTe_2$-contacted WSe_2 device. (d) Quantitative comparison of the extracted hole and electron mobilities between the direct Pd and $PdTe_2$ contacts, verifying the fundamental polarity shift.

To further demonstrate the universality and process scalability of reactive phase-transformation strategy, we extended its application to WSe_2 field-effect transistors, as depicted in the optical microscope image (Fig. 4a). WSe_2 is a prototypical ambipolar 2D semiconductor, however, its experimental transport polarity is often restricted by the interface physics governed by MIGS and FLP[34]. As explicitly compared in the transfer characteristics (Fig. 4b), WSe_2 FETs with directly evaporated Pd electrodes exhibit a unipolar, n-type dominant behavior. The energetic metal bombardment during deposition introduces dense interfacial defects that pin the Fermi level near the conduction band, severely restricting hole injection despite the inherently high theoretical work function of Pd[6]. In striking contrast, devices integrating the synthesized $PdTe_2$ electrodes undergo a dramatic polarity modulation, displaying robust ambipolar transport. By preserving a pristine vdW interface, the reactive phase-transformation strategy successfully depins the Fermi level[6]. This depinning allows its high work function to effectively align with the valence band of WSe_2, boosting the hole on-current by several orders of magnitude[6, 35]. The corresponding output characteristics (Fig. 4c) for the $PdTe_2$-contacted WSe_2 exhibit excellent linearity. This unambiguously confirms the formation of highly transparent, Ohmic-like contacts for bidirectional charge injection. To quantitatively assess this fundamental contact optimization, the field-effect mobilities of the devices were extracted and compared (Fig. 4d). The $PdTe_2$ contacts yield a substantially enhanced hole mobility compared to the direct Pd control group, while maintaining an excellent and balanced electron mobility. These quantitative metrics verify that the $PdTe_2$ electrode acts as

a non-destructive, transparent contact window. Rather than forcing the device into a pinned unipolar state, it successfully uncovers the intrinsic ambipolarity of WSe_2, highlighting its broad applicability for advanced 2D complementary logic architectures.

3 Conclusions

In summary, we have proposed and experimentally demonstrated a novel reactive phase-transformation strategy that resolves the critical Fermi level pinning challenge in 2D semiconductor contacts. By on-device thermal reaction, we transformed Te/Pd into a highly conductive $PdTe_2$ functional electrode. This approach physically shields the delicate vdW interface from deposition-induced damage while providing a high-work-function contact. Consequently, $MoTe_2$ transistors utilizing the $PdTe_2$ electrodes exhibit excellent p-type performance with significantly minimized contact resistance. Furthermore, this strategy is universally applicable, as demonstrated by the successful polarity modulation from n-type to ambipolar transport in WSe_2 devices through effective Fermi level depinning. This on-device phase engineering paves a scalable, non-destructive, and highly reliable pathway for the development of high-performance 2D CMOS electronics.

4 Experimental

Synthesis of $MoTe_2$ Films

High-quality $MoTe_2$ thin films were synthesized via the direct atmospheric-pressure tellurization of pre-deposited molybdenum (Mo) films on SiO_2/Si substrates. The process was conducted in a horizontal hot-wall tube furnace under a continuous flow of Ar and H_2 carrier gases. Specifically, the system was heated to 620°C and maintained for 1 hour to ensure the complete conversion of the Mo precursor into highly crystalline $MoTe_2$.

Synthesis of $PdTe_2$ Electrodes

The $PdTe_2$ functional electrodes were synthesized via a precisely controlled on-device reactive phase transformation. Initially, a thin Te buffer layer was deposited via low-temperature thermal evaporation. Subsequently, 10 nm Pd thin film was deposited onto the 20 nm Te layer using electron-beam evaporation. To trigger the chemical transformation, the Te/Pd bilayer stack was subjected to thermal annealing at 300 °C for 10 minutes.

Characterizations

The atomic-scale structural analysis and chemical mapping were performed using a Thermo Fisher Scientific Titan Themis Z (60–300 kV) STEM equipped with aberration correctors for both condenser and objective lenses. To achieve high-resolution HAADF-STEM imaging, the instrument was operated at an accelerating voltage of 300 kV with an atomic resolution of 80 pm. The specific imaging conditions included a 30 pA beam current, a 25 mrad convergence semiangle, and a collection semiangle range of 80–379 mrad. Elemental distribution and stoichiometric analysis were conducted via EDS using a Bruker Super-X EDX detector integrated within the STEM system. Surface morphology and film roughness were characterized by AFM using an Oxford Cypher S system in tapping mode. Raman spectroscopy was performed with a WITec alpha300 confocal micro-Raman system using a 532 nm excitation laser to confirm the vibrational modes and phase purity of the $MoTe_2$ and $PdTe_2$.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and/or the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

All the contributing authors report no conflict of interests in this work."

Author contribution statement

Y.W. and X.X. supervised the project. X.X. conceived the idea. X.X. and M.H. designed the experiments and analyzed the results. S.Q. performed the STEM characteristics under the supervision of X.X.. M.H. performed the CVD growth with the help of Y.D., B.Z., S.W.. M.H. and X.X. wrote the manuscript with input from all the authors. Y.W. reviewed and edited the manuscript. All the authors help with the discussion.

Informed consent

Not applicable

Ethics statement

Not applicable

Use of AI statement

None

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Electronic Supplementary Material

Mitigating Fermi-level pinning in 2D transistors via reactive phase-transformed contacts

Mengting Huang, Shuangquan Qu, Yiming Ding, Binbin Zhang, Shibo Wang, Xiaolong Xu, and Yeliang Wang

School of Integrated Circuits and Electronics, MIIT Key Laboratory for Low-Dimensional Quantum Structure and Devices, Beijing Institute of Technology, Beijing 100081, China

Address correspondence to Xiaolong Xu, xuxiaolong@bit.edu.cn; Yeliang Wang, yeliang.wang@bit.edu.cn

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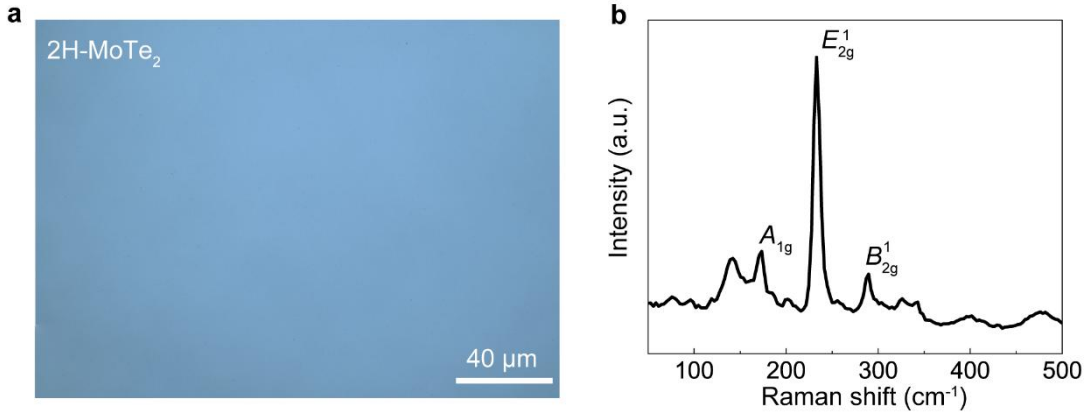

Figure S1 Morphological and Raman characterization of the as-synthesized $MoTe_2$ films. (a) Optical microscope image of the 2H-$MoTe_2$ film demonstrating macroscopic continuity and surface uniformity over a large area. (b) Raman spectrum of the synthesized film. The prominent vibration modes at 173 cm^{-1} (A_{1g}), 233 cm^{-1} (E^1_{2g}), and 290 cm^{-1} (B^1_{2g}) are consistent with the characteristic peaks of 2H-$MoTe_2$, verifying the successful phase-controlled synthesis and high crystalline quality of the channel material.

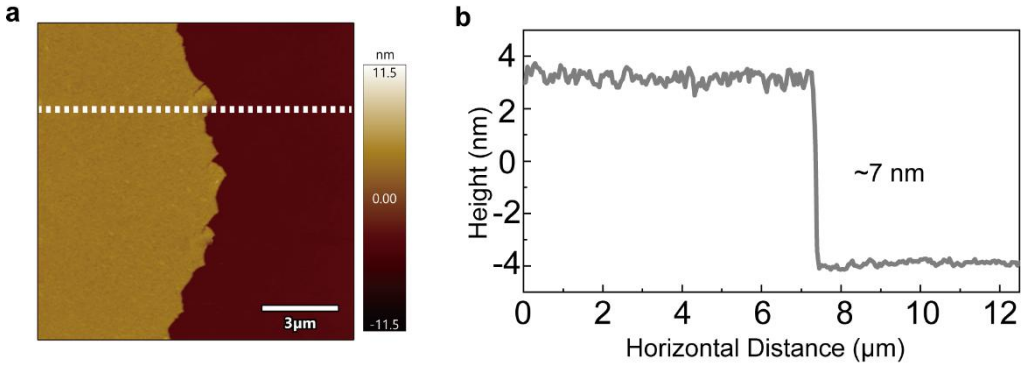

Figure S2 Atomic force microscopy (AFM) characterization and thickness evaluation of the $MoTe_2$ film. (a) Representative AFM topography image of the as-synthesized $MoTe_2$ film, showing a flat and continuous surface morphology. (b) Height profile extracted from the line scan indicated in (a). The step height confirms a uniform film thickness of approximately 7 nm.

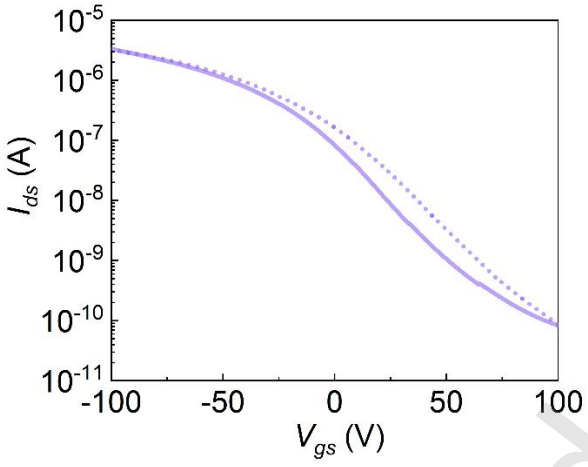

Figure S3 Dual-sweep transfer characteristics of $PdTe_2$-contacted $MoTe_2$ FET. The forward (solid line) and backward (dashed line) sweeps exhibit negligible hysteresis, confirming the high interface quality and the absence of significant charge trapping states.

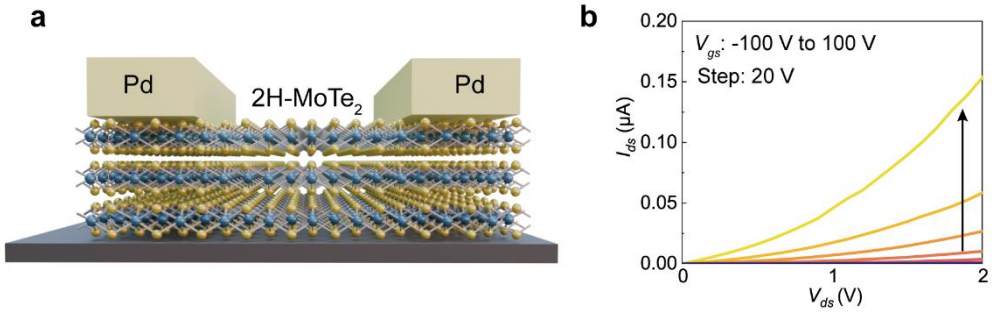

Figure S4 Structural and electrical characterization of $MoTe_2$ FET with direct Pd electrodes. (a) Schematic illustration of the device architecture featuring directly evaporated Pd source/drain electrodes on the $MoTe_2$ channel. This configuration represents the conventional contact method without the protective Te buffer layer. (b) Output characteristics of the Pd-contacted device measured at various gate voltages. Compared to the $PdTe_2$-contacted FETs shown in the main text, these curves exhibit significantly lower drain current levels and a less linear behavior at low bias, highlighting the high contact resistance and interface degradation induced by the high-energy metal deposition.

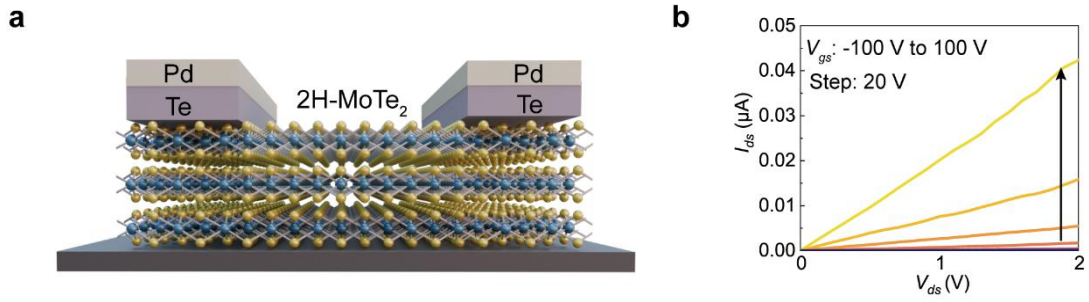

Figure S5 Structural and electrical characterization of the precursor $MoTe_2$ FET with unannealed Te/Pd electrodes. (a) Schematic illustration of the device architecture featuring the as-deposited Te/Pd precursor stack as source/drain electrodes. This state represents the device after metal deposition but prior to the thermal annealing process. (b) Output characteristics of the unannealed precursor device. The curves exhibit relatively low current magnitudes and pronounced non-linearity at low drain bias. This sub-optimal performance is attributed to the lack of a well-defined $PdTe_2$ at the interface, serving as a baseline to highlight the critical role of the subsequent thermal transformation.

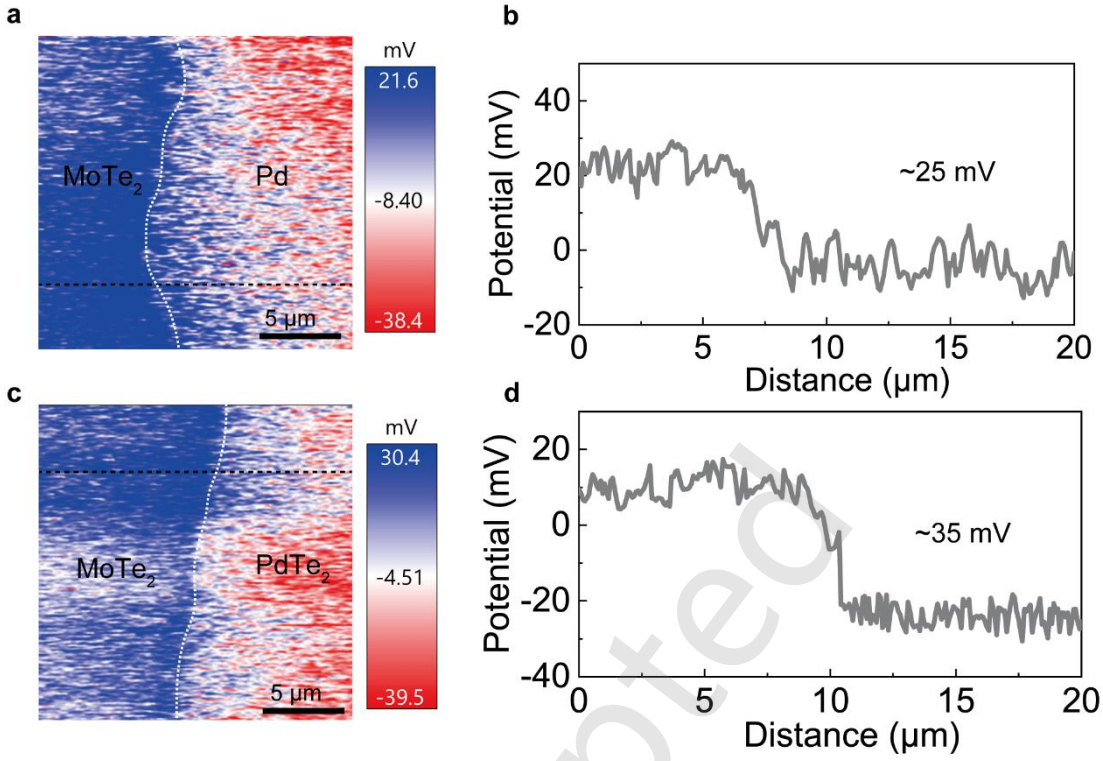

Figure S6 KPFM characterization of the contact interfaces. (a, b) The surface potential mapping and corresponding line profile of the Pd-$MoTe_2$ junction. (c, d) The surface potential mapping and corresponding line profile of the $PdTe_2$-$MoTe_2$ junction.

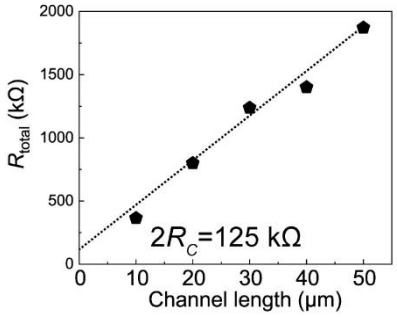

Figure S7 Extraction of the Pd-contact resistance (R_c) using the TLM.

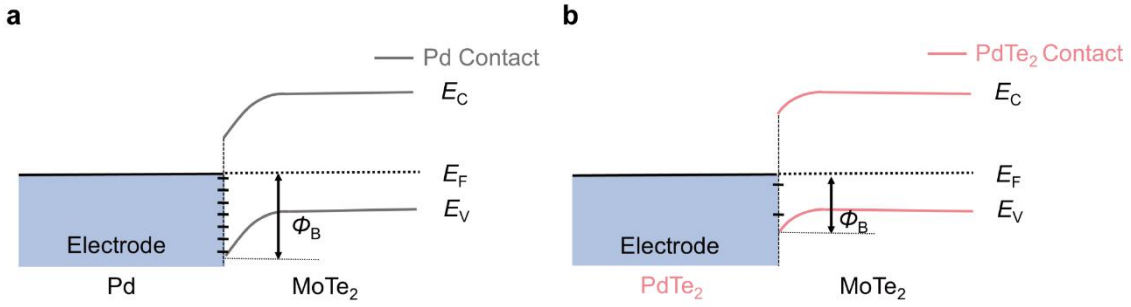

Figure S8 Energy band diagrams of the contact interface. (a) Pd Contact. (b) $PdTe_2$ Contact.

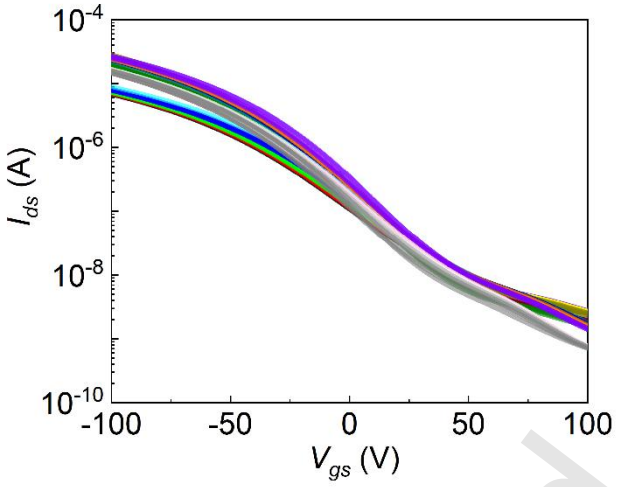

Figure S9 Overlaid transfer curves of 100 $PdTe_2$-contacted devices with various channel lengths (L=10-50 μm), demonstrating high process uniformity.

Table S1 Comparison between the present study and representative reports from the literature.

Reference	Contact Type	Dielectric	Mobilities ($cm^2/V·s$)	I_{ON}/I_{OFF}
Present work	$PdTe_2$	SiO_2	3.5	10^5
21	1T′-$MoTe_2$	SiO_2	14	8×10^4
31	$Mo_xW_{1-x}Te_2$	SiO_2	6.3	$10^{3.5}$
32	In/Au	SiO_2	0.61	10^3
33	1T′-WTe_2	SiO_2	6.7	7×10^4