

Robust Sb₂Se₃ memristors via pressure-modulated growth for noise-resilient neuromorphic computing

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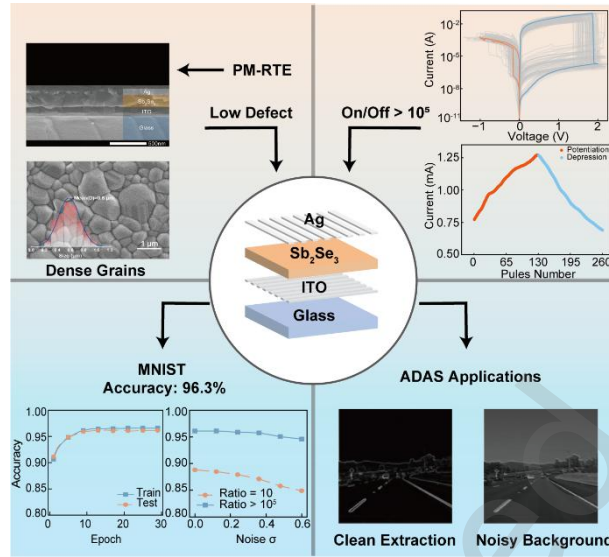
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Robust Ag/Sb₂Se₃/ITO synapses are fabricated via a pressure-modulated rapid thermal evaporation strategy to control intrinsic defects, preserving an ultralow carrier concentration and achieving a high ON/OFF ratio ($> 10^5$) that suppresses array-level leakage. Consequently, the hardware enables noise-resilient neuromorphic computing with 96.3% recognition accuracy and robust motion-edge extraction in dynamic, noise-corrupted scenarios.

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ABSTRACT: High-fidelity neuromorphic computing requires synaptic hardware that balances analog precision with array-level noise immunity, yet suppressing leakage currents in chalcogenide crossbars often necessitates complex interface engineering. Here, a robust Ag/Sb₂Se₃/ITO synapse is reported, fabricated *via* a pressure-modulated rapid thermal evaporation (RTE) strategy that targets intrinsic defect control. Crucially, this thermodynamic optimization preserves the ultralow intrinsic carrier concentration ($\sim 10^{14} \text{ cm}^{-3}$) of the Sb₂Se₃ functional layer, physically prohibiting background leakage pathways without requiring additional buffer layers. Consequently, the device demonstrates highly uniform analog switching behavior, a substantial ON/OFF ratio ($>10^5$), and low set/reset voltages. These characteristics effectively suppress sneak path currents and maximize the sensing margins within the crossbar array. At the system level, physics-based neural networks achieve 96.3% accuracy on MNIST, maintaining exceptional robustness against severe salt-and-pepper noise. Furthermore, we demonstrate that the hardware can execute complex motion perception algorithms, successfully extracting clear motion edges in dynamic spatiotemporal scenarios. This work establishes intrinsic carrier concentration modulation as a minimalist yet powerful paradigm for next-generation noise-resilient edge intelligence.

KEYWORDS: antimony selenide, memristors, rapid thermal evaporation, neuromorphic computing, noise-resilient, edge intelligence

1 Introduction

The rapid evolution of the Artificial Intelligence of Things (AIoT) has catalyzed a paradigm shift towards intelligent edge computing, enabling real-time perception in autonomous systems and smart robotics[1–3]. Unlike static data analysis, these applications necessitate the continuous processing of massive, unstructured, and often noise-corrupted spatiotemporal data streams[4,5]. This imposes a dual challenge where systems must be exceptionally energy-efficient to operate at the edge while remaining sufficiently robust to maintain high computational fidelity amidst environmental fluctuations[6–8]. Traditional digital architectures, constrained by the "memory wall" due to the physical separation of processing and storage units, struggle to meet these latency and power constraints[9–11]. To overcome this, neuromorphic computing has emerged as a transformative solution[12–14]. By leveraging memristor crossbars to perform in-memory computing, this architecture executes massively parallel vector-matrix multiplications directly within the memory array, theoretically offering orders of magnitude improvement in throughput and efficiency for data-intensive computing tasks[15–17].

Despite the theoretical potential, implementing high-fidelity neuromorphic hardware requires overcoming the intrinsic non-

idealities of synaptic devices, particularly in passive crossbar array configurations[18,19]. A critical challenge lies in the trade-off between array-level noise immunity and analog weight precision[20–22]. In large-scale arrays, the accumulation of leakage currents through devices in the low-resistance state or unselected high-resistance state creates sneak paths[23,24]. Crucially, this background leakage acts as intrinsic hardware noise, which compresses the read-out margin and degrades the Signal-to-Noise Ratio (SNR) of the computation[25]. An insufficient device ON/OFF ratio causes the accumulated crosstalk to overwhelm the subtle current differences representing synaptic weights, rendering the neural network susceptible to external input noise, such as dynamic background clutter[26,27]. Although integrating selector devices can mitigate leakage, this approach often introduces abrupt switching behaviors that compromise the linear plasticity required for effective learning[28,29]. Consequently, developing a selector-free synaptic device that inherently combines a high ON/OFF ratio to suppress hardware noise with linear analog switching is paramount for realizing reliable and noise-resilient edge intelligence[30,31].

Among the emerging switching media, antimony selenide (Sb₂Se₃) is characterized by its earth abundance, environmental benignity, and exceptional thermodynamic stability, making it a

compelling candidate for sustainable electronics[32,33]. More critically, unlike metallic chalcogenides, Sb_2Se_3 possesses a theoretically low intrinsic carrier concentration ($\sim 10^{14} \text{ cm}^{-3}$) due to its stable semiconducting band structure[34,35]. This intrinsic property implies that, in its pristine state, the material acts as a "pseudo-insulator" capable of effectively suppressing background currents to enable high ON/OFF ratios[36]. Despite these advantages, the application of Sb_2Se_3 in resistive memory is often hindered by relatively high off-state leakage currents[37]. Fundamental studies on defect thermodynamics reveal that this issue stems from the uncontrolled microstructure of the material. Films prepared by conventional vacuum deposition typically suffer from a high density of selenium vacancies (V_{Se}), which act as shallow donors, and result in a polycrystalline structure with small grains and abundant grain boundaries[38–40]. These grain boundaries serve as conductive percolation pathways that deteriorate the insulating property of the high-resistance state, consequently limiting the ON/OFF switching ratio[41–43]. While interface engineering strategies, such as inserting buffer layers, can block these leakage pathways, they do not address the root cause regarding the intrinsic crystalline quality and often complicate the fabrication process[44–46]. Therefore, a synthesis strategy that can suppress defect formation and restore the intrinsic low-carrier nature of Sb_2Se_3 is essential to unlock its full potential.

In this work, we demonstrate a robust $\text{Ag/Sb}_2\text{Se}_3/\text{ITO}$ synaptic memristor that addresses the leakage challenge through intrinsic material optimization. We report a pressure-modulated Rapid Thermal Evaporation (RTE) strategy to thermodynamically control the film growth dynamics[47]. Unlike conventional evaporation, this process utilizes a high-pressure annealing stage that suppresses material re-evaporation and promotes the growth of dense, micrometer-sized grains. This microstructural enhancement significantly reduces the density of grain boundaries, thereby eliminating major leakage channels. As a result, the device achieves a substantial ON/OFF ratio exceeding 105 and low off-state current without requiring additional buffer layers. Leveraging these superior electrical characteristics, including high linearity and a large dynamic range, we constructed a physics-aware neuromorphic simulation framework. The system achieves 96.3% accuracy on the MNIST dataset and demonstrates exceptional robustness against noise due to the physical suppression of array-level crosstalk. This work establishes the RTE-processed Sb_2Se_3 memristor as a high-performance candidate for reliable and energy-efficient edge intelligence hardware.

2 Experimental

Materials: All chemical reagents employed in this study were of analytical grade and used as received without further purification. Antimony selenide (Sb_2Se_3) powder, 99.99%, acetone, anhydrous ethanol, and isopropyl alcohol (IPA) were purchased from Aladdin Biochemical Technology Co., Ltd. High-purity gold (Au, 99.995%) and silver (Ag, 99.995%) granules were obtained from China New Metal Materials Technology Co., Ltd.

Device Fabrication: The memristive devices were fabricated on commercial glass substrates pre-coated with Indium Tin Oxide (ITO). Prior to deposition, the ITO substrates underwent a rigorous cleaning process involving sequential ultrasonic agitation in deionized (DI) water, acetone, anhydrous ethanol, and IPA for 45 min each. The substrates were subsequently dried under a stream of high-purity nitrogen (N_2) gas. To eliminate organic residues and enhance interfacial wettability, the substrates were subjected to UV-Ozone treatment for 40 min.

The Sb_2Se_3 functional layer was deposited via a Rapid Thermal Evaporation (RTE) technique. The Sb_2Se_3 source powder was placed in a quartz boat within a tube furnace, while the cleaned ITO substrate was fixed face-down on a graphite holder. The chamber was evacuated to a base pressure lower than $5 \times 10^{-4} \text{ Pa}$. To ensure high-quality crystallinity, a two-step pressure regulation strategy was employed: (1) nucleation was initiated at a low pressure of 5 mTorr for 60 s; (2) high-purity argon (Ar) gas was introduced to rapidly increase the pressure to 200 Torr, which was maintained for 120 s while the substrate temperature was held at 480°C for in-situ annealing and growth. Finally, the device structure was completed by thermally evaporating Ag top electrodes through a custom-made strip-shaped shadow mask under a vacuum of $5 \times 10^{-4} \text{ Pa}$.

Characterization: The crystallographic structure of the films was analyzed using an X-ray diffractometer (XRD; DX-2700, Hao Yuan Instrument) equipped with a $\text{Cu K}\alpha$ radiation source. Surface morphology and cross-sectional microstructure were examined using field-emission scanning electron microscopy (FESEM; JSM-7001F, JEOL). Cross-sectional SEM analysis clearly revealed the distinct layered architecture of the device, with measured thicknesses of 170.57 nm, 296.47 nm, and 100 nm for the ITO bottom electrode, Sb_2Se_3 functional layer, and Ag top electrode, respectively. To further investigate the surface topography and roughness, atomic force microscopy (AFM; Multimode 8.0, Bruker) was performed in tapping mode. Surface chemical composition and elemental valence states were determined by X-ray photoelectron spectroscopy (XPS; Thermo Scientific ESCALab 250Xi), with all binding energies calibrated to the adventitious C 1s peak at 284.8 eV.

Electrical Measurements: The electrical characteristics of the devices, including DC current-voltage (I-V) sweeps and pulse measurements, were characterized at room temperature in a light-tight, electrically shielded environment. Data acquisition was performed using a semiconductor parameter analyzer (Keysight B2912B or Keithley 2602B). During all measurements, bias voltages were applied to the Ag top electrode while the ITO bottom electrode was grounded.

Neuromorphic Simulations: To evaluate the computational capability of the $\text{Ag/Sb}_2\text{Se}_3/\text{ITO}$ memristor within a neuromorphic hardware system, a physics-based hardware-aware simulation framework was developed. Detailed simulation parameters and model equations are provided in Note S1 and Table S1 in the Electronic Supplementary Material (ESM). This framework bridges the gap between single-device physics and system-level performance by incorporating realistic device properties, including nonlinear conductance modulation, device-to-device variability, and circuit-level constraints. The experimental Long-Term Potentiation (LTP) and Long-Term Depression (LTD) behaviors were fitted using a nonlinear exponential model to extract the synaptic update dynamics. A three-layer Fully Connected (FC) Multilayer Perceptron (MLP) was constructed to perform a standard pattern classification task using the MNIST benchmark. The input data were pre-processed into 400-dimensional feature vectors to match the scale of the crossbar array. The synaptic weights were mapped to the discrete conductance states of the memristors, strictly bounded by the experimental $G_{\min}$ and $G_{\max}$ values, realizing a hardware-faithful representation. The training was performed using a custom "MemristorSGD" optimizer, which updates the synaptic conductance based on the fitted nonlinearity factors (v_p and v_D) rather than ideal floating-point gradient descent. To accurately simulate the signal integrity in a neuromorphic system, we modeled the readout mechanism based on Kirchhoff's Current Law. A critical circuit constraint—the saturation limit of the Transimpedance Amplifier (TIA)—was introduced to evaluate

the system's dynamic range. The saturation threshold was calibrated based on the peak current of the high-ratio Ag/Sb₂Se₃/ITO device. Comparative simulations were conducted between the Ag/Sb₂Se₃/ITO device (High Ratio) and a baseline material (Low Ratio) under varying input noise levels to demonstrate the superior noise tolerance and leakage suppression capability of the proposed neuromorphic hardware.

Neuromorphic Hardware Implementation for Edge Computing: To evaluate the system-level viability of the Ag/Sb₂Se₃/ITO memristor in intricate neuromorphic computing tasks, we constructed a physics-aware hardware convolution engine. The differential mapping strategy and noise modeling details are described in Note S2 and Table S2 in the Electronic Supplementary Material (ESM). This architecture mimics the biological receptive fields to perform analog signal processing directly within the memory array. As illustrated in Figure 5a, the sensory input signal (V_{in}) is mapped to a parallel analog voltage matrix and processed concurrently by a differential memristor pair structure. The Positive Array (G_{pos}) and Negative Array (G_{neg}) physically encode the excitatory and inhibitory synaptic weights, respectively. Through Kirchhoff's Current Law (KCL), the system performs massive parallel multiply-accumulate (MAC) operations, generating intermediate analog current maps that represent the spatial gradients.

The robustness of this neuromorphic processing unit was validated against device non-idealities. We incorporated a stochastic noise model to simulate the intrinsic conductance variability and finite ON/OFF ratio of the physical devices. By leveraging the high switching ratio and uniformity of our Ag/Sb₂Se₃ synapse, the system effectively suppresses the common-mode leakage current during the analog subtraction stage, yielding a high signal-to-noise ratio (SNR) in edge feature extraction. In contrast, simulations based on low-ratio baseline devices exhibit a "Noisy Background" due to leakage accumulation. Furthermore, to demonstrate spatiotemporal processing capabilities, the system successfully performed motion detection on consecutive temporal frames, enabling real-time navigational cues for autonomous systems without reliance on power-hungry digital processors.

3 Results and discussion

3.1 Material Characterization and Structural Analysis

To elucidate the fundamental material properties, a vertical Ag/Sb₂Se₃/ITO heterostructure was fabricated, as schematically illustrated in Fig. 1(a). The structural integrity of the device was verified using cross-sectional scanning electron microscopy (SEM) (Fig. 1(b)). The image confirms a well-defined stacked architecture with sharp interfaces, where the layer thicknesses for the Ag top electrode (TE), Sb₂Se₃ functional layer, and ITO bottom electrode (BE) were determined to be approximately 100 nm, 296 nm, and 170 nm, respectively. The surface micromorphology was further investigated via top-view SEM (Fig. 1(c)), which reveals that the Sb₂Se₃ film consists of large,

tightly packed grains with an average size of approximately 600 nm. Notably, the film exhibits a dense, continuous microstructure devoid of pinhole defects. This high morphological quality, directly attributed to the high-pressure annealing phase of the RTE process, is critical for ensuring electrical stability by minimizing leakage paths[47]. This coarse-grained morphology minimizes grain boundary density, thereby reducing carrier scattering[38]. To verify the necessity of 200 Torr as the optimal growth pressure, comparative experiments reveal that the Sb₂Se₃ film grown at an intermediate pressure of 50 Torr exhibits a fine-grained nanocrystalline morphology with abundant grain boundaries, confirming that this lower pressure is thermodynamically insufficient to suppress material re-evaporation and promote sufficient grain coarsening (Fig. S5, in the Electronic Supplementary Material (ESM)). The crystallographic structure was characterized by X-ray diffraction (XRD), as shown in Fig. 1(d). All diffraction peaks index well to the orthorhombic Sb₂Se₃ phase (JCPDS No. 15-0861). The pronounced intensity of the (120), (211), and (240) peaks signifies a high degree of crystallinity, which ensures a robust structural framework essential for stable device operation[35].

To quantify surface texture, atomic force microscopy (AFM) was employed (Fig. 1(e)). The extracted cross-sectional height profile (Fig. 1(f)) along the marked line reveals a vertical variation of approximately 180 nm, reflecting the intrinsic topography of the polycrystalline grains, where the peaks and valleys correspond to the grain bodies and boundaries, respectively. Kelvin Probe Force Microscopy (KPFM) confirms the film's electrical homogeneity (Figs. S1 and S2, in the Electronic Supplementary Material (ESM)). Notably, the potential drop at grain boundaries (Fig. S2) indicates the accumulation of donor-like V_{se} , providing preferential hopping sites to facilitate Ag^+ electromigration. Hall-effect measurements at 308 K further confirm the intrinsically resistive nature of the RTE-grown Sb₂Se₃ film, characterized by an ultralow carrier concentration of $1.46 \times 10^{14} \text{ cm}^{-3}$ and a high resistivity of $1.56 \times 10^6 \text{ } \Omega \cdot \text{cm}$ (Table S3, in the Electronic Supplementary Material (ESM)). Phase purity was corroborated by Raman spectroscopy (Fig. 1(g)), which displays two dominant peaks at 189.27 cm^{-1} and 210.24 cm^{-1} , characteristic of Sb–Se vibrational modes[32]. Finally, surface chemical composition was analyzed via X-ray photoelectron spectroscopy (XPS). The high-resolution Sb 3d spectrum (Fig. 1(h)) and Se 3d spectrum (Fig. 1(i)) confirm the presence of Sb³⁺ and Se²⁺ valence states, respectively. While trace amounts of surface oxides (Sb-O and Se-O) are observed due to inevitable air exposure, the dominant Sb-Se bonding environment validates the high stoichiometric quality of the functional layer[45]. The high chemical purity is also corroborated by the XPS survey spectrum (Fig. S3, in the Electronic Supplementary Material (ESM)).

3.2 Resistive Switching Performance

The resistive switching performance was systematically evaluated using the configuration shown in Fig. 2(a). Fig. 2(b)

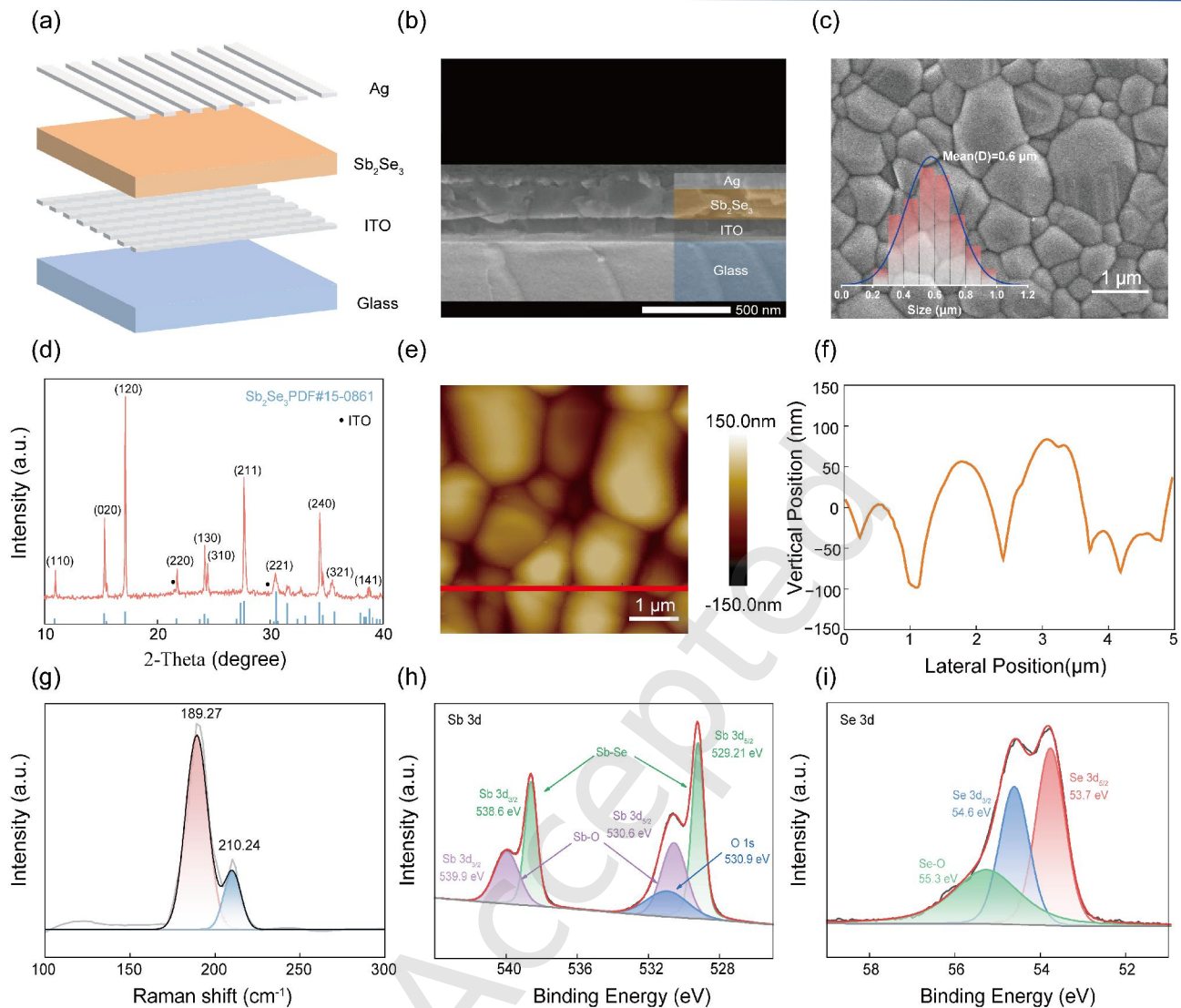


Figure 1 Material characterization of the Ag/Sb₂Se₃/ITO heterostructure. (a) Schematic illustration of the vertical device structure. (b) Cross-sectional SEM image showing a well-defined layered stack. (c) Top-view SEM image of the Sb₂Se₃ film, the inset shows the grain size distribution statistic. (d) XRD pattern corresponding to the orthorhombic Sb₂Se₃ phase. (e) AFM topography and (f) the corresponding cross-sectional height profile along the marked red line. (g) Raman spectrum of the functional layer. (h, i) High-resolution XPS spectra for (h) Sb 3d and (i) Se 3d core levels.

presents representative current–voltage (I - V) characteristics, demonstrating bipolar switching behavior with ultralow operating voltages[35,45,48]. The device transitions from a high resistance state (HRS) to a low resistance state (LRS) at a SET voltage of approximately -0.15 V and restores the HRS at a RESET voltage of roughly $+1.8$ V. To further optimize switching stability, the operating voltage window was modulated (Fig. 2(c)). Extending the negative sweep to -1 V was found to ensure a robust and stable LRS. Meanwhile, increasing the RESET cutoff voltage from 1.2 V to 2 V significantly expanded the memory window. However, notably, a further increase to 3 V resulted in current saturation or slight degradation of the switching cycles. This degradation is likely attributed to excessive Joule heating or the overgrowth of conductive filaments induced by the high electric field, which hinders the complete rupture of conductive paths during the reset process, resulting in a compromised high-resistance state and a reduced switching ratio. Consequently, the sweep range of -1 V / $+2$ V was identified as the optimal, energy-efficient operating window.

Under these optimized conditions, the device exhibits excellent uniformity, as evidenced by the statistical analysis of the resistance ratios (Fig. 2(d)) and switching voltages (Fig.

2(e)). The operating voltages are narrowly distributed around -0.28 V (V_{SET}) and $+1.82$ V (V_{RESET}), with standard deviations of only 0.08 V and 0.16 V, respectively. The device maintains a substantial ON/OFF ratio, with the RESET process yielding a resistance change of nearly 10^5 . Corresponding electrical measurements further demonstrate that devices fabricated under the 50 Torr condition exhibit a notably higher off-state leakage current and a severely degraded ON/OFF switching ratio, fundamentally because the abundant grain boundaries in the fine-grained film act as percolative leakage channels (Fig. S6, in the Electronic Supplementary Material (ESM)). Besides analog switching, the device also exhibits binary switching potential for digital storage (Fig. S4, in the Electronic Supplementary Material (ESM)).

To understand the physical origins of these characteristics, the I - V curves were analyzed in a double-logarithmic plot (Fig. 2(f)). The LRS follows Ohmic conduction (slope ≈ 1.196), indicating the formation of metallic filaments. Conversely, the HRS aligns with the trap-controlled space-charge-limited current (SCLC) model (slope transitions from ~ 1 to ~ 1.6 to ~ 2.6)[41,49]. The operational uniformity is further evidenced by the cumulative probability distribution of resistance states

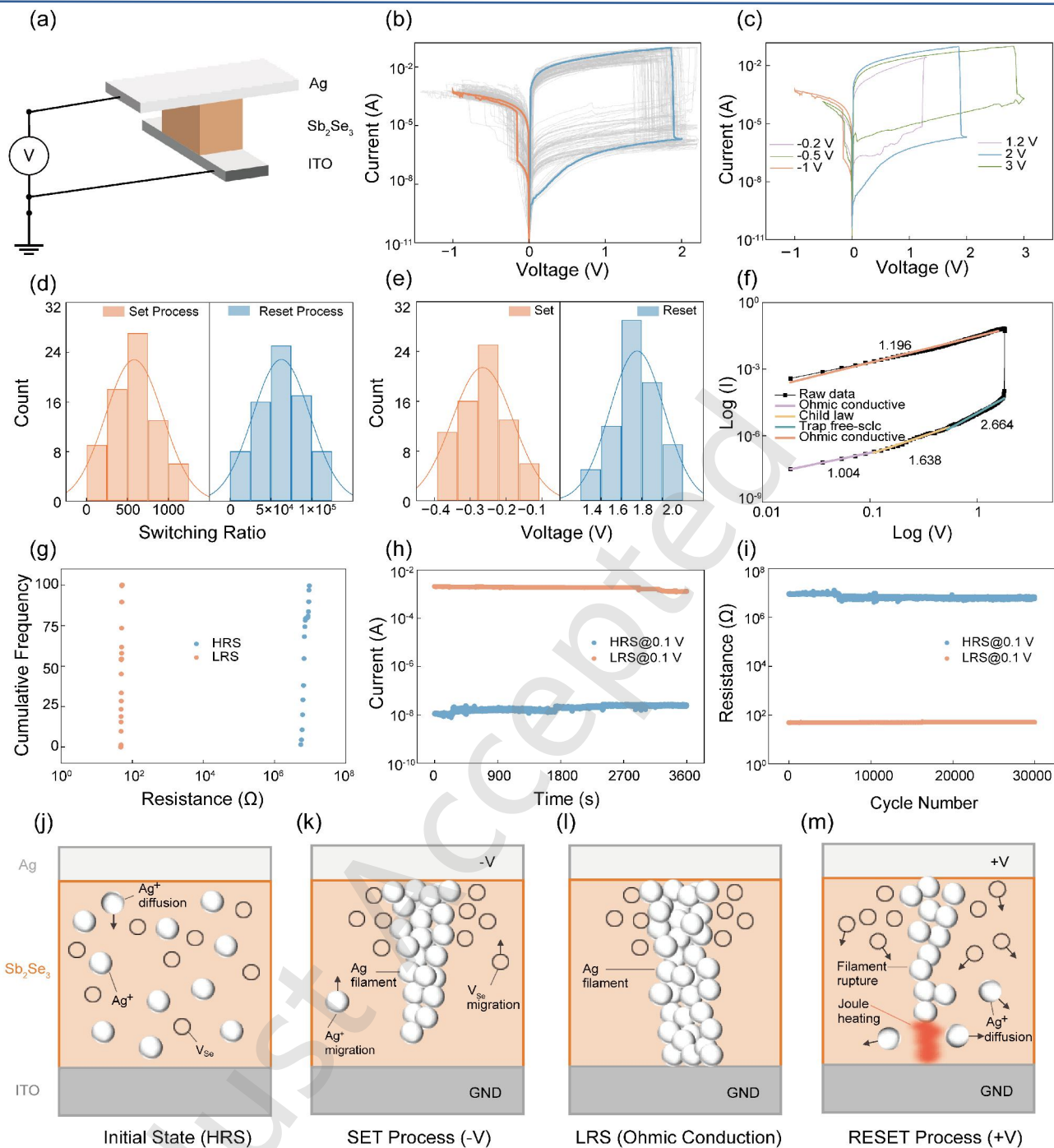


Figure 2 Resistive switching performance and mechanism of the Ag/Sb₂Se₃/ITO device. (a) Schematic of the electrical measurement configuration. (b) Typical bipolar I-V characteristics plotted in logarithmic coordinates. (c) Evolution of switching behavior under different operating voltage windows. (d) Statistical distribution of the resistance values for HRS and LRS. (e) Statistical distribution of the SET (V_{SET}) and RESET (V_{RESET}) voltages. (f) Double-logarithmic I-V plot with linear fittings indicating the conduction mechanisms for different regions. (g) Cumulative probability distribution of the resistance states. (h) Retention characteristics measured at a read voltage of 0.1 V for over 3.6×10^3 s. (i) Endurance test demonstrating stable switching for over 3×10^4 cycles. (j) Schematic of the initial high-resistance state (HRS), depicting the random distribution of mobile Ag⁺ ions and Se vacancies (V_{Se}) within the Sb₂Se₃ matrix. (k) The SET process under negative bias (-V). The electric field drives Ag⁺ migration towards the top electrode, facilitating filament growth via reduction. (l) Low-resistance state (LRS) characterized by the formation of a complete metallic Ag filament, corresponding to Ohmic conduction. (m) The RESET process under positive bias (+V). Localized Joule heating triggers filament rupture and the diffusion of Ag species, restoring the HRS.

(Fig. 2(g)), which shows steep profiles and a massive memory window from approximately 100 Ω in the LRS to nearly 7 M Ω in the HRS. Reliability was assessed via retention and endurance tests. The device demonstrates exceptional non-volatile retention (Fig. 2(h)), maintaining stable states for over 3.6×10^3 s. Furthermore, it exhibits robust fatigue resistance, sustaining over 3×10^4 measured switching cycles (Fig. 2(i)). To assess array-level reliability, we statistically analyzed the conductance

stability of multiple devices over 10^4 cycles (Figs. S7 and S8, in the Electronic Supplementary Material (ESM)), where the consistent LRS performance and low absolute HRS leakage current, enabled by a high ON/OFF ratio ($> 10^5$), provide a robustly defined memory window. Although the experimental setup limited the continuous cycling test, the resistance states exhibited negligible drift. A logarithmic extrapolation model was employed, as it

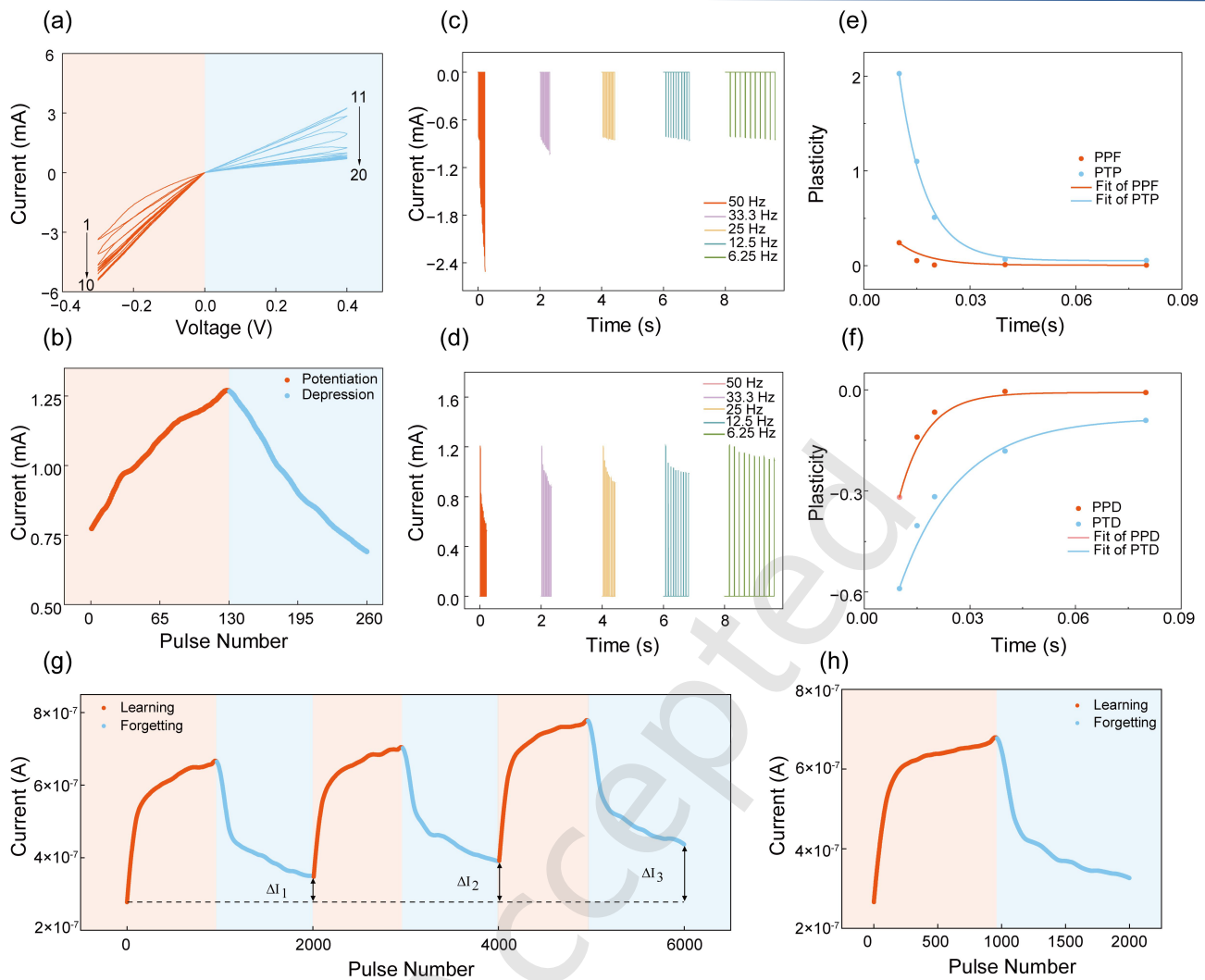


Figure 3 Emulation of biological synaptic functions and plasticity dynamics. (a) Analog conductance modulation under consecutive negative (potentiation) and positive (depression) DC sweeps. (b) Linearity of LTP and LTD characteristics under 130 potentiation pulses (-1 V) and 130 depression pulses (+1.6 V). (c, d) Spike-rate-dependent plasticity (SRDP) demonstrating (c) potentiation and (d) depression behaviors under different stimulation frequencies from 6.25 Hz to 50 Hz. (e, f) Short-term plasticity dynamics including (e) PPF/PTP and (f) PPD/PTD. The solid lines represent the fitting results using a double-exponential decay function. (g, h) Emulation of the “forgetting curve” and the “savings effect” during the transition from STM to LTM, showing the conductance decay after (g) a relearning process and (h) a single stimulation train.

accurately captures the diffusion-limited accumulation of residual Ag and the intrinsic structural relaxation of the Sb_2Se_3 matrix. Based on this physical model, the projected endurance lifetime exceeds 10^6 cycles before the memory window collapses, indicating sufficient reliability for neuromorphic inference applications.

To elucidate the physical origins of the observed bipolar switching, a dynamic mechanism driven by the synergistic migration of Ag cations and Se vacancies (V_{Se}) is proposed, as schematically illustrated in Figs. 2(j)–2(m). Initially, the device resides in the HRS, characterized by a stochastic distribution of mobile species within the Sb_2Se_3 matrix (Fig. 2(j)). Upon the application of a negative bias (SET process, Fig. 2(k)), the electric field drives the electromigration of pre-existing Ag^+ ions towards the Ag top electrode. Crucially, this process is accompanied by the drift of positively charged V_{Se} under the electric field [5,38,44]. These vacancies serve as preferential hopping sites and diffusion channels, lowering the activation energy for Ag migration within the chalcogenide lattice [50,51]. The accumulation of Ag^+ at the cathode interface facilitates their electrochemical reduction, leading to the nucleation and growth of conductive filaments. The complete

bridging of the electrodes by these metallic Ag filaments marks the transition to the LRS (Fig. 2(l)), which structurally corroborates the Ohmic conduction behavior identified in the electrical analysis.

Conversely, the RESET process is governed by a thermal dissolution mechanism (Fig. 2(m)). Under a positive bias, the high current density within the filament induces localized Joule heating [25,36]. This thermal energy triggers the rupture of the metallic bridge and promotes the diffusion of Ag species back into the chalcogenide matrix, thereby restoring the HRS. It is noteworthy that the RESET voltage (+1.8 V) is significantly larger than the SET voltage (-0.15 V). This pronounced asymmetry originates from the high diffusion barrier of Ag atoms within the dense Sb_2Se_3 lattice [47]. While the formation of filaments is facilitated by the electric field-driven drift of ions along vacancy-rich paths, the dissolution process requires overcoming the substantial kinetic barrier for Ag diffusion back into the matrix [34]. Consequently, sufficient Joule heating—provided by a higher voltage—is necessary to supply the activation energy required to rupture the robust filaments and disperse the Ag species, thereby restoring the HRS.

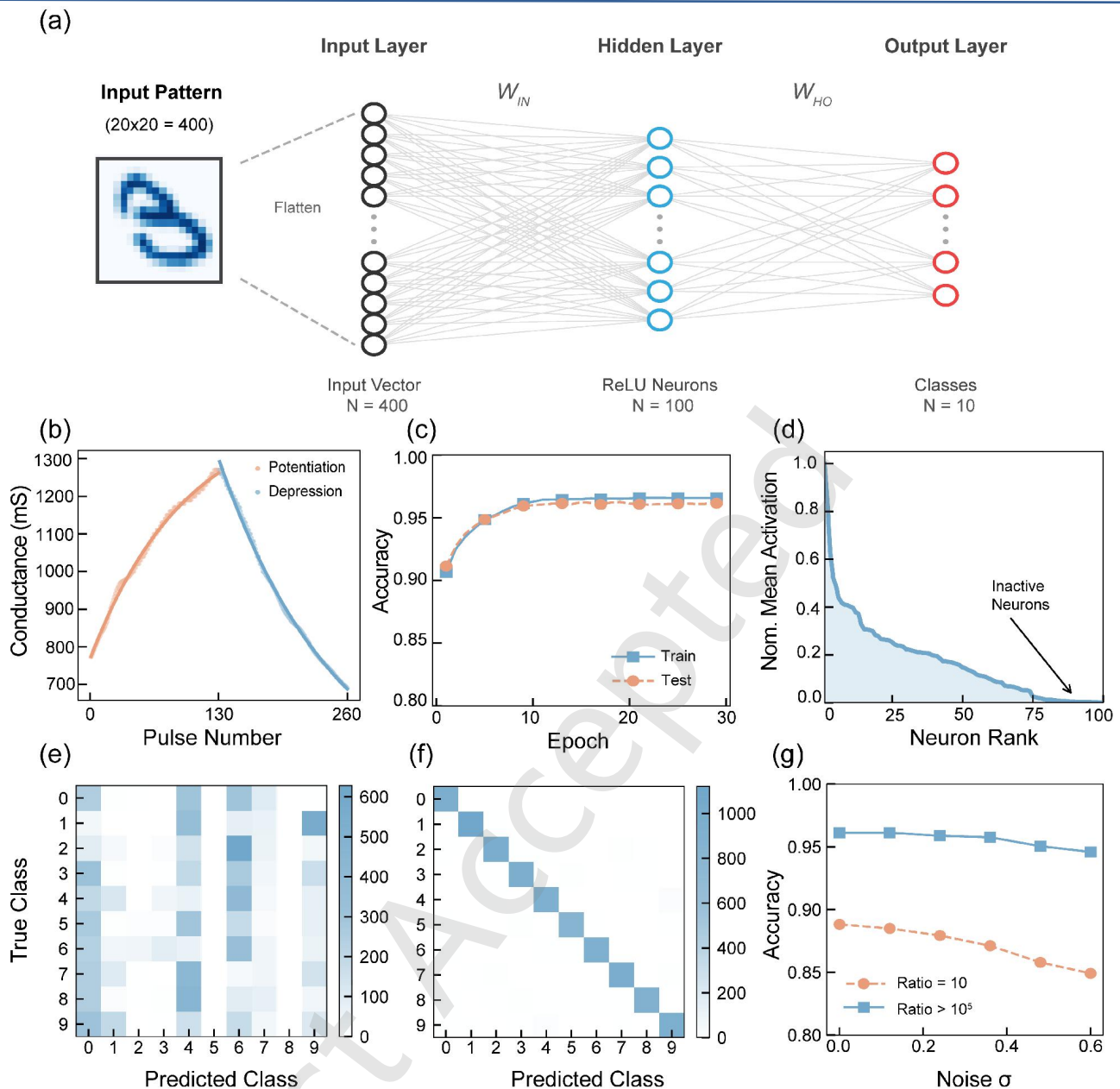


Figure 4 System-level neuromorphic simulation based on physical device parameters. (a) Schematic of the 400-100-10 MLP network architecture used for MNIST classification. (b) Experimental LTP/LTD data fitted with exponential models, demonstrating high linearity ($R^2 > 0.995$). (c) Evolution of recognition accuracy over 30 training epochs, reaching a peak of ~96.3%. (d) Experimental hidden layer sparsity analysis. The sorted mean activation profile reveals that the network operates in a highly sparse regime. This allows the high ON/OFF ratio Sb_2Se_3 devices to effectively minimize static power, whereas low-ratio devices suffer from leakage even in inactive states. (e, f) Confusion matrices for (e) the initial random state and (f) the trained state, demonstrating precise classification capabilities. (g) Noise robustness evaluation. The high ON/OFF ratio device (blue) maintains high accuracy under increasing noise, whereas the low-ratio baseline (orange) suffers from performance collapse due to TIA readout saturation induced by high leakage currents.

3.3 Bio-Synaptic Emulation and Plasticity Dynamics

Beyond binary storage, the device exhibits analog switching capabilities essential for emulating biological synaptic functions[20,44,52]. Fig. 3 illustrates the response of the device to various electrical stimuli, mimicking synaptic plasticity. Conductance modulation was first investigated under consecutive DC sweeps (Fig. 3(a)), where repeated negative and positive sweeps triggered gradual potentiation and depression, respectively. Dynamic modulation was further validated using pulse stimulation (Fig. 3(b)). Application of 130 consecutive potentiation pulses induced a highly linear current increase from

roughly 0.78 mA to 1.28 mA, while 130 subsequent depression pulses returned the device to its initial state. This high linearity and symmetry in weight updates are crucial for accurate synaptic emulation[29,45].

The device also demonstrates spike-rate-dependent plasticity (SRDP), a biological rule where synaptic weight is regulated by impulse frequency. As shown in Figs. 3(c) and 3(d), high-frequency stimulation (50 Hz) induces significant potentiation or depression, whereas low-frequency stimulation (6.25 Hz) results in negligible weight changes. This frequency-dependent response effectively mimics the high-pass filtering characteristics of biological synapses[53–55].

Short-term plasticity (STP) dynamics were quantified via

Table 1 Comparison of performance metrics among Sb- and Bi-based chalcogenide memristors.

Device Material	Preparation Method	Structure	Set / Reset	ON/OFF Ratio	Endurance (Cycles)	MNIST Accuracy	Ref.
Sb ₂ S ₃	Hydrothermal	Ag/PMMA /Sb ₂ S ₃ /FTO	+2.0 / -3.0	10 ²	1,500	93.09%	[44]
Sb ₂ Se ₃	Solution-processed	Ag/Sb ₂ Se ₃ /HZO /Si	+1.0 / -0.9	> 10	>10,000	90.33%	[45]
Bi ₂ Te _{2.7} Se _{0.3}	PLD	Bi ₂ Te _{2.7} Se _{0.3} /SnSe	+0.6 / -0.6	10 ²	10,000	97.68%	[53]
Bi ₂ S ₃	Solvothermal	Ag/Bi ₂ S ₃ /TiN	+1.0 / -1.5	~ 6	>1,000	86.25%	[42]
Bi ₂ Se ₃	Plasma Injection	Au/Bi ₂ Se ₃ /SiO ₂	+1.2 / -0.6	> 10 ⁴	300	—	[41]
Sb ₂ Se ₃	RTE	Ag/Sb ₂ Se ₃ /ITO	-0.28 / +1.82	~ 10 ⁵	>30,000	96.30%	(This Work)

paired-pulse facilitation (PPF) and depression (PPD)[39,56]. The plasticity indices decay exponentially with increasing pulse interval (Δt). To elucidate the relaxation kinetics, the decay curves in Figs. 3(e) and 3(f) were fitted using a double-exponential function:

$$Y = y_0 + A_1 \exp(-t/\tau_1) + A_2 \exp(-t/\tau_2)$$

where y represents the plasticity index (PPF/PPD ratio), y_0 is a constant offset, A_1 and A_2 are the amplitudes of the fast and slow decay components, and τ_1 and τ_2 denote the corresponding characteristic relaxation times. The fitting yielded specific time constants: for potentiation (Fig. 3(e)), the fast and slow relaxation times (τ_1/τ_2) were 7.5 ms / 9.1 ms (PPF) and 6.6 ms / 8.0 ms (PTP). Similarly, for depression (Fig. 3(f)), the constants were 7.0 ms / 8.6 ms (PPD) and 15.3 ms / 18.7 ms (PTD). These millisecond-scale dynamics suggest the coexistence of fast electronic processes and slower ionic migration[57].

Finally, the transition from short-term memory (STM) to long-term memory (LTM) was simulated (Figs. 3(g), 3(h)). While the conductance decays naturally after a single stimulus train, repeated training (“relearning”) after a delay significantly elevates the baseline conductance and retards the decay rate. This phenomenon, known as the “savings effect”, confirms that the Sb₂Se₃ synapse supports memory consolidation through repetition, enabling hardware-level learning comparable to biological systems[26,58].

3.4 Potential Applications: System-Level Neuromorphic Simulations

To bridge the gap between single-device physics and system-level computational performance, we constructed a physics-based hardware-aware simulation framework. This framework evaluates the potential of the Ag/Sb₂Se₃/ITO memristor in

artificial neural networks (ANNs). A three-layer fully connected multilayer perceptron (MLP) was designed to perform the standard MNIST handwritten digit recognition task (Fig. 4(a))[15,16,59]. First, to accurately quantify the analog conductance modulation, the experimental long-term potentiation (LTP) and depression (LTD) data were fitted using the exponential model:

$$G(P) = G_{\min} + A(1 - e^{-vP}) / (1 - e^{-vP_{\max}}) \quad (2)$$

(Fig. 4(b)). The device exhibits excellent linearity, with extracted nonlinearity factors (v) of 1.35 for potentiation and -0.87 for depression ($R^2 > 0.995$). This high linearity ensures precise weight updates, serving as the physical foundation for rapid network convergence[21,45].

Based on these physical parameters, the training simulation was conducted. Fig. 4(c) illustrates the evolution of recognition accuracy, ultimately reaching 96.3%. To reveal the mechanism behind this efficiency, we analyzed the sparsity of the hidden layer neurons (Fig. 4(d)). The network operates in a highly sparse regime where most neurons remain inactive. This algorithmic sparsity perfectly aligns with the high OFF-state resistance (High R_{OFF}) of our device[1]. In our system, devices corresponding to inactive neurons generate negligible static leakage, enabling true event-driven low-power computing[1,60]. In contrast, low-switching-ratio devices generate significant background leakage even in the OFF-state. The precise classification capability is further visualized by the confusion matrices for the initial and trained states (Figs. 4(e), 4(f)), showing a clear diagonal alignment after training.

Critically, a robustness experiment (Fig. 4(g)) elucidated the decisive advantage of the high ON/OFF ratio. We compared the Sb₂Se₃ device (Ratio $\approx 10^5$) against a typical low-ratio baseline (Ratio ≈ 10) under varying input noise. As noise increased, the accuracy of the low-ratio device

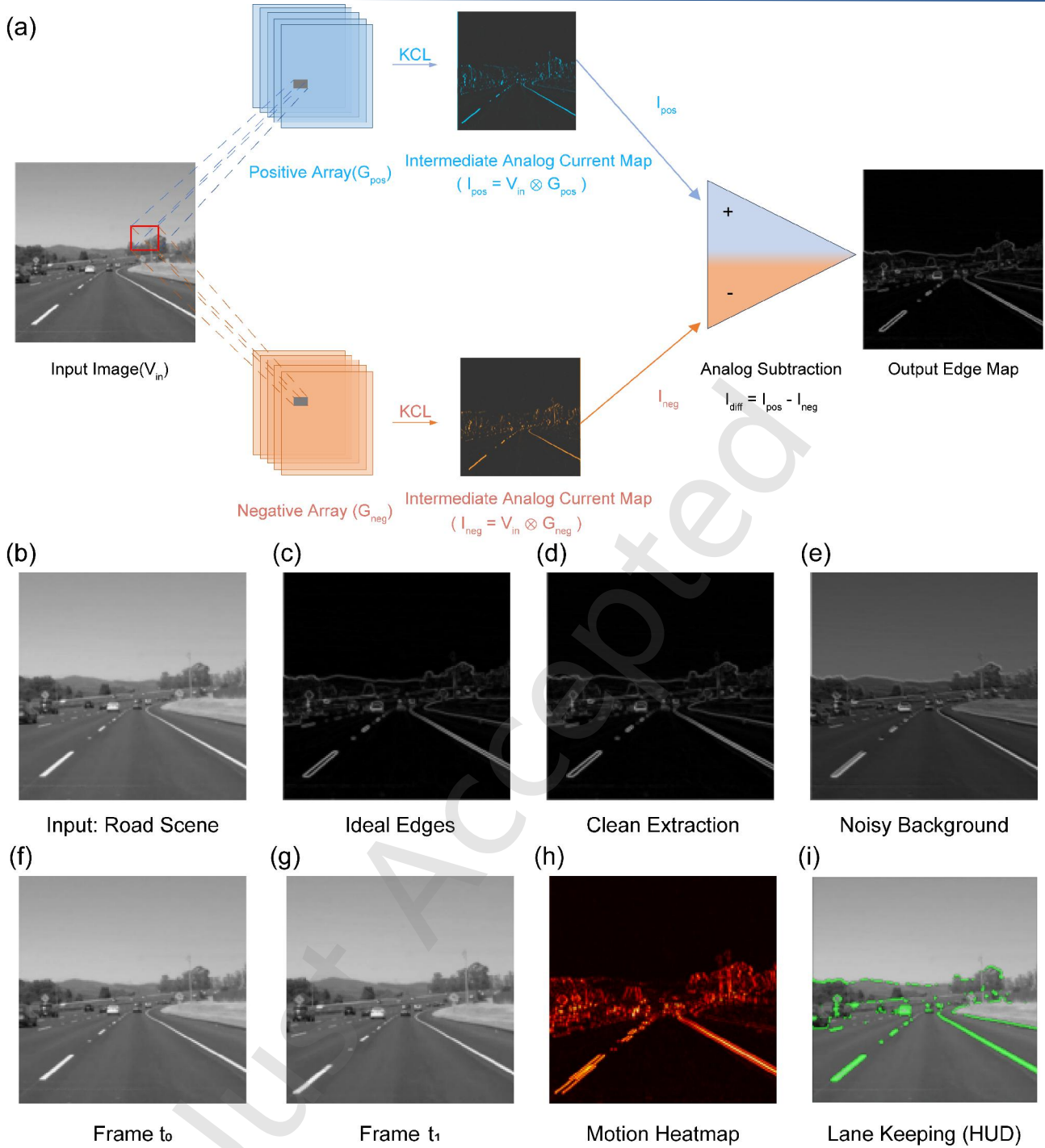


Figure 5 Bio-inspired neuromorphic computing system based on parallel analog computing. (a) Schematic of the physics-aware convolution engine. Input signals (V_{in}) are processed by Positive (G_{pos}) and Negative (G_{neg}) arrays via KCL to produce Intermediate Analog Current Maps (I_{pos}, I_{neg}). A subsequent Analog Subtraction stage (I_{diff}) extracts signed edges while suppressing common-mode leakage. (b) Input: Road Scene. (c) Ideal Edges. (d) Clean Extraction using High- R_{off} Ag/Sb₂Se₃/ITO devices. (e) Noisy Background in low-ratio baseline simulation (I_{leak}). (f–g) Sequential frames (t_0, t_1). (h) Motion Heatmap via temporal differencing. (i) Lane Keeping (HUD) application.

collapsed ($\sim 85\%$), while our device maintained robust performance ($> 94\%$). This divergence stems from the limited dynamic range of array-level readout circuits. In low-ratio arrays, the massive accumulation of common-mode leakage current saturates the transimpedance amplifier (TIA), causing signal clipping[12,18]. Conversely, the Ag/Sb₂Se₃/ITO device utilizes its high ON/OFF ratio to provide intrinsic leakage suppression, effectively reserving the circuit's dynamic headroom for extracting valid signals. Further quantitative evaluations regarding alternative readout modes (e.g., dynamic gain) and the RC settling limits associated with the high resistance state are

provided (Tables S4 and S5, in the Electronic Supplementary Material (ESM)).

To contextualize this superior noise immunity within the broader landscape of chalcogenide memristors, we benchmark our device against state-of-the-art counterparts. Table 1 compares the key performance metrics of our RTE-fabricated Sb₂Se₃ device with other reported antimony- and bismuth-based chalcogenide memristors. Our work stands out by simultaneously achieving a large switching window, high endurance, and superior system-level accuracy. While other works may excel in single parameters, the balanced combination

of a 10^5 ON/OFF ratio and high linearity in our device provides a distinct advantage for reliable neuromorphic computing.

3.5 Potential Applications: Complex Motion Perception and Dynamic Processing

To elucidate the system-level viability for intricate edge computing tasks, we constructed a bio-inspired hardware convolution engine (Fig. 5(a)) [4,19]. In this dual-pathway architecture, the sensory input signal (V_{in}) is concurrently processed by two parallel memristor crossbar arrays: a Positive Array (G_{pos}) and a Negative Array (G_{neg}), where synaptic weights are physically mapped as differential conductance pairs [3]. The convolution operation is executed in the analog domain via Kirchhoff's Current Law (KCL), generating intermediate Analog Current Maps (I_{pos}, I_{neg}) that encode the positive and negative spatial gradients, respectively. A subsequent Analog Subtraction stage ($I_{diff} = I_{pos} - I_{neg}$) is critical, which not only reconstructs the signed edge features but also effectively suppresses the common-mode leakage current, thereby maximizing the output dynamic range and signal fidelity.

We evaluated the edge extraction performance using a complex real-world driving scenario (Fig. 5(b)) [61]. Figure 5(c) presents the "Ideal Edges" digital ground truth. The reconstruction result based on our high-ON/OFF ratio Ag/Sb₂Se₃/ITO devices is shown in Fig. 5(d) ("Clean Extraction"). Exploiting the device's ultra-low off-state leakage, the system achieves sharp lane markers and distinct environmental boundaries, exhibiting a signal-to-noise ratio (SNR) comparable to the ideal case [28,62]. In stark contrast, simulations using low-ratio baseline devices (Fig. 5(e)) reveal a "Noisy Background." Here, the substantial leakage current (I_{leak}) from unselected devices accumulates, severely compressing readout margins and degrading feature contrast, resulting in compromised structural details. To quantitatively evaluate the edge intelligence performance, the hardware-aware outputs were compared with ideal reference algorithms, yielding an edge-extraction SSIM of 0.573 ± 0.017 and an mIoU of 0.579 ± 0.008 for the high-ON/OFF device under an input noise of $\sigma = 0.05$. (Table. S6, in the Electronic Supplementary Material (ESM))

Furthermore, dynamic spatiotemporal processing capabilities are demonstrated in Figs. 5(f)–5(i). Two consecutive temporal frames, t_0 (Fig. 5(f)) and t_1 (Fig. 5(g)), are processed to simulate forward ego-motion. By computing the inter-frame analog difference, the system generates a Motion Heatmap (Fig. 5(h)) that highlights the expansion field dynamics associated with the moving vehicle [13,44]. Finally, leveraging the high-fidelity edge extraction demonstrated in Fig. 5(d), we illustrate a high-level driver assistance application: the Lane Keeping (HUD) interface shown in Fig. 5(i). Here, the analog-computed lane edges are accurately superimposed onto the input stream, providing real-time navigational cues [2].

4 Conclusions

In summary, we have successfully demonstrated a high-performance neuromorphic perception hardware platform based on Ag/Sb₂Se₃/ITO memristors. Enabled by our unique pressure-regulated RTE technique, we successfully reconciled the intrinsic trade-off between switching dynamics and leakage suppression. This optimized synthesis process yields a dense microstructure that supports the coexistence of a substantial ON/OFF ratio ($>10^5$) and excellent analog linearity within a single device. Leveraging these dual characteristics, our hardware-aware simulations confirmed that the high linearity ensures precise learning, yielding a recognition accuracy of 96.3% on the MNIST dataset. Simultaneously, the high ON/OFF

ratio functions as an intrinsic physical barrier against array-level leakage, allowing the system to maintain robust performance ($>94\%$ accuracy) even under severe noise conditions where conventional low-ratio devices fail. Furthermore, we validated the system's capability in complex dynamic spatiotemporal tasks, specifically realizing expansion optical flow estimation for motion perception. For real-world edge computing scenarios, this inherent leakage suppression significantly reduces static power consumption, while the exceptional noise robustness ensures high system reliability when processing unstructured data. This work validates that the RTE-processed Sb₂Se₃ synapse is a critical enabler for constructing reliable, noise-resilient, and energy-efficient edge perception systems.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

Z. N. W.: Investigation, Formal analysis, Data curation, Visualization, Writing – original draft. C. S. S.: Investigation, Methodology, Validation, Data curation. H. Y. C.: Investigation, Validation, Formal analysis. X. S. L., X. Z., J. C. Z., and H. L. L.: Conceptualization, Supervision, Resources, Funding acquisition, Project administration, Writing – review & editing. All authors have approved the final manuscript.

Informed consent

Not applicable

Ethics statement

Not applicable

Use of AI statement

None.

References

- [1] Gao, C.; Liu, M.; Aierken, A.; Liu, X.; Wang, D.; Wang, Z.; Wang, G.; Wu, Y.; Zhou, G.; Chen, H. et al. A dynamic adaptive activation neuron-transistor for dynamic sparse neural networks in advanced driving assistance system. *Adv. Funct. Mater.* 2026, 36, e17785.
- [2] Zhang, G.; Fan, X.; Wang, J.; Wang, Z.; Zhang, Z.; Li, P.; Ma, Y.; Huang, K.; Yu, B.; Wan, Q. et al. Self-rectifying memristors with high rectification ratio for attack-resilient autonomous driving systems.

- Nat. Commun.* 2025, 16, 5759.
- [3] Wang, S.; Gao, S.; Tang, C.; Occhipinti, E.; Li, C.; Wang, S.; Wang, J.; Zhao, H.; Hu, G.; Nathan, A. et al. Memristor-based adaptive neuromorphic perception in unstructured environments. *Nat. Commun.* 2024, 15, 4671.
 - [4] Cui, K.; Rao, S.; Xu, S.; Huang, Y.; Cai, X.; Huang, Z.; Wang, Y.; Feng, X.; Liu, F.; Zhang, W. et al. Spectral convolutional neural network chip for in-sensor edge computing of incoherent natural light. *Nat. Commun.* 2025, 16, 81–90.
 - [5] Chen, M.; Ki, S. J.; Liang, X. Bi₂Se₃-based memristive devices for neuromorphic processing of analogue video signals. *ACS Appl. Electron. Mater.* 2023, 5, 3831–3842.
 - [6] Lee, Y.; Rhee, H.; Kim, G.; Cheong, W. H.; Kim, D. H.; Song, H.; Kay, S. N.; Lee, J.; Kim, K. M. Flexible self-rectifying synapse array for energy-efficient edge multiplication in electrocardiogram diagnosis. *Nat. Commun.* 2025, 16, 4312.
 - [7] Ortner, T.; Petschenig, H.; Vasilopoulos, A.; Renner, R.; Brglez, Š.; Limbacher, T.; Piñero, E.; Linares-Barranco, A.; Pantazi, A.; Legenstein, R. Rapid learning with phase-change memory-based in-memory computing through learning-to-learn. *Nat. Commun.* 2025, 16, 1243.
 - [8] Xia, Z.; Sun, X.; Wang, Z.; Meng, J.; Jin, B.; Wang, T. Low-power memristor for neuromorphic computing: from materials to applications. *Nano-Micro Lett.* 2025, 17, 217–241.
 - [9] Ielmini, D.; Wong, H.-S. P. In-memory computing with resistive switching devices. *Nat. Electron.* 2018, 1, 333–343.
 - [10] Sebastian, A.; Le Gallo, M.; Khaddam-Aljameh, R.; Eleftheriou, E. Memory devices and applications for in-memory computing. *Nat. Nanotechnol.* 2020, 15, 529–544.
 - [11] Tan, D.; Luo, Z.-D.; Yang, Q.; Xiao, F.; Gan, X.; Zhang, D.; Chu, Z.; Xue, F.; Zhang, J.; Xia, Y. et al. Reconfigurable logic and in-memory computing based on electrically controlled charge trapping in dielectric engineered 2D semiconductor transistors. *Adv. Funct. Mater.* 2025, 35, 2417887.
 - [12] Gao, K.; Sun, B.; Cao, Z.; Wang, M.; Zhang, J.; Wang, K.; Zhou, G.; Lu, Z.; Shao, J. Brain-inspired computing based on large-scale memristor crossbar arrays. *Adv. Funct. Mater.*, in press, DOI: 10.1002/adfm.202528309.
 - [13] Yang, F.; Jang, Y.; Wang, C.; Liang, J.; Li, Y. Metal oxide-based neuromorphic artificial visual perception devices and systems for information perception, memory and processing. *Adv. Funct. Mater.* 2026, 36, e15213.
 - [14] He, S.; Zhong, W.; Zhu, M.; Wu, S.; Xie, W.; Ouyang, Z.; Cheng, B.; Zhao, J. In-memory computing with self-rectification and dynamic logical reconfiguration of 12 algorithms in a single halide perovskites. *Adv. Funct. Mater.* 2025, 35, 2424114.
 - [15] Prezioso, M.; Merrih-Bayat, F.; Hoskins, B. D.; Adam, G. C.; Likharev, K. K.; Strukov, D. B. Training and operation of an integrated neuromorphic network based on metal-oxide memristors. *Nature* 2015, 521, 61–64.
 - [16] Li, C.; Hu, M.; Li, Y.; Jiang, H.; Ge, N.; Montgomery, E.; Zhang, J.; Song, W.; Dávila, N.; Graves, C. E. et al. Analogue signal and image processing with large memristor crossbars. *Nat. Electron.* 2017, 1, 52–59.
 - [17] Choi, S.; Bezugam, S. S.; Bhattacharya, T.; Kwon, D.; Strukov, D. B. Wafer-scale fabrication of memristive passive crossbar circuits for brain-scale neuromorphic computing. *Nat. Commun.* 2025, 16, 8757.
 - [18] Nguyen, T. V.; An, J.; Min, K.-S. Memristor-CMOS hybrid neuron circuit with nonideal-effect correction related to parasitic resistance for binary-memristor-crossbar neural networks. *Micromachines* 2021, 12, 791–808.
 - [19] Kim, G.; Youn, S.; Park, J.; Kim, H. Configurable kernel map implementation in memristor crossbar for convolution neural network. *Adv. Intell. Syst.* 2025, 7, 2500032.
 - [20] Li, Y.; Xiong, Y.; Zhang, X.; Yin, L.; Yu, Y.; Wang, H.; Liao, L.; He, J. Memristors with analogue switching and high on/off ratios using a van der waals metallic cathode. *Nat. Electron.* 2024, 8, 36–45.
 - [21] Guan, Z.; Wang, Z.; Shen, S.; Yin, Y.; Li, X. Symmetric and energy-efficient conductance update in ferroelectric tunnel junction for neural network computing. *Adv. Mater. Technol.* 2024, 9, 2302238.
 - [22] Yu, H.; Liu, H.; Li, L.; Duan, X.; Peng, Z.; Lu, L.; Lin, X.; Chang, K.-C. Integration of non-volatile multi-bit storage and logic computing in GaN enhancement-mode devices for In-memory computing. *Adv. Funct. Mater.* 2026, 36, e13256.
 - [23] Kim, D.-e.; Chabungbam, A. S.; Kim, G.; Son, J.; Lim, B. M.; Lee, Y. M.; Kim, S. J.; Kim, M.; Lee, H.-S.; Park, H.-H. Doping engineering for optimized self-rectifying TaO_x memristor for crossbar array neuromorphic applications. *Adv. Funct. Mater.* 2025, 35, 2503883.
 - [24] Tan, T.; Sivan, M.; Zhou, K.; Guo, H.; Wu, Y.; Sun, L.; Li, Y.; Feng, X. Self-rectifying MoS₂ memristor via asymmetry contact metal engineering for neuromorphic computing. *Small*, in press, DOI: 10.1002/sml.202503716.
 - [25] Sun, P.; Lu, N.; Li, L.; Li, Y.; Wang, H.; Lv, H.; Liu, Q.; Long, S.; Liu, S.; Liu, M. Thermal crosstalk in 3-dimensional RRAM crossbar array. *Sci. Rep.* 2015, 5, 13504.
 - [26] Li, H.; Liao, Z.; Kataoka, R.; Shamim, M. S.; Kijima, T.; Yamahara, H.; Tabata, H.; Seki, M. Enhanced switching performance in single-crystalline PbTiO₃ ferroelectric memristors for replicating synaptic plasticity. *Adv. Funct. Mater.* 2026, 36, e10715.
 - [27] Guo, T.; Pan, Z.; Shen, Y.; Yang, J.; Chen, C.; Xiong, Y.; Chen, X.; Song, Y.; Huo, N.; Xu, R. et al. Oxygen vacancy induced 2D Bi₂SeO₃ non-volatile memristor for 1T1R integration. *Nano Lett.* 2025, 25, 8258–8266.
 - [28] Chai, T.; Xu, C.; Wang, Y.; Zheng, L.; Hu, K.; Zhang, K.; Zhu, M. Lead-free perovskite based self-rectifying memristor with self-organizing heterojunction for energy-efficient image information sensing, processing, and protection. *Adv. Funct. Mater.*, in press, DOI: 10.1002/adfm.202522022.
 - [29] Zhu, J.; Liu, C.; Gao, R.; Zhang, Y.; Zhang, H.; Cheng, S.; Liu, D.; Wang, J.; Liu, Q.; Wang, Z. et al. Ultra-flexible high-linearity silicon nanomembrane synaptic transistor array. *Adv. Mater.* 2025, 37, 2413404.
 - [30] Liu, Z.; Tang, J.; Gao, B.; Yao, P.; Li, X.; Liu, D.; Zhou, Y.; Qian, H.; Hong, B.; Wu, H. Neural signal analysis with memristor arrays towards high-efficiency brain-machine interfaces. *Nat. Commun.* 2020, 11, 4234.
 - [31] He, B.; Bao, B.; Martins, R.; Wang, S.; He, G. Frame-channel engineered multimodal transistor integrating neuromorphic computing with cross-modal edge intelligence. *Adv. Funct. Mater.* 2025, 35, 2506332.
 - [32] Liu, J.; Chen, Z.; Wu, C.; Yu, X.; Yu, X.; Chen, C.; Li, Z.; Qiao, Q.; Cao, Y.; Zhou, Y. Recent advances in antimony selenide photodetectors. *Adv. Mater.* 2024, 36, 2406028.
 - [33] Jakomin, R.; Rampino, S.; Spaggiari, G.; Pattini, F. Advances on Sb₂Se₃ solar cells fabricated by physical vapor deposition techniques. *Solar* 2023, 3, 566–595.
 - [34] Li, T.; He, X.; Yang, J.; Nazarov, R. S.; Deribina, E. I.; Kapitonov, Y.; Wu, J.; Cui, X.; Li, Y.; Zhai, T. Recent research progress of antimony-based two-dimensional materials for electronics and optoelectronics. *Adv. Mater.* 2025, 37, 2503509.
 - [35] Liu, C.; Yuan, Y.; Cheng, L.; Su, J.; Zhang, X.; Li, X.; Zhang, H.; Xu, M.; Li, J. A study on optical properties of Sb₂Se₃ thin films and resistive switching behavior in Ag/Sb₂Se₃/W heterojunctions. *Results Phys.* 2019, 13, 102228.
 - [36] Zhou, G.; Gu, D.; Ye, J.; Sun, B.; Shi, H.; Ran, H.; Ji'e, M.; Hu, X.; Wang, L.; Duan, S. et al. Anomalous phase change in SbSe_x memristors for ultrafast image encryption. *Adv. Mater.* 2025, 37, e08107.
 - [37] Luo, P.; Imran, T.; Ren, D.-L.; Zhao, J.; Wu, K.-W.; Zeng, Y.-J.; Su, Z.-H.; Fan, P.; Zhang, X.-H.; Liang, G.-X. et al. Electron transport layer engineering induced carrier dynamics optimization for efficient Cd-free Sb₂Se₃ thin-film solar cells. *Small* 2024, 20, 2306516.

- [38] Peng, K.; Wu, Z.; Liu, X.; Yang, J.; Guan, Z. Suppressing Se vacancies in Sb_2Se_3 photocathode by In situ annealing with moderate Se vapor pressure for efficient photoelectrochemical water splitting. *Small* 2025, 21, 2406035.
- [39] Nandi, S.; Ghosal, S.; Choudhary, G.; Roy, S. S.; Meyyappan, M.; Giri, P. K. Tellurium-vacancy engineering in ultrathin Bi_2Te_3 enables broadband multifunctional optoelectronic synapse for energy-efficient neuromorphic and optical information processing. *Small*, in press, DOI: 10.1002/sml.202511836.
- [40] Ren, X.; He, X.; Duan, Z.; An, X.; Li, Y.; Gao, F.; Zhang, J.; Hu, P. Self-powered and broadband optical synapse device based on Se-vaporized $\text{Bi}_2\text{O}_3\text{Se}$ for artificial vision system application. *ACS Photonics* 2024, 11, 4991–4999.
- [41] Yin, C.; Gong, C.; Tian, S.; Cui, Y.; Wang, X.; Wang, Y.; Hu, Z.; Huang, J.; Wu, C.; Chen, B. et al. Low-energy oxygen plasma injection of 2D Bi_2Se_3 realizes highly controllable resistive random access memory. *Adv. Funct. Mater.* 2022, 32, 2108455.
- [42] Harke, S. S.; Kapur, O.; Dai, P.; Zhang, T.; Ding, B.; Ding, B.; Huang, R.; Gurnani, C. Solution-processed Bi_2S_3 nanostructures for flexible memory and neuromorphic computing. *Adv. Electron. Mater.* 2025, 11, e00370.
- [43] Gao, S.; Liu, G.; Chen, Q.; Xue, W.; Yang, H.; Shang, J.; Chen, B.; Zeng, F.; Song, C.; Pan, F. et al. Improving unipolar resistive switching uniformity with cone-shaped conducting filaments and its logic-In-memory application. *ACS Appl. Mater. Interfaces* 2018, 10, 6453–6462.
- [44] Yang, Y.; Yang, Y.; Xiong, S.; Wang, Y.; Hu, K.; Wang, F.; Li, X.; Feng, L.; Guo, H.; Zheng, L. et al. Bio-inspired Sb_2S_3 memristors supporting dual-mode operation via self-regulating transport pathways for all-in-one neuromorphic perception and computation. *Adv. Funct. Mater.* 2026, 36, e10212.
- [45] Jiang, S.; Yang, Y.; Gu, J.; Zhang, J.; Chen, X.; Zhang, Z.; Su, J.; Qiu, J.; Guo, H.; Xu, Q. et al. Robust Sb_2Se_3 /hafnium zirconium oxide synaptic memristors with dynamic learning rate strategy for generalizable neuromorphic networks. *Adv. Funct. Mater.*, in press, DOI: 10.1002/adfm.202527371.
- [46] Khan, R.; Rehman, N. U.; Iqbal, S.; Abdullaev, S.; Aldosari, H. M. Resistive switching properties in memristors for optoelectronic synaptic memristors: deposition techniques, key performance parameters, and applications. *ACS Appl. Electron. Mater.* 2024, 6, 73–119.
- [47] Liu, X.; Liu, Y.; Zhang, S.; Sun, X.; Zhuang, Y.; Liu, J.; Wang, G.; Cheng, K.; Du, Z. Regulating deposition pressures during rapid thermal evaporation processes to enable efficient Sb_2Se_3 solar cells. *Small Methods* 2024, 8, 2300728.
- [48] Xu, J.; Zhang, Y.; Wang, J.; Zhang, W.; Li, T.; Zhang, K.; Yan, X. Ultra-low power and robust Bi_2SeO_5 films optoelectronic memristors for bio-visual perception computing systems. *Adv. Mater.* 2025, 37, 2509174.
- [49] Ding, G.; Wang, Y.; Zhang, G.; Zhou, K.; Zeng, K.; Li, Z.; Zhou, Y.; Zhang, C.; Chen, X.; Han, S.-T. 2D metal–organic framework nanosheets with time-dependent and multilevel memristive switching. *Adv. Funct. Mater.* 2019, 29, 1806637.
- [50] Aleshin, A. N.; Ruban, O. A. Estimation of the activation energy in the $\text{Ag}/\text{SnSe}/\text{Ge}_2\text{Se}_3/\text{W}$ self-directed channel memristor. *Mod. Electron. Mater.* 2023, 9, 115–122.
- [51] Gubicza, A.; Manrique, D. Z.; Pósa, L.; Lambert, C. J.; Mihály, G.; Csontos, M.; Halbritter, A. Asymmetry-induced resistive switching in $\text{Ag-Ag}_2\text{S-Ag}$ memristors enabling a simplified atomic-scale memory design. *Sci. Rep.* 2016, 6, 30775.
- [52] Jang, S.; Soh, K.; Lee, C.; Nam, T.; Jang, M.; Park, J.-i.; Lee, C.; Choi, J.; Yoon, J. H.; Im, S. G. A unipolar-driven synaptic transistor for environment-adaptable vision system. *Nat. Commun.* 2025, 16, 7636.
- [53] Wang, H.; Tang, Y.; Wang, Z.; He, C.; Liu, H.; Lin, R.; Xu, W.; Chen, J.; Wang, S.; Yan, X. Efficient and stable topological/ferroelectric $\text{Bi}_2\text{Te}_3/\text{SnSe}$ hetero-memristor for In situ bionic-visual semi-hardware systems. *Adv. Mater.* 2025, 37, 2501066.
- [54] Park, H.; Jang, H.; Park, S.; Na, H.; Kim, S. Photonic encoding-driven neuromorphic and cryptographic system based on oxide semiconductor device. *Adv. Funct. Mater.*, in press, DOI: 10.1002/adfm.202520150.
- [55] Li, J. C.; Liu, Z. C.; Xia, Y. H.; Liu, X.; Yang, H. X.; Ma, Y. X.; Wang, Y. L. Room-temperature-integrated flexible diffusive oxide memristors for artificial nociceptive systems. *Adv. Funct. Mater.* 2025, 35, 2416635.
- [56] Yang, Z.; Huo, S.; Zhang, Z.; Meng, F.; Liu, B.; Wang, Y.; Ma, Y.; Wang, Z.; Xu, J.; Tian, Q. et al. High-precision multibit optoelectronic synapses based on $\text{ReS}_2/\text{h-BN}/\text{graphene}$ heterostructure for energy-efficient and high-accuracy neuromorphic computing. *Adv. Funct. Mater.* 2025, 35, 2509119.
- [57] Ma, T.; Han, S.; Yang, D.; Ye, Y.; Liu, Y.; Shen, Z.; Li, F.; Li, H.; Chen, C. Two-dimensional $\alpha\text{-In}_2\text{Se}_3$ memory devices from resistive switching to synaptic plasticity. *Appl. Phys. Lett.* 2023, 123, 263503.
- [58] Han, S.; Ma, T.; Li, H.; Wu, J.; Liu, R.; Cao, R.; Li, F.; Li, H.; Chen, C. Photoferroelectric perovskite synapses for neuromorphic computing. *Adv. Funct. Mater.* 2024, 34, 2309910.
- [59] He, Q.; Wang, H.; Zhang, Y.; Chen, A.; Fu, Y.; Xue, G.; Liu, K.; Huang, S.; Xu, Y.; Yu, B. Two-dimensional materials based two-transistor-two-resistor synaptic kernel for efficient neuromorphic computing. *Nat. Commun.* 2025, 16, 4340.
- [60] Zhou, J.; Zhang, X.; Zhang, Y.; Huang, S.; Chen, A.; Gong, Z.; Li, Z.; Wang, L.; Xue, F.; Wang, H. et al. Hardware-implemented DropConnect function for energy-efficient neuromorphic computing. *Adv. Funct. Mater.* 2025, 35, 2503452.
- [61] Geiger, A.; Lenz, P.; Stiller, C.; Urtasun, R. Vision meets robotics: The KITTI dataset. *Int. J. Rob. Res.* 2013, 32, 1231–1237.
- [62] Fan, W.; Yan, H.; Wang, X.; Tong, L.; Yan, W.; Su, C.; Wang, Q.; Yin, S. Polarization-sensitive photosynapse based on $\text{PdSe}_2/\text{WS}_2$ heterostructure for visible-infrared broadband artificial vision system. *Adv. Funct. Mater.* 2025, 35, 2416703.

Robust Sb₂Se₃ memristors via pressure-modulated growth for noise-resilient neuromorphic computing

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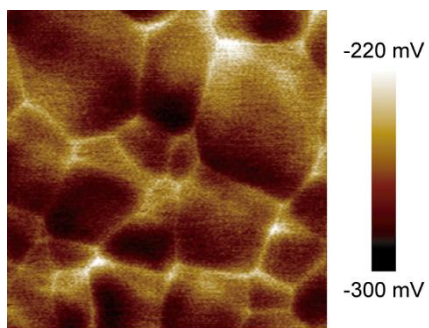


Figure S1 KPFM surface potential mapping of the Sb₂Se₃ film. The image reveals a uniform potential distribution within the grains (~ -220 mV) and distinct boundaries (~ -300 mV), indicating high electrical homogeneity and reduced defect density.

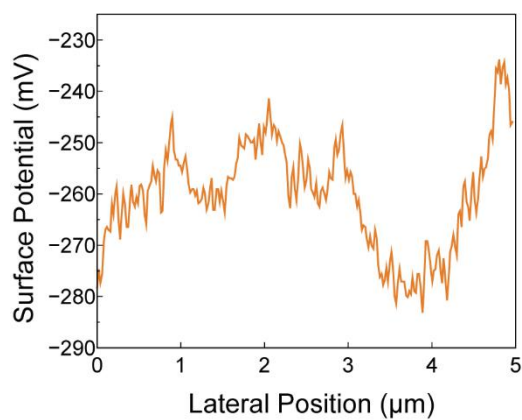


Figure S2 Cross-sectional surface potential profile extracted from the KPFM mapping. The curve reveals a periodic potential fluctuation corresponding to the polycrystalline microstructure. The grain interiors exhibit a relatively higher and stable potential (~ -240 mV), while the grain boundaries show a lower potential (~ -280 mV). The moderate potential variation (~ 40 mV) further confirms the electrical homogeneity of the RTE-processed Sb_2Se_3 film.

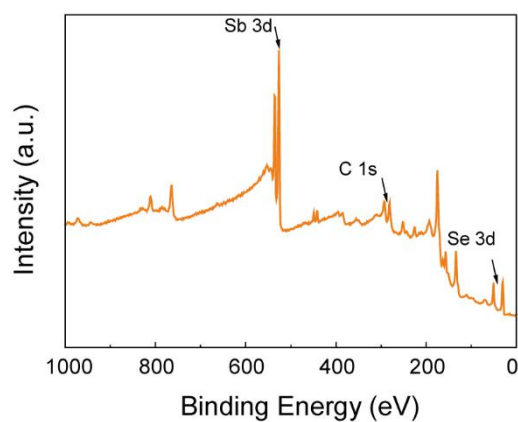


Figure S3 XPS survey spectrum of the RTE-processed Sb_2Se_3 thin film. The spectrum confirms the presence of Antimony (Sb) and Selenium (Se) as the primary constituent elements. The C 1s peak at 284.8 eV is attributed to adventitious carbon and was used for binding energy calibration. No other metallic impurity peaks were detected, indicating the high chemical purity of the functional layer.

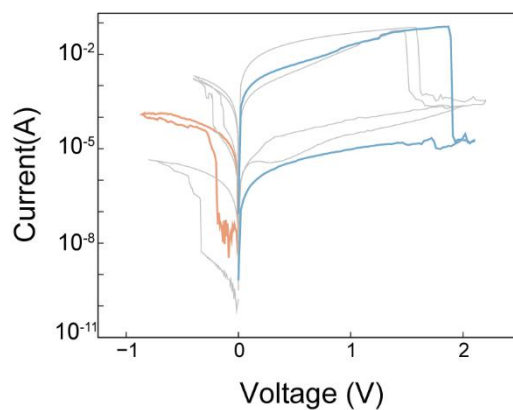


Figure S4 Complementing the analog linearity reported in the main text, the I - V curves here reveal the intrinsic binary switching capability of the Ag/Sb₂Se₃/ITO memristor. The distinct memory window and abrupt conductance changes indicate that the RTE-processed high-quality film can effectively support high-density digital storage, expanding the potential application scenarios of the proposed device.

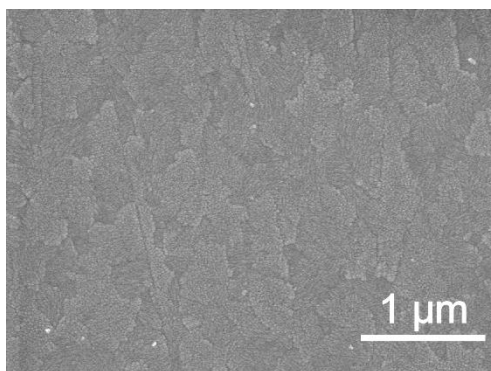


Figure S5 Top-view SEM image of the Sb₂Se₃ film deposited under an intermediate pressure of 50 Torr. The film exhibits a highly dense, fine-grained nanocrystalline morphology with abundant grain boundaries, indicating that 50 Torr is thermodynamically insufficient to suppress material re-evaporation and promote sufficient grain coarsening.

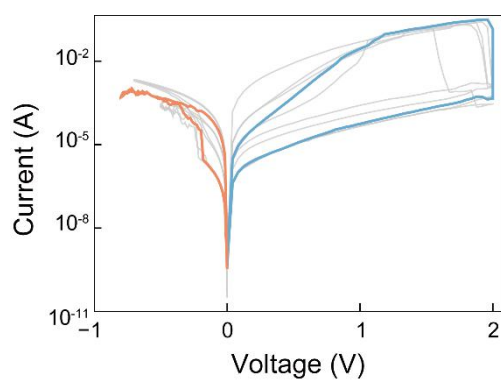


Figure S6 Bipolar I-V characteristics of the Ag/Sb₂Se₃/ITO memristor fabricated at an intermediate pressure of 50 Torr. The device exhibits a notably high off-state leakage current and a significantly degraded ON/OFF switching ratio.

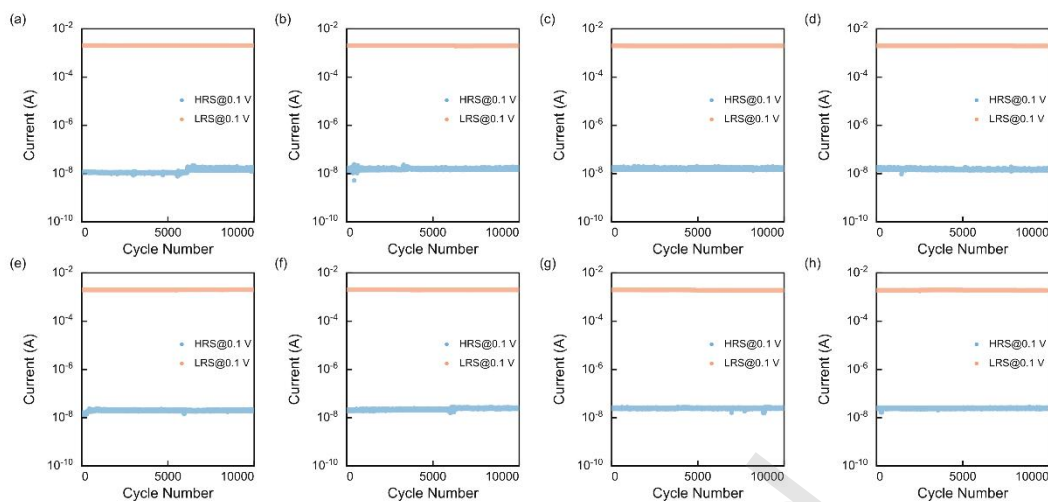


Figure S7 Endurance performance of multiple devices. (a–h) Representative endurance characteristics of 8 randomly selected Ag/Sb₂Se₃/ITO memristors over 10^4 switching cycles. The current values for both the high-resistance state (HRS) and low-resistance state (LRS) were measured at a read voltage of 0.1 V, demonstrating consistent state separation and high array-level uniformity.

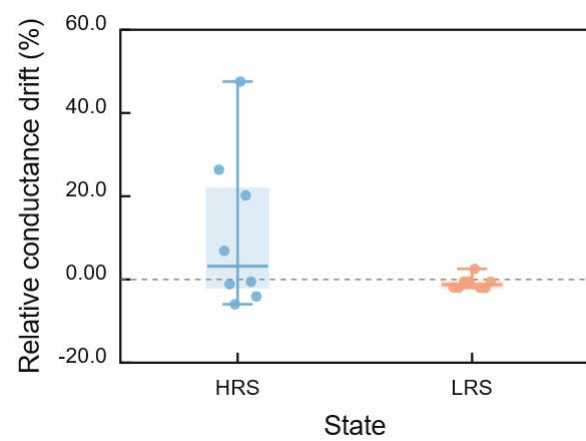


Figure S8 Statistical distribution of conductance drift. Statistical analysis of the relative conductance drift for HRS and LRS extracted from multiple devices after 10^4 cycles. The LRS exhibits minimal drift, while the HRS shows a stochastic distribution within a manageable range. The high ON/OFF ratio ($> 10^5$) ensures a robust memory window despite the observed fluctuations.

Note S1. Physics-Based Hardware-Aware Neuromorphic Simulation Framework

S1.1 Synaptic Nonlinearity Modeling To incorporate the experimental switching behavior into the neuromorphic network, the measured conductance update curves were fitted using the following nonlinear model:

$$G_P(n) = G_{\min} + (G_{\max} - G_{\min}) \frac{1 - e^{-v_P n}}{1 - e^{-v_P}} \quad (S1)$$

$$G_D(n) = G_{\max} - (G_{\max} - G_{\min}) \frac{1 - e^{-v_D n}}{1 - e^{-v_D}} \quad (S2)$$

where n represents the normalized pulse number ($n \in [0, 1]$), and $G_{\min}$ and $G_{\max}$ are the minimum and maximum conductance values, respectively. The nonlinearity factor v determines the update trajectory of the artificial synapse. Based on the experimental data fitting (Figure 4b in the main text), the extracted parameters are listed in **Table S1**.

Table S1. Extracted Simulation Parameters

Parameter	Symbol	Value (Ag/Sb ₂ Se ₃ /ITO)	Value (Baseline)
Potential Nonlinearity	v_P	1.35	1.35
Depression Nonlinearity	v_D	0.87	0.87
On/Off Ratio	$G_{\max}/G_{\min}$	$>10^5$	10
Max Conductance	$G_{\max}$	1200 μS	1200 μS
Min Conductance	$G_{\min}$	$\sim 0.12 \mu S$	120 μS

S1.2 Hardware-Aware Training Algorithm The network training utilized a custom optimizer designed to emulate the physical weight update process in a crossbar array. The simulation setup included:

Network Topology: Input layer (N=400), Hidden layer (N=100, ReLU activation), Output layer (N=10).

Weight Mapping: The synaptic weights W were mapped to the differential conductance pair (G^+ , G^-) logic. The effective weight is represented as

$$W \propto (G^+ - G^-) \quad (S3)$$

Update Logic: During backpropagation, the gradients are translated into write pulses. The conductance state of each synapse is updated according to the equations in Section S1.1, ensuring that the trained weights respect the physical nonlinearity and dynamic range of the device.

Sparsity: The use of the Rectified Linear Unit (ReLU) activation function in the hidden layer naturally induces sparsity (as shown in Figure 4d). For the high-ratio Ag/Sb₂Se₃/ITO device, inactive neurons (output = 0) correspond to the High-Resistance State (HRS), resulting in negligible leakage current.

S1.3 Readout Circuit and Saturation Modeling A key contribution of this work is the modeling of the Transimpedance Amplifier (TIA) saturation to evaluate the robustness of the neuromorphic system. In a physical crossbar array, the output current is the integration of currents from all connected synapses:

$$I_{\text{sum}} = \sum V_{\text{in}} \cdot G \quad (S4)$$

However, real-world readout circuits have a limited dynamic range. We defined a strict **Saturation Limit** (I_{sat}) based on the ideal performance of the high-ratio device:

$$I_{\text{sat}} \approx 1.1 \times \max(I_{\text{peak,ideal}}) \quad (\text{S5})$$

where $I_{\text{peak,ideal}}$ is the maximum instantaneous current observed during inference with the Ag/Sb₂Se₃/ITO device under clean input conditions.

During the robustness test (Figure 4g), Gaussian noise $N(0, \sigma^2)$ was injected into the input vectors. The resulting column currents were clamped at I_{sat} :

$$I_{\text{out}} = \min(I_{\text{sum}}, I_{\text{sat}}) \quad (\text{S6})$$

For the low-ratio baseline device (Ratio $\approx$ 10), the high G_{min} causes a massive accumulation of common-mode leakage current. This leakage consumes the majority of the circuit's dynamic headroom. Consequently, even small amounts of input noise cause the total current to exceed I_{sat} , leading to signal clipping and severe accuracy degradation. In contrast, the Ag/Sb₂Se₃/ITO device maintains a low background current, preserving the dynamic range for effective neuromorphic computing.

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Note S2. Implementation Details of the Neuromorphic Convolution Engine

S2.1 Differential Synaptic Mapping Strategy In neuromorphic hardware, implementing signed synaptic weights (e.g., standard convolution kernels) on passive memristor crossbars (where conductance $G \geq 0$) requires a differential architecture. We adopted a dual-pathway scheme where the logical weight W is encoded as the difference between two physical conductance states, G_{pos} (excitatory) and G_{neg} (inhibitory). The mapping function from the normalized logical weight $w \in [-1, 1]$ to physical synaptic conductance is defined as:

$$\begin{cases} G_{\text{pos}} = G_{\text{min}} + w \cdot (G_{\text{max}} - G_{\text{min}}), & G_{\text{neg}} = G_{\text{min}} & \text{if } w > 0 \\ G_{\text{pos}} = G_{\text{min}}, & G_{\text{neg}} = G_{\text{min}} + |w| \cdot (G_{\text{max}} - G_{\text{min}}) & \text{if } w \leq 0 \end{cases} \quad (\text{S7})$$

This approach allows the analog differential current

$$I_{\text{diff}} \propto V_{\text{read}} \cdot (G_{\text{pos}} - G_{\text{neg}}) \quad (\text{S8})$$

to linearly represent the computing result, utilizing the device's variable resistance state to perform in-memory arithmetic.

S2.2 Stochastic Device Modeling To accurately predict the performance of the neuromorphic system, the simulation explicitly models the intrinsic stochasticity of the memristive synapses. Device-to-Device (D2D) variability is introduced as multiplicative Gaussian noise injected into the programmed conductance states. The effective conductance G_{eff} for each synapse is modeled as:

$$G_{\text{eff}} = G_{\text{target}} \cdot (1 + N(0, \sigma^2)) \quad (\text{S9})$$

where σ represents the coefficient of variability. The simulation also accounts for circuit-level constraints, such as the saturation limit of the Transimpedance Amplifier (TIA), ensuring the model reflects realistic hardware operating conditions.

S2.3 Simulation Parameters Table S1 summarizes the key physical parameters used in the neuromorphic simulation engine. The “Ours” configuration utilizes the experimental metrics of the Ag/Sb₂Se₃ device, characterized by a high ON/OFF ratio (10^5) to minimize signal leakage. The “Baseline” configuration represents typical low-ratio devices, where high background conductance leads to significant common-mode current accumulation.

Table S2. Parameters for the Neuromorphic Simulation Engine

Parameter	Symbol	Value (Ours)	Value (Baseline)	Description
Read Voltage	V_{read}	0.2 V	0.2 V	Amplitude of input pulse
Max Conductance	G_{max}	100 μS	100 μS	Synaptic ON-state
Min Conductance	G_{min}	0.01 μS	10 μS	Synaptic OFF-state (Leakage source)
On/Off Ratio	r	100,000	10	Synaptic Dynamic Range
Variability	σ	3% (0.03)	35% (0.35)	D2D Variation
TIA Limit	I_{sat}	200 μA	200 μA	Current saturation threshold

S2.4 Spatiotemporal Processing Workflow The simulation was implemented using a PyTorch-based tensor engine to emulate the parallel nature of crossbar arrays. The input sensory frames were pre-processed and mapped to the analog voltage domain $[0, V_{\text{read}}]$. The convolution operations were executed via kernel-based current summation to simulate the KCL mechanism. For dynamic motion analysis (Figure 5f-h), two sequential time-steps, t_0 and t_1 (simulating a forward motion vector), were processed. The motion features were extracted by computing the analog difference of the output feature maps:

$$M=|\text{Map}_{t1}-\text{Map}_{t0}|$$

(S10)

, demonstrating the system's capability for temporal change detection.

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Table S3. Hall measurement results of the optimized Sb₂Se₃ film.

Temperature (K)	Carrier Concentration (cm ⁻³)	Resistivity (Ω·cm)	Hall Mobility (cm ² /V·s)
308	1.46×10^{14}	1.56×10^6	2.74×10^{-2}

Table S4. Comparison of edge extraction performance under different readout modes (Input noise $\sigma = 0.10$).

Device Configuration	Readout Mode	SSIM	Saturation Fraction
High ON/OFF (Ours)	Fixed-gain TIA	0.267	0.00%
Low ON/OFF baseline	Fixed-gain TIA	0.058	6.95%
Low ON/OFF baseline	Dynamic gain	0.092	0.00%

Table S5. Estimation of RC settling time limits based on the ultra-high resistance state.

Device HRS	Parasitic Column Capacitance	Time Constant (τ)	5τ Settling Time
7 GΩ	1 fF	7 μs	35 μs
7 GΩ	10 fF	70 μs	350 μs
7 GΩ	50 fF	350 μs	1.75 ms
7 GΩ	100 fF	700 μs	3.5 ms

Table S6. Quantitative evaluation of edge extraction and motion heatmaps (Input noise $\sigma = 0.05$, evaluated across 5 random seeds).

Processing Task	Device Configuration	SSIM	mIoU
Edge Extraction	High ON/OFF (Ours)	0.573 ± 0.017	0.579 ± 0.008
Edge Extraction	Low ON/OFF baseline	0.079 ± 0.089	0.413 ± 0.045
Motion Heatmap	High ON/OFF (Ours)	0.678 ± 0.020	0.562 ± 0.004
Motion Heatmap	Low ON/OFF baseline	0.106 ± 0.093	0.396 ± 0.046