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High driving current and enhanced gate control in 1-nm gate length type-II ZnO/GaN vdWH field-effect transistor via a constituent-layer-selective doping strategy

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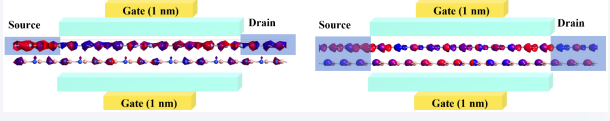
ABSTRACT: Two-dimensional (2D) semiconductors provide promising channels for sub-3 nm field-effect transistors (metal-oxide-semiconductor field-effect transistors (MOSFETs)) due to their atomic thickness and strong electrostatic control. At this scale, conventional 2D MOSFETs face a trade-off between driving current and gate control: High source/drain (S/D) doping increases current but weakens gate modulation, whereas low doping improves electrostatics but reduces current. Here, we propose a layer-selective doping (LSD) strategy for the S/D electrodes of type-II ZnO/GaN MOSFETs, which exhibit an intrinsic staggered band alignment that spatially separates electrons and holes. In LSD-ZnO/GaN MOSFETs, only the constituent ZnO layer in the S/D electrodes is n-type doped, while the GaN layer remains intrinsic, spatially separating electrons and holes. Fully doped S/D electrodes of ZnO/GaN MOSFETs (FD-ZnO/GaN MOSFETs), where both ZnO and GaN layers are n-type doped, serve as a reference. Quantum transport simulations show that both FD- and LSD-ZnO/GaN MOSFETs achieve sufficient driving current at sub-3 nm gate lengths. Notably, LSD-ZnO/GaN MOSFETs reach high on-currents of 1493 μA/μm (high-performance) and 392 μA/μm (low-power) with a minimal subthreshold swing of 78 mV/dec at an optimal 1 nm gate length, outperforming previously reported 2D MOSFETs. These improvements of LSD-ZnO/GaN MOSFETs arise from current confinement, which reduces channel capacitance, suppresses leakage current, and mitigates drain-induced barrier lowering, thereby enhancing gate control. The proposed LSD strategy is compatible with the existing layer-by-layer doping technique. It offers a transferable design concept for constituent-layer-selective carrier modulation in other type-II van der Waals heterostructures in sub-3 nm (including 1 nm) logic devices.



KEYWORDS: ZnO/GaN, van der Waals heterostructure, field-effect transistor, constituent-layer-selective doping, full doping, first-principles quantum simulation

1 Introduction

The continuous downscaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) has been the foundation of modern integrated circuits, yet conventional silicon MOSFETs suffer from severe short-channel effects (SCEs) as the gate length approaches the sub-10 nm regime [1–4]. Two-dimensional (2D) semiconductors, with their atomic-scale thickness and absence of surface dangling bonds, have emerged as promising channel materials for suppressing SCEs and enhancing gate control [5–10]. Experimentally and theoretically, various 2D MOSFETs have demonstrated reliable gate control and reasonable driving current at sub-10 nm scale gate lengths [11–17], including MoS_2 [12, 13, 18], GaSe [15], black phosphorus [19], $MoSi_2N_4$ [16, 20], InSe/In_2SSe MOSFETs [21], and $WSe_2/SnSe_2$ TFET [22]. However, achieving both strong gate control and high driving current in sub-3 nm MOSFETs remains a critical challenge [20, 22, 23], motivating the search for alternative device strategies.

A critical yet often overlooked factor contributing to this limitation is the source/drain (S/D) doping strategy in 2D MOSFETs. Higher doping enhances carrier injection and driving current but weakens gate control [24], whereas lower doping improves gate control at the cost of reduced current [25]. This

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apparent trade-off is fundamentally governed by the spatial distribution of free carriers near the source/channel junction. By confining carrier flow to targeted channel regions, the current confinement effect enhances gate control, suppresses parasitic carriers, and improves device performance [26, 27]. Hence, we propose a layer-selective doping (LSD) strategy (Fig. 1(a)), in which high-concentration doping is confined to the specific functional layer of the S/D electrodes, maximizing channel injection while minimizing unwanted carrier accumulation. Spatially selective doping in 2D atomic-scale vdWH devices remains experimentally challenging because it requires precise dopant control and suppression of interlayer cross-diffusion. While recent advances, including atomic layer doping and remote plasma treatment, have demonstrated the potential for constituent-layer-selective doping in atomically thin semiconductors [28–35], a systematic platform for validating and optimizing such strategies is still lacking. Therefore, identifying an appropriate physical platform for implementing and evaluating the proposed LSD strategy is essential.

Type-II van der Waals heterostructures (vdWHs) provide a natural platform for implementing LSD, as their staggered band alignment spatially separates electrons and holes into different constituent layers [36, 37]. This unique feature enables layer-selective n-/p-type doping in the S/D regions, thereby realizing a current confinement effect. Among various type-II 2D vdWHs, the ZnO/GaN vdWH is particularly attractive for sub-3 nm MOSFETs. Monolayer ZnO (ML-ZnO) and ML-GaN have been synthesized [38–40] and possess atomic-scale thickness, which is highly desirable for strong gate control [7, 41, 42]. ZnO/GaN exhibits a type-II band alignment, with the conduction-band minimum located in the ZnO layer [43], naturally enabling the selective n-type doping in the constituent ZnO layer while maintaining the GaN layer intrinsic. Moreover, its wide bandgap (~ 2.78 eV) effectively suppresses off-state leakage current [43], which is critical at ultra-short gate lengths [44]. Although ZnO/GaN has been extensively investigated in optoelectronic applications [43, 45], its potential as channel material for sub-3 nm MOSFETs remains largely unexplored.

In this work, we systematically investigate sub-3 nm ZnO/GaN MOSFETs employing LSD strategy for the S/D electrodes through first-principles quantum transport simulations, with fully doped (FD) S/D electrodes as a reference (Fig. 1(b)). Theoretical results demonstrate that both FD- and LSD-ZnO/GaN MOSFETs at sub-3 nm gate length can meet the International Technology Roadmap for Semiconductors (ITRS) requirements for high-performance (HP) and low-power (LP) electronics. Compared with FD counterparts, sub-3 nm LSD-ZnO/GaN MOSFETs display much better gate control and smaller tunneling leakage current. Notably, our simulations show that the gate length of ZnO/GaN MOSFETs can be scaled down to 1 nm, and the LSD approach plays a critical role in reinforcing gate control at this scale. Beyond ZnO/GaN MOSFETs, the LSD concept provides a general design principle for other 2D type-II vdWHs, such as MoS_2/WSe_2 and $MoS_2/MoSSe$ [46–49]. In these systems, the difference in intrinsic electronic properties between the constituent layers, often reflected in their different work functions, enables carrier modulation to be naturally defined at the constituent-layer level, offering a versatile framework for sub-3 nm (including 1 nm) logic devices.

2 Computational methods

The structural and electronic characteristics of the lowest-energy ZnO/GaN were calculated within VASP [50, 51]. After that, the double-gate FD- and LSD-ZnO/GaN MOSFETs are established (Figs. 1(a) and 1(b)). For FD MOSFETs, the ZnO and GaN layers in S/D electrodes were both n-type doped. For LSD MOSFETs, only the ZnO layer in S/D electrodes was n-type doped. The doping concentration was set to 5×10^{13} e/cm^2 (2×10^{20} e/cm^3) [52]. A source-drain bias V_{SD} of 0.64 V was applied in accordance with ITRS guidelines [53], following several recent works [17, 22, 23]. The undoped ZnO/GaN lied in the y–z plane and functions as the channel, where free-carrier transport occured along the z direction. Underlap (UL) regions of varying lengths were incorporated between the S/D electrodes and the gated channel area [54]. HfO_2 was adopted as the gate insulator, featuring an oxide thickness of 0.41 nm and a relative permittivity of 25. Both top and bottom gates consisted of 0.2 nm-thick metal layers. The transfer characteristics were simulated using the Non-Equilibrium Green's Function (NEGF) within Atomistix ToolKit (ATK) [55], and additional methodological details are provided in the Electronic Supplementary Material (ESM).

The driving current, represented by the on-current I_{ON}, is a critical factor affecting the performance of 2D MOSFETs in both HP and LP electronics [56]. The I_{ON} is defined as the drain current at $V_G(\text{on}) = V_G(\text{off}) + V_{SD}$, where V_{SD} is the S/D voltage (0.64 V), and $V_G(\text{off})$ is the off-state gate voltage. The gate control in the subthreshold region is quantified by the subthreshold swing (SS) using $SS = \partial V_G / \partial(\log I_d)$. Lower SS values indicate stronger gate control. The transconductance g_m values are obtained in the super-threshold region using $g_m = dI_D/dV_G$. The delay time (τ) quantifies 2D MOSFETs' switching speed and is expressed as $\tau = C_t \times V_{SD}/I_{ON}$, where C_t denotes the total capacitance. C_t includes contributions from the channel component C_{ch} and the fringing component C_f, where C_f is assumed to be twice C_{ch} [57]. C_{ch} is given by $C_{ch} = dQ_{ch}/(W \times dV_G)$, where Q_{ch} denotes the accumulated charge within the channel region, and W is the channel width (3.24 Å). The power delay product (PDP)

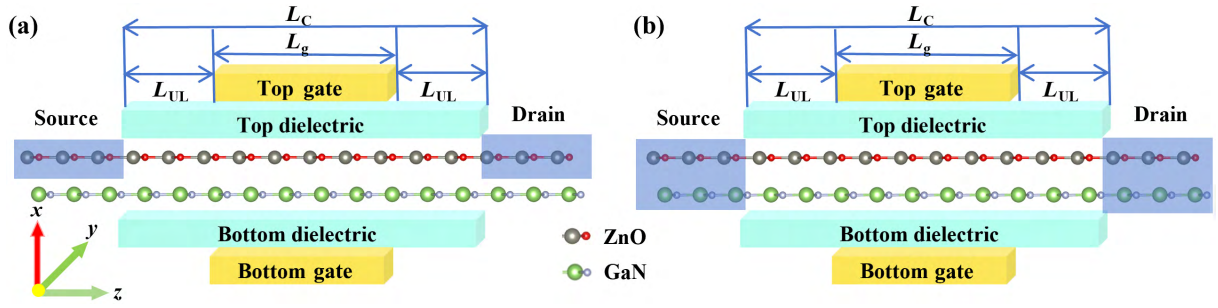

Figure 1 Schematic illustrations of the different doping configurations in (a) LSD- and (b) FD-ZnO/GaN MOSFETs.

reflects the consumed energy during a single switching and is given by PDP = $V_{SD} \times I_{ON} \times \tau = C_t \times V_{SD}^2$. The drain-induced barrier lowering (DIBL) is calculated as DIBL = $(V_{th}^{low} - V_{th}^{high})/(V_{SD}^{low} - V_{SD}^{high})$, where V_{th}^{low} and V_{th}^{high} are the threshold voltages extracted at low and high drain biases, respectively. Lower DIBL values indicated reduced drain-induced barrier modulation and thus improved electrostatic integrity. The reliability of present simulations is validated in Fig. S1 and Table S1 in the ESM.

3 Theoretical results

3.1 Electronic properties of ZnO/GaN

The optimized ZnO/GaN exhibits an in-plane lattice constant of 3.24 Å and an interlayer distance of 2.93 Å (Fig. S2 in the ESM). It has an indirect wide band gap of 2.84 eV and a typical type-II band alignment (Fig. 2(a)), consistent with previous reports [43]. The conduction band minimum (CBM) is primarily delocalized within the ZnO layer (Fig. 2(b)), forming continuous electron transport pathways that favor high-performance n-type MOSFETs. In contrast, the valence band maximum (VBM) is predominantly localized in the GaN layer, originating mainly from N atomic orbitals (Fig. 2(c)), which limits the hole transport in p-type ZnO/GaN electronic devices. On the other hand, the theoretical effective masses of electrons and holes along the *x*-direction (*y*-direction) are 0.22 and 1.95 m_e, respectively. The lighter electron effective mass further suggests the high performance of n-type ZnO/GaN electronic devices. These characteristics provide the rationale for focusing on n-type ZnO/GaN MOSFETs in this study.

3.2 Fully doped source/drain electrodes

As a reference, the performance of FD-ZnO/GaN MOSFETs is first examined, and the key device parameters are extracted from the transfer characteristics (Fig. S3 in the ESM). For the HP application (Fig. 3(a) and Table S2 in the ESM), the I_{ON} at $L_g = 3$ nm exhibits a nonmonotonic dependence on the underlap length, first increasing from 1684 μA/μm ($L_{UL} = 0$ nm) to 4920 μA/μm ($L_{UL} = 2$ nm), and then decreasing to 1970 μA/μm ($L_{UL} = 4$ nm), which is well above the ITRS HP requirement of 900 μA/μm. A similar trend is observed for $L_g = 2$ nm, where the I_{ON} values also meet the ITRS requirement for ($L_{UL} = 1$–4 nm). Notably, even at the ultimate gate length of 1 nm, the device still maintains a high I_{ON} exceeding 1720 μA/μm for $L_{UL} = 2$–4 nm. For LP application (Fig. 3(b) and Table S3 in the ESM), the I_{ON} ranges from 1453 to 874 μA/μm at $L_g = 3$ nm ($L_{UL} = 2$–4 nm), significantly exceeding the ITRS LP target of 295 μA/μm. For $L_g = 2$ nm ($L_{UL} = 3$–4 nm), I_{ON} also remains above the LP requirement. Meanwhile, when L_g=1 nm ($L_{UL} = 4$ nm), which still meets the ITRS requirement, the device achieves an I_{ON} of 447 μA/μm.

After confirming that FD-ZnO/GaN MOSFETs achieve adequate I_{ON} for HP and LP applications, their τ, PDP (Fig. S4 in the ESM), g_m, and SS are further evaluated. Specifically, τ ranges from 0.054 to 0.153 ps (HP) and 0.171 to 0.399 ps (LP), well below the ITRS limits of 0.423 ps (HP) and 1.493 ps (LP), respectively. Meanwhile, the PDP values remain lower than the ITRS threshold of 0.24 fJ/μm (HP) and 0.28 fJ/μm (LP), indicating energy-efficient operation. The g_m values of FD-ZnO/GaN MOSFETs range from 16.36 to 5.28 mS/μm (Table S2 in the ESM), which significantly exceed those of ML-Ga_2O_3 [52] and are comparable to those of ML-GaN (AlN) [58]. The SS ranges from 170 to 70 mV/dec at L_g=3 nm ($L_{UL} = 0$–4 nm), from 138 to 84 mV/dec at $L_g = 2$ nm ($L_{UL} = 2$–4 nm), and from 155 to 92 mV/dec at $L_g = 1$ nm ($L_{UL} = 2$–4 nm) (Table S2 in the ESM).

In summary, FD-ZnO/GaN MOSFETs exhibit satisfactory I_{ON}, τ, and PDP values for HP and LP applications across the sub-3 nm gate length. HP targets are met at $L_g = 3$ nm ($L_{UL} = 0$–4 nm), 2 nm ($L_{UL} = 1$–4 nm), and 1 nm ($L_{UL} = 2$–4 nm), while LP targets are satisfied at $L_g = 3$ nm ($L_{UL} = 2$–4 nm), 2 nm ($L_{UL} = 3$–4 nm), and 1 nm ($L_{UL} = 4$ nm). However, the relatively large SS value at 2 and 1 nm, such as 92 mV/dec at $L_g = 1$ nm ($L_{UL} = 4$ nm), suggests that the gate control still requires further improvement.

3.3 Layer-selective doping of source/drain electrodes

The key device parameters of LSD-ZnO/GaN MOSFETs are extracted from the transfer characteristics (Fig. S5 in the ESM). Compared with FD-ZnO/GaN MOSFETs, LSD-ZnO/GaN MOSFETs exhibit a slight reduction in I_{ON}, primarily due to the narrower doped source region, which limits electron injection. For HP applications (Fig. 4(a) and Table S4 in the ESM), the I_{ON} at

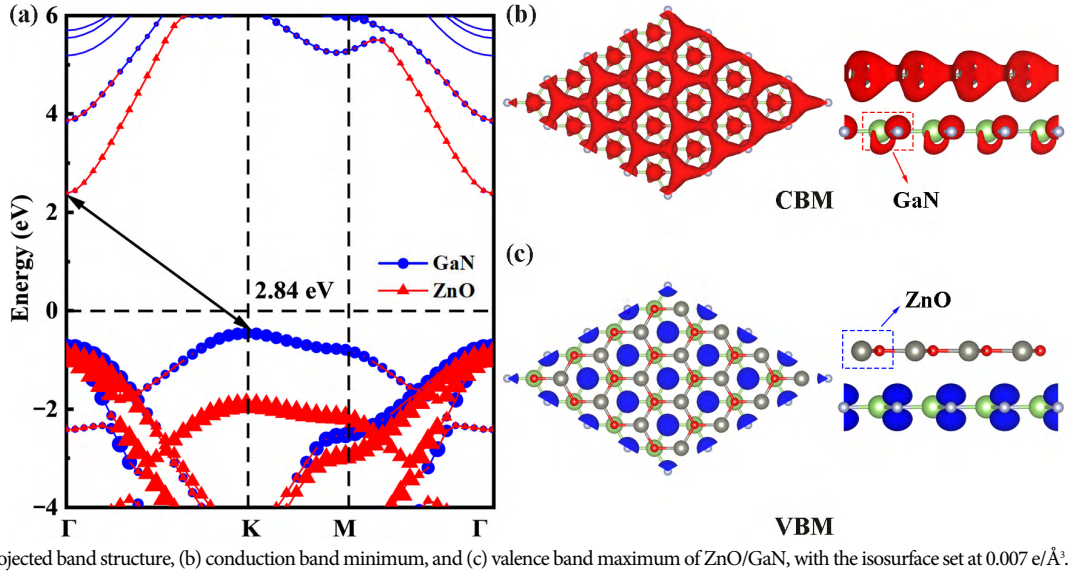

Figure 2 (a) Projected band structure, (b) conduction band minimum, and (c) valence band maximum of ZnO/GaN, with the isosurface set at 0.007 e/Å^3.

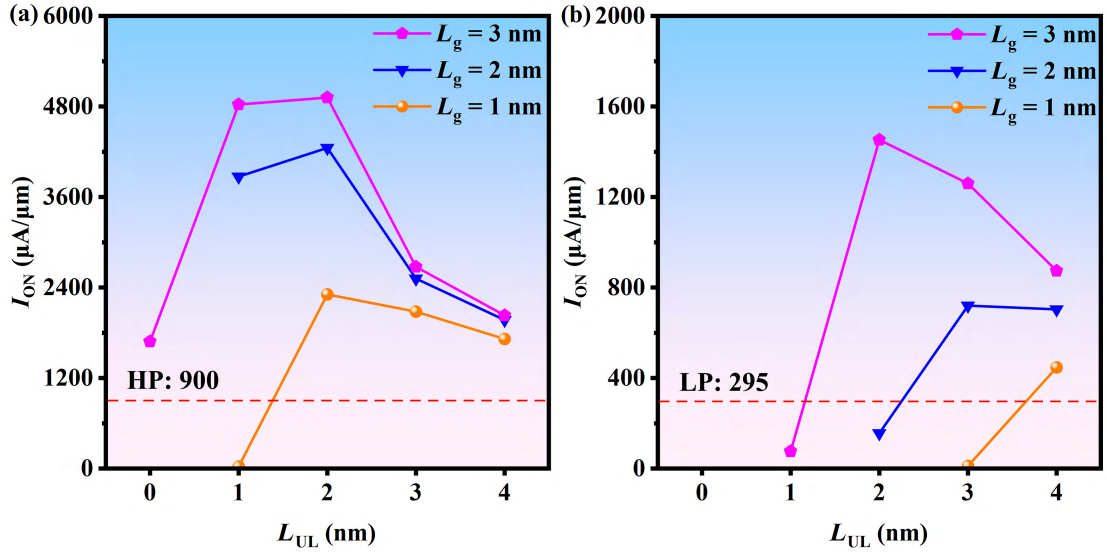

Figure 3 Calculated I_{ON} for (a) high-performance and (b) low-power applications of FD-ZnO/GaN MOSFETs.

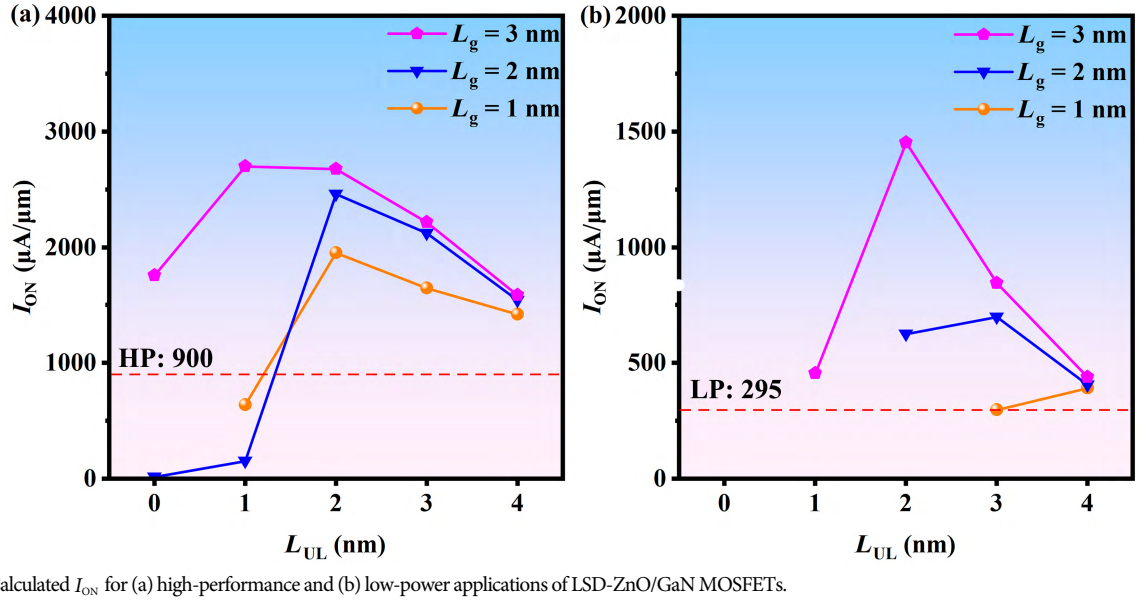

Figure 4 Calculated I_{ON} for (a) high-performance and (b) low-power applications of LSD-ZnO/GaN MOSFETs.

L_g = 3 nm (L_{UL} = 0–4 nm) ranges from 1587 to 2700 μA/μm, which significantly exceeds the ITRS HP requirement of 900 μA/μm. As L_g scales down to 2 nm, the I_{ON} still meets the ITRS requirement for L_{UL} = 2–4 nm. Even at the ultimate gate length of 1 nm, the I_{ON} remains as high as 1952–1423 μA/μm for L_{UL} = 2–4 nm. For LP applications (Fig. 4(b) and Table S5 in the ESM), the I_{ON} ranges from 440 to 1453 μA/μm at L_g = 3 nm (L_{UL} = 1–4 nm), with the ITRS target (295 μA/μm) achieved. For L_g = 2 nm (L_{UL} = 2–4 nm) and 1 nm (L_{UL} = 3–4 nm), the I_{ON} remains above the LP requirement. Moreover, LSD-ZnO/GaN MOSFETs exhibit generally lower τ and PDP values than FD counterparts (Tables S2 and S4 in the ESM). Specifically, the τ ranges from 0.066 to 0.126 ps for HP applications and 0.12 to 0.48 ps for LP applications, while the PDP ranges from 0.09 to 0.144 fJ/μm, all satisfying the ITRS requirement (Fig. S6 in the ESM).

The LSD strategy also influences the g_m of ZnO/GaN MOSFETs (Table S4 in the ESM). The g_m values range from 9.23 to 3.07 mS/μm, showing a significant decrease compared with FD-ZnO/GaN MOSFETs. Nevertheless, these values remain comparable to those of yet-reported ML-$PtSe_2$, ML-ZrS_2, and ML-BAs MOSFETs [59–61]. The reduced g_m is consistent with the slightly degraded I_{ON}, which is mainly due to the limited carrier injection into the channel. Significantly, LSD-ZnO/GaN MOSFETs exhibit improved SS compared with their FD counterparts, and this improvement becomes more pronounced as L_g shortens, indicating the enhanced gate control. Specifically, the SS ranges from 157 to 64 mV/dec at L_g = 3 nm (L_{UL} = 0–4 nm), from 96 to 69 mV/dec at L_g = 2 nm (L_{UL} = 2–4 nm), and from 120 to 78 mV/dec at L_g = 1 nm (L_{UL} = 2–4 nm). To further optimize device performance, biaxial strain is examined for the representative L_g = 1 nm (L_{UL} = 4 nm) device. The results indicate that the unstrained configuration remains optimal in terms of the overall balance between driving current and gate control.

In summary, LSD-ZnO/GaN MOSFETs exhibit satisfactory I_{ON}, τ, and PDP values for HP and LP applications across sub-3 nm gate length. HP targets are met at L_g = 3 nm (L_{UL} = 0–4 nm), 2 nm (L_{UL} = 2–4 nm), and 1 nm (L_{UL} = 2–4 nm), while LP targets

are satisfied at $L_g = 3$ nm (L_{UL} = 1–4 nm), 2 nm (L_{UL} = 2–4 nm), and 1 nm (L_{UL} = 3–4 nm). The significantly reduced SS values at 2 and 1 nm, such as 78 mV/dec at $L_g = 1$ nm ($L_{UL} = 4$ nm), explicitly confirm the effectiveness of the LSD strategy in enhancing gate control.

3.4 Performance comparison with previously reported MOSFETs

To benchmark the performance of FD- and LSD-ZnO/GaN MOSFETs, a comparison with previously reported 2D FETs is presented [15–20, 23, 62–67]. At L_g = 3 nm, for HP applications (Fig. 5(a)), FD-ZnO/GaN MOSFETs exhibit the highest I_{ON}, while LSD-ZnO/GaN MOSFETs also display a large I_{ON} just below that of ML-AlN MOSFET. For LP applications (Fig. 5(b)), FD- and LSD-ZnO/GaN MOSFETs deliver I_{ON} values apparently surpassing those of all reported 2D MOSFETs within our knowledge. At L_g = 2 nm, only a few reported 2D MOSFETs meet the ITRS I_{ON} requirements due to aggravated short-channel effects. In contrast, FD- and LSD-ZnO/GaN MOSFETs consistently retain superior I_{ON} for both HP and LP applications.

At the extreme gate length of 1 nm, among the reported MOSFETs, only the ML-AlN and $MoSiGeN_4$ (cold-source) MOSFETs meet the HP requirement, while their I_{ON} remains lower than that of FD- and LSD-ZnO/GaN MOSFETs. For LP applications, only the $MoSiGeN_4$ (cold-source) MOSFETs fulfill the ITRS requirement, with their I_{ON} exceeding that of FD- and LSD-ZnO/GaN MOSFETs. In terms of SS (Fig. 5(c)), the LSD-ZnO/GaN MOSFET exhibits highly competitive SS among the reported 2D MOSFETs. At L_g = 3 nm, only the $MoSiGeN_4$ (cold-source) MOSFETs show a lower value (64 mV/dec), whereas all other devices have larger values. At L_g = 2 nm, the CuI MOSFETs show a lower SS (62 mV/dec), while the remaining devices still perform worse. Notably, at L_g = 1 nm, the LSD-ZnO/GaN MOSFET exhibits a clear and significant advantage, highlighting its excellent gate controllability. Overall, these comparisons demonstrate the pronounced advantage of FD- and especially LSD-ZnO/GaN MOSFETs over reported MOSFETs at the sub-3 nm scale, particularly at the rarely reported 2 and 1 nm gate lengths.

4 Extended discussion

4.1 Impact of LSD on the on-state current

As discussed above, the on-state current I_{ON} of FD-ZnO/GaN MOSFETs is higher than that of LSD-ZnO/GaN MOSFETs. To elucidate the underlying conduction mechanism, the transmission eigenstates are analyzed. For both FD- and LSD-ZnO/GaN MOSFETs, the transmission eigenstates exhibit a dominant and continuous distribution along the ZnO layer (Figs. 6(a) and 6(b)), demonstrating that charge transport is primarily confined to the ZnO layer. This behavior is consistent with the CBM being located in the ZnO layer and the n-type doping of the S/D electrodes.

In FD-ZnO/GaN MOSFETs, additional localized transmission eigenstates emerge in the GaN layer due to carrier injection. In contrast, the transmission eigenstates in the GaN layer are almost negligible in LSD-ZnO/GaN MOSFETs owing to the absence of carrier injection. Consequently, FD-ZnO/GaN MOSFETs exhibit a larger on-state current I_{ON} than their LSD counterparts. Moreover, the LSD strategy effectively suppresses undesired conduction paths and enforces a more directional current flow within the ZnO layer, leading to improved current confinement in 2D vdWH MOSFETs. This directional carrier transport may enhance the gate control over the channel.

4.2 Impact of LSD on the subthreshold swing

The enhanced gate control is reflected in the subthreshold swing $SS = \ln(10) \cdot \frac{kT}{q} \cdot \left(1 + \frac{C_{ch}}{C_{ox}}\right)$ [68]. A reduction in C_{ch} directly results in a lower SS and thus stronger gate control. In FD-ZnO/GaN MOSFETs, the gate-induced charge is mainly stored in the ZnO layer and partly in the GaN layer. In LSD-ZnO/GaN MOSFETs, the gate-induced charge is only stored in the ZnO layer and remains negligible in the GaN layer. From this standpoint, the gate-induced charge C_{ch} of LSD-ZnO/GaN MOSFETs could be reduced compared to that of FD-counterparts, so LSD-ZnO/GaN MOSFETs may acquire a lower SS.

To quantitatively substantiate the improved gate control enabled by the LSD strategy, we further numerically compare the C_{ch} of FD-

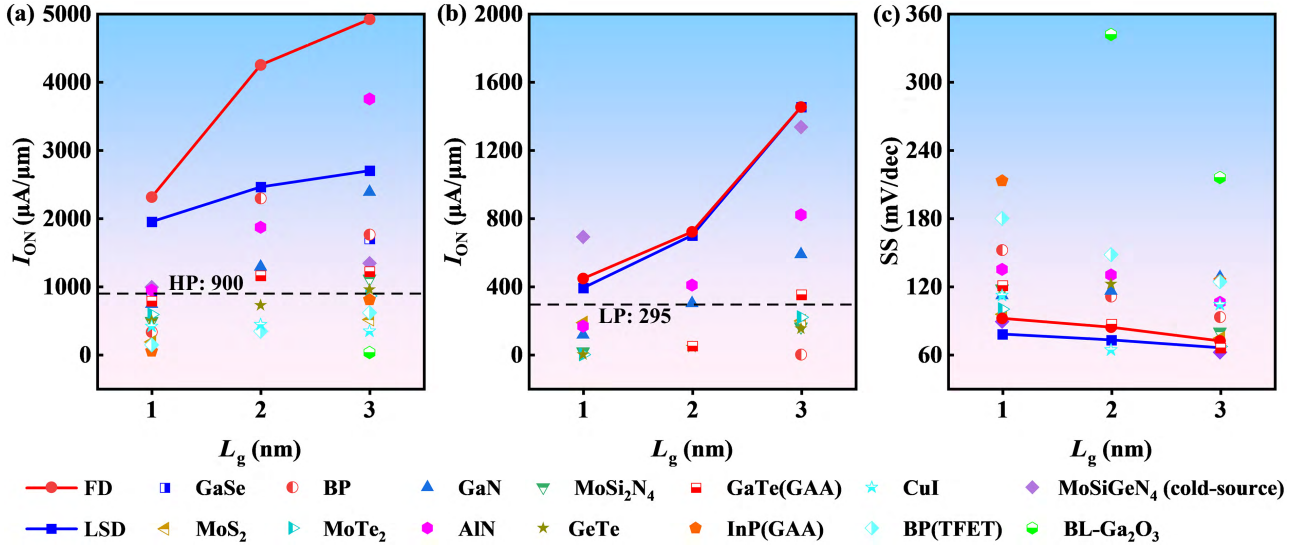

Figure 5 Comparison of FD-(LSD-)ZnO/GaN MOSFETs with previously reported 2D n-MOSFETs: (a) I_{ON} for HP applications, (b) I_{ON} for LP applications, and (c) SS values.

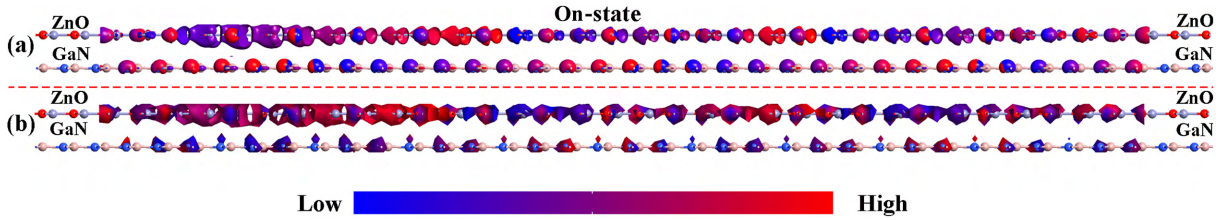

Figure 6 On-state transmission eigenstates of (a) FD- and (b) LSD-ZnO/GaN MOSFETs ($L_g = 1$ nm, $L_{UL} = 3$ nm) at $V_g = 0.3$ V, with the isosurface value set at 0.18 e/Å^3.

and LSD-ZnO/GaN MOSFETs at different gate lengths. For all L_g, C_{ch} of LSD-ZnO/GaN MOSFETs is smaller than that of FD-ZnO/GaN MOSFETs. For instance, at $L_g = 3$ nm (L_{UL}=0–4 nm), the C_{ch} of FD-ZnO/GaN MOSFETs ranges from 0.135 to 0.104 fF/μm (Tables S2 and S3 in the ESM), whereas it ranges from 0.116 to 0.079 fF/μm in LSD-ZnO/GaN MOSFETs (Tables S4 and S5 in the ESM). For $L_g = 2$ nm (L_{UL}=0–4 nm), the C_{ch} of FD- and LSD-ZnO/GaN MOSFETs ranges from 0.124 to 0.100 fF/μm and 0.085 to 0.075 fF/μm. For $L_g = 1$ nm (L_{UL}=1–4 nm), the C_{ch} of FD- and LSD-ZnO/GaN MOSFETs ranges from 0.116 to 0.093 and 0.080 to 0.072 fF/μm. Consequently, for all L_g, the SS of LSD-ZnO/GaN MOSFETs remains lower than that of FD-ZnO/GaN MOSFETs (Figs. 7(a)–7(c)). These results confirm that the LSD approach suppresses the C_{ch} and consequently enhances gate control.

4.3 Impact of LSD on the off-state leakage current

Because electron injection occurs in both the ZnO and GaN layers in FD-ZnO/GaN MOSFETs, whereas it is confined to the ZnO layer in LSD devices, FD-ZnO/GaN MOSFETs exhibit a higher channel tunneling probability and electron concentration. According to the self-consistent solution of Poisson's equation

$$\nabla^2\psi = -\rho/\varepsilon \quad (1)$$

where ε denotes the permittivity of the channel material. As the electron concentration increases, enhanced charge density (ρ) elevates the electrostatic potential ψ. The conduction band edge is related to the electrostatic potential by $E_C = E_{C0} - e\psi$, where E_{C0} represents the intrinsic conduction band minimum. Therefore, the elevated ψ induces a downward shift of E_C, effectively reducing the source-channel potential barrier Φ_B. A one-dimensional parametric study of electron density, detailed in Fig. S9 in the ESM, illustrates these trends and provides representative values of ρ, ψ, and E_C, consistent with our above analysis.

The impact of the reduced barrier on tunneling current (I_{tunnel}) can be further understood by the direct source–drain tunneling model [69]

$$I_{tunnel} \propto \exp(-L_{ch}\sqrt{m^*\Phi_B}) \quad (2)$$

where L_{ch} is the channel length and m^* is the effective mass. According to this equation, a reduction of Φ_B results in an increase in off-state I_{tunnel}. To further verify the proposed mechanism, the transmission spectra, local density of state (LDOS), and current spectra for FD- and LSD-ZnO/GaN MOSFETs with $L_g = 1$ nm ($L_{UL} = 3$ nm) are calculated (Figs. 8(a)–8(f)). FD-ZnO/GaN MOSFET exhibits a much higher charge density in the source/drain and channel region compared with their LSD counterparts (Figs. 8(b) and 8(e)), indicating pronounced carrier accumulation induced by full S/D doping, which is also consistent with the larger channel charge accumulation discussed above. Moreover, in the off-state of FD-ZnO/GaN MOSFETs, the lower channel potential barrier ($\Phi_B = 0.52$ eV) allows a relatively large tunneling current ($I_{tunnel} = 8.89 \times 10^{-15}$ A). In contrast, in LSD-ZnO/GaN MOSFETs, the suppression of carrier accumulation in the GaN layer leads to a significantly increased potential barrier of $\Phi_B = 0.82$ eV. Consequently, the I_{tunnel} is reduced nearly two orders of magnitude to 2.81×10^{-17} A. Further evidence is provided by the drain-induced barrier lowering (DIBL), which decreases from 102 mV/V in *FD*-ZnO/GaN MOSFETs with $L_g = 1$ nm ($L_{UL} = 3$ nm) to 66 mV/V in LSD devices, reflecting improved electrostatic integrity and stronger gate control. These results provide direct spectroscopic and quantitative evidence that the LSD strategy effectively mitigates the short-channel effect.

5 Conclusion

In summary, quantum transport simulations demonstrate that both FD- and LSD-ZnO/GaN MOSFETs satisfy the ITRS requirements for HP and LP applications in the sub-3 nm regime. Compared with their FD-counterparts, sub-3 nm LSD-ZnO/GaN MOSFETs benefit from current confinement, which reduces channel capacitance, effectively raises the barrier to suppress leakage current, and mitigates drain-induced barrier lowering, thereby enhancing gate control. Notably, the LSD-ZnO/GaN MOSFETs achieve a high on-current of 1493 μA/μm (HP) and 392 μA/μm (LP) with a minimal subthreshold swing of 78 mV/dec at an optimal 1 nm gate length, demonstrating superior overall performance compared with previously reported 2D MOSFETs. Overall, the proposed LSD strategy is experimentally feasible in 2D materials and provides a transferable design concept for other type-II van der Waals heterostructures in sub-3 nm (including 1 nm) logic devices, where intrinsic electronic properties differences between constituent layers, often reflected in their different work functions, naturally enable carrier modulation at the constituent-layer level.

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Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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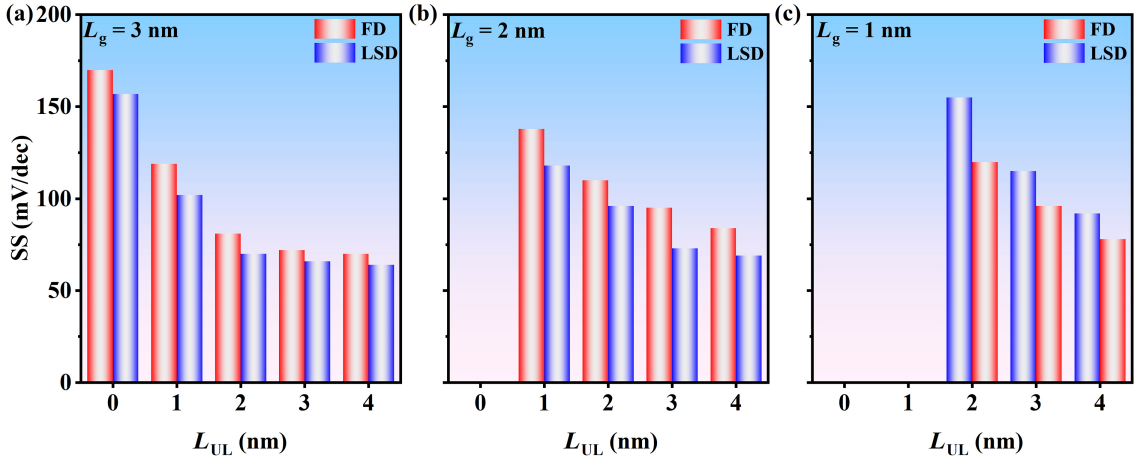

Figure 7 Calculated SS values of FD- and LSD-ZnO/GaN MOSFETs: (a) L_g = 3 nm, (b) L_g = 2 nm, and (c) L_g = 1 nm.

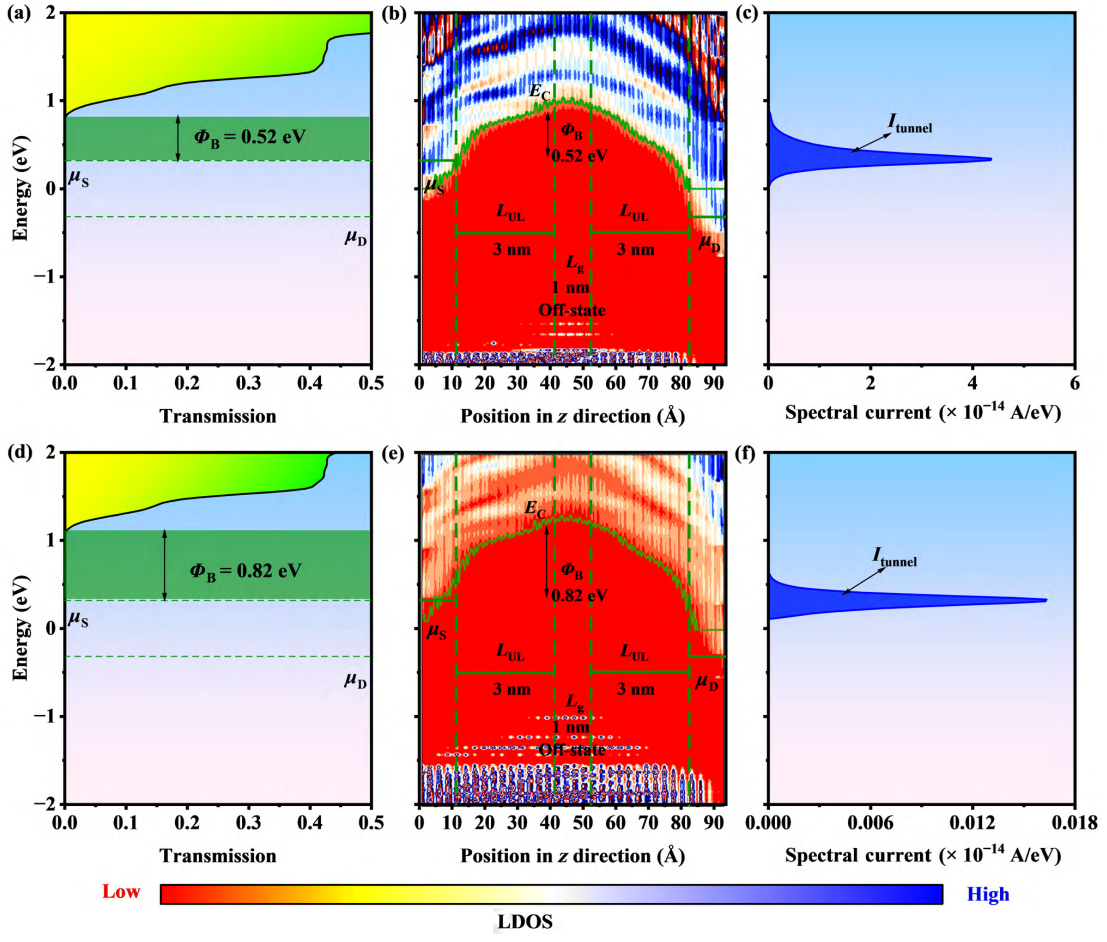

Figure 8 Comparison of (a) transmission spectra, (b) LDOS, and (c) spectral current for FD-ZnO/GaN MOSFETs (L_g = 1 nm, L_{UL} = 3 nm) at V_G = −0.9 V, and (d)–(f) for LSD-ZnO/GaN MOSFETs (L_g = 1 nm, L_{UL} = 3 nm) at V_G = −0.9 V

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Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Author contribution statement

Y. X.: Conceptualization, simulation, data analysis, writing – original draft. L.-J. W.: Conceptualization, data analysis. Q. X.: Data curation, validation. H.-L. M.: Data analysis. Z.-Q. F.: Software, resources. C.-M. Y.: Software, resources. L. H.: Conceptualization,

data analysis, methodology, supervision, funding acquisition, writing – review & editing.

Use of AI statement

None.

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