Nano Research

ISSN 1998-0124 CN 11-5974/O4
https://doi.org/10.26599/NR.2026.94908826

Research Article

Watt-level transistors based on molybdenum disulphide

Chengyuan Li[1,2,3,§], Chen Yan[4,§], Guanran Wang[5,§], Yu Bai[3,§], Hanwen Wang[3], Xuanzhe Sha[6,7], Meng Zhang[6,7], Naijie Ren[6,7], Hong Wang[4](✉), Dongming Sun[1](✉), Yu Duan[5](✉), Zheng Vitto Han[3,6,7](✉), Yaning Wang[3](✉)

[1] Shenyang National Laboratory for Materials Science, Institute of Metal Research, Chinese Academy of Sciences, Shenyang 110016, China

[2] School of Material Science and Engineering, University of Science and Technology of China, Hefei 230026, China

[3] Liaoning Academy of Materials, Shenyang 110167, China

[4] State Key Laboratory of Wide Band Gap Semiconductor Devices and Integrated Technology, School of Microelectronics, Xidian University, Xi'an 710126, China

[5] State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun 130012, China

[6] State Key Laboratory of Quantum Optics and Quantum Optics Devices, Institute of Optoelectronics, Shanxi University, Taiyuan 030006, China

[7] Collaborative Innovation Center of Extreme Optics, Shanxi University, Taiyuan 030006, China

[§] Chengyuan Li, Chen Yan, and Guanran Wang and Yu Bai contributed equally to this work.

Nano Res., **Just Accepted Manuscript** • https://doi.org/10.26599/NR.2026.94908826

https://www.sciopen.com/journal/1998-0124 on May. 9, 2026

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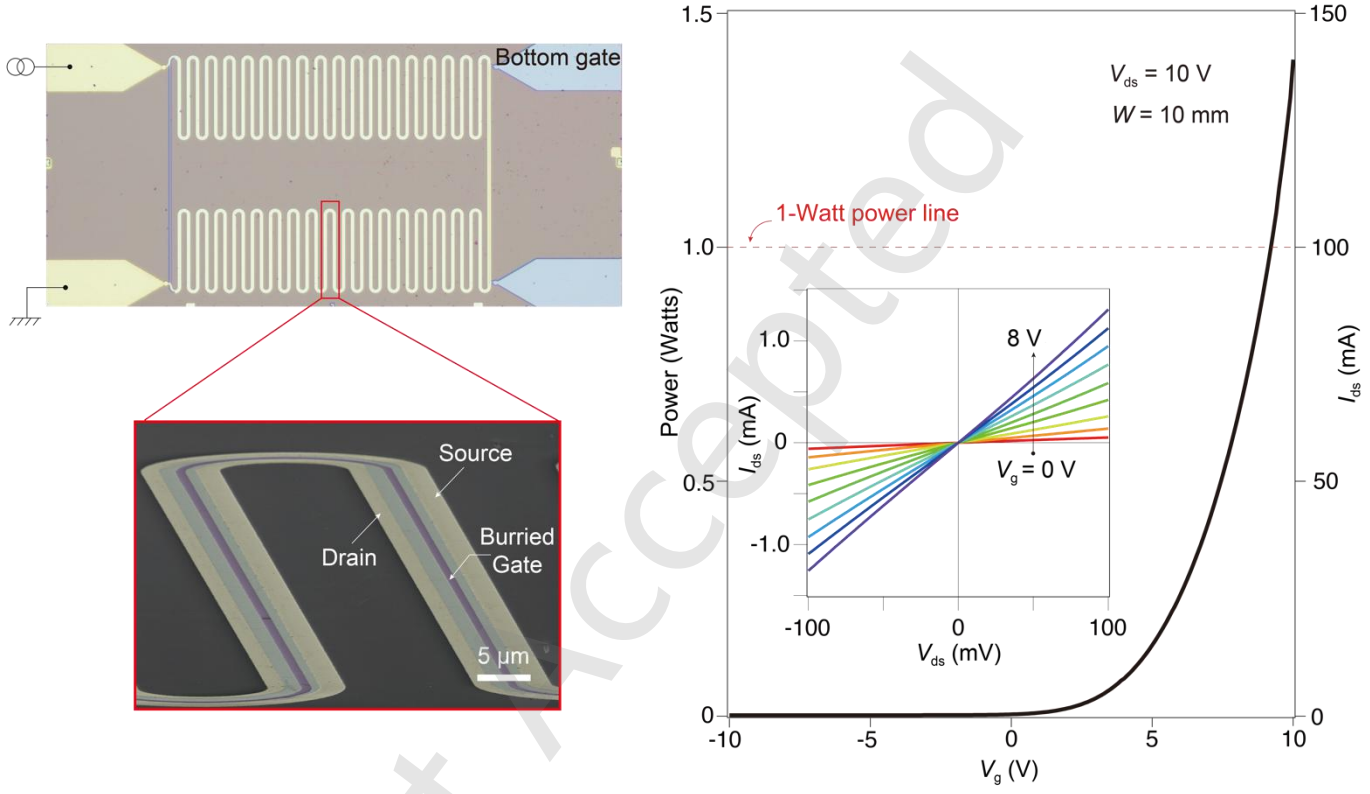

A molybdenum disulphide (MoS_2) device design is reported to achieve watt-level power handling by strategically optimizing channel dimensions to mitigate self-heating. This architecture maintains a high on/off ratio of 10^5 while dissipating ~1 W of power, showcasing the massive potential of 2D semiconductors for high-power electronics.

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Watt-level transistors based on molybdenum disulphide

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[1] *Shenyang National Laboratory for Materials Science, Institute of Metal Research, Chinese Academy of Sciences, Shenyang 110016, China*
[2] *School of Material Science and Engineering, University of Science and Technology of China, Hefei 230026, China*
[3] *Liaoning Academy of Materials, Shenyang 110167, China*
[4] *State Key Laboratory of Wide Band Gap Semiconductor Devices and Integrated Technology, School of Microelectronics, Xidian University, Xi'an 710126, China*
[5] *State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun 130012, China*
[6] *State Key Laboratory of Quantum Optics and Quantum Optics Devices, Institute of Optoelectronics, Shanxi University, Taiyuan 030006, China*
[7] *Collaborative Innovation Center of Extreme Optics, Shanxi University, Taiyuan 030006, China*
[§] *Chengyuan Li, Chen Yan, and Guanran Wang and Yu Bai contributed equally to this work.*

Received: 24 March 2026; **Revised:** 2 May 2026; **Accepted:** 9 May 2026

✉Address correspondence to Hong Wang, hongwang@xidian.edu.cn; Dongming Sun, dmsun@imr.cas.cn; Yu Duan, duanyu@jlu.edu.cn; Zheng Vitto Han, vitto.han@gmail.com Yaning Wang, ynwang@lam.ln.cn

Cite this article: *Nano Research*, 2026, 19, 94908826 https://doi.org/10.26599/NR.2026.94908826

ABSTRACT: Two-dimensional (2D) semiconductor devices hold great promise in specialized operating regimes including radio-frequency, high-temperature, and cryogenic conditions – yet their potential for power handling has received little emphasis, so far. Here we report a molybdenum disulphide (MoS_2) device design that strategically selects the channel width (W) and length (L) to distribute current density and mitigate self-heating, enabling operation at a source-drain bias V_{ds} of 10 V and a drain current I_{ds} of 0.1 A, while maintaining an on/off ratio of 10^5. This corresponds to sustained dissipation P = $I_{ds}V_{ds}$~1 W, and highlights a pathway for watt-level switching in van der Waals electronics. We demonstrate a sensor circuit that uses our watt-level MoS_2 transistors to function as a step-down converter and a switching device. Further, a proof-of-concept on flexible substrates is presented. Our findings mark a step change in 2D power electronics, paving the way for higher-voltage devices compatible with flexible substrates and, ultimately, wearable and conformal power systems.

KEYWORDS: molybdenum disulphide, field effect transistors, Watt-level, power switches, flexible device

1 Introduction

Two-dimensional (2D) semiconductors such as MoS_2 combine an atomically thin and flexible body with a sizable intrinsic hard band gap and open interfaces that can be freely coupled to another layer, attracting tremendous interest in regimes where conventional silicon devices face constraints [1-10]. For instance, high-temperature switches [11], sub-10 nm channel devices [12-14], radio frequency (RF) ring oscillators [15], cryogenic transistors [16], wearable electronics [17,18], as well as hetero-structure photo-detectors [19,20], as well as field-emission devices for vacuum electronics under high electric fields [21,22], have been showcased using 2D semiconductors as a platform [23,24]. Yet, despite demonstrations of various potential applications, the power-handling dimension of 2D semiconductors remains largely non-investigated, so far. Pushing 2D transistors into the Watt-class is of particular interest, as it may open paths toward circuitry such as compact point-of-load conversion, low-voltage step-down stages, and switching elements for sensor nodes-especially for applications on conformal substrates.

In conventional silicon vertical metal-oxide field effect transistors (MOS-FET) devices or high electron mobility transistors (HEMTs), a high tension (up to several hundred volts) between source-drain can be sustained by either introducing a thick low-doping drift layer or adopting a field-plate design [25-32]. Nevertheless, these device architectures are fundamentally unsuitable for flexible, conformal, or wearable implementations. Scaling to Watt class with source-drain voltage of ~ 10 V (and then ideally above 100 V and higher in the future) is a key challenge for

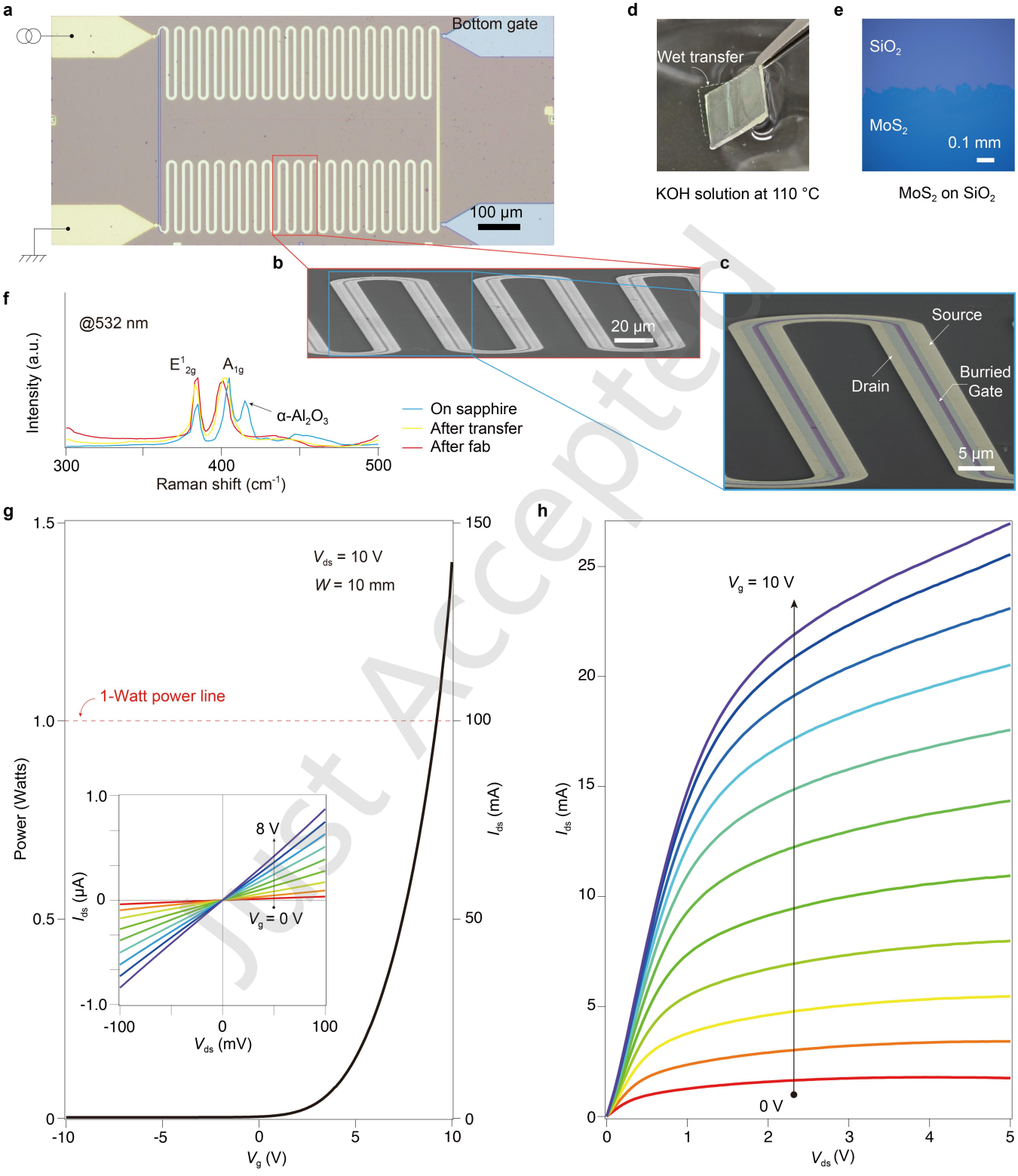

Figure 1 Construction of Watt-class MoS_2 FET. (a) Optical micrograph with meander-line layout. Buried bottom gate can be seen as the bluish part which is covered by a 50 nm Al_2O_3 atomic layer deposited dielectric (scale bar: 100 μm). (b) and (c) are enlarged from the red boxed area in (a), with the high-magnification view marking source, drain, and buried gate (scale bars are 20 and 5 μm, respectively). (d) Optical image of the KOH wet transfer process carried out at a temperature of 110 ℃. (e) Transferred mono-layered MoS_2 film on SiO_2 showing rather uniform coverage over mm ranges. (f) 532 nm Raman before/after transfer and after fabrication, indicating the E^1_{2g}/A_{1g} characteristic peaks, while the sapphire features are gone after transfer. (g) Gate-dependent power $P = I_{ds}V_{ds}$ (left axis) and I_{ds} (right axis) at V_{ds} = 10 V and channel width W = 10 mm. Dashed line highlights the 1 Watt level. Inset in (g) shows ±100 mV I - V sweeps for gate ranges in 0 and 8 V, at a step size of 1 V. (h) Output I_{ds}–V_{ds} for V_g =0 – 10 V, in the V_d range of 0 to 5 V. Samples are tested at ambient conditions unless otherwise noted.

2D semiconductors in this context. It simultaneously requires simultaneously a thin gapped semiconducting channel (for high on/off) with a large current density capability, and high lateral breakdown fields, which balance the power output, I_{ds} and V_{ds} in a single unipolar device. Meanwhile, state-of-the-art MoS_2 and WS_2 FETs have achieved record current densities approaching or exceeding ~ 1 mA/μm in short-channeled devices [33-35], but detailed experiments identify self-heating and limited heat extraction through the channel/oxide interface as the primary bottlenecks in them [36,37]. To date, 2D semiconducting circuits have been limited to milliwatt-level output powers, underscoring the difficulties of combining gain, linearity, and power delivery in atomically thin channels without proper engineering.

In this work, we report a MoS_2 transistor design that strategically chooses channel width (W) and length (L) to distribute current density and mitigate hot-spot formation, allowing sustained operation at V_{ds} = 10 V and I_{ds} = 0.1 A while maintaining an on/off ratio ~ 10^5, which corresponds to continuous dissipation of 1 W in a single device. Beyond raw power, we translate this capability into circuit-level function, demonstrating a sensor circuit in which the watt-level MoS_2 FET acts as a step-down (switching) element. We further present a flexible-substrate proof-of-concept, indicating that the approach is compatible with mechanically compliant platforms. Together, these results document a clear power handling pathway for van der Waals electronics. It may help bridging the gap between laboratory-scale 2D devices and application-oriented power building blocks in distributed, low-footprint systems.

2 Results and discussion

2.1 Construction of watt-level MoS_2 transistors

In order to achieve the goal of 1 watt-class power output, we introduce a meander-line type very wide channel architecture. Fig. 1a shows an optical micrograph of the completed device with a layout that expands the effective channel width W while keeping the footprint compact; a buried (bottom) gate uniformly modulates the atomically thin channel across the full active area. The red-boxed region in Fig. 1a is enlarged in Fig. 1b and c to highlight the detailed higher-magnification views identifying the source, drain, and buried gate contacts, which can be categorized into a MOSFET device geometry. This design takes advantage of breakdown voltage of lateral MoS_2 monolayer, together with a multiplicative amplification effect of many squares connected in parallel by source-drain electrodes. It thus establishes even distribution of high current and realizes millimeter-scale total width W and μm channel length L in a single uni-polar n-type FET.

Figure 1d and e summarize the material preparations. First, a wet-transfer step is included in the process, using KOH solution at 110 ℃ bath to release the MoS_2 monolayer from the sapphire substrate for its growth. We tested several types of single- and poly-crystalline MoS_2 monolayers grown by chemical vapor deposition (CVD). Despite significant sample quality variations among commercial suppliers, the macroscopic crystallinity of CVD-grown MoS_2 does not dominate device performance. While crystallinity affects transport, overall electrical characteristics are primarily dictated by contact interfaces and supplier-dependent point-defect fluctuations, superseding the effects of grain size. More detailed characterization of MoS_2 monolayer film is shown in Fig. S1 in the Electronic Supplementary Material (ESM). Once the PMMA-coated MoS_2 is fully detached from sapphire substrates (indicated by white dashed lines in Fig. 1d), the PMMA/MoS_2 bilayer is then ready to be rinsed in DI water and to be laminated onto SiO_2 wafers, followed by bake-dry in air. Typical MoS_2 thin film after PMMA removal is shown in Fig. 1e, we discuss in Methods further details and Figure S2 in the ESM. The resulting MoS_2/SiO_2 shows uniform coverage over mm scales. Raman spectroscopy at a laser wavelength of 532 nm compares the MoS_2 spectra on sapphire, after transfer, and after device fabrication, shown in Fig. 1f. The characteristic modes E^1_{2g} and A_{1g} remain sharp with only minor shifts, while the α-Al_2O_3 features from sapphire vanish after transfer, indicating preserved crystalline quality and negligible process-induced damage - sufficient for the electrical testing in the following sections.

DC performances of the as-prepared MoS_2 devices are shown in Fig. 1g. At a fixed V_{ds} = 10 V for typical samples with W = 10 mm and L = 1 μm, the power $P = I_{ds}V_{ds}$ (left axis) and the corresponding I_{ds} (right axis) rise steeply with gate bias Vg, crossing the 1-Watt guideline (indicated by the red dashed line in Fig.1g) and reaching the $I_{ds} \approx 0.1$ A regime. The inset shows linear I_{ds}–V_{ds} characteristics within ±100 mV for different V_g, confirming its rather ohmic contact (more details see Figure S3 and S4 in the ESM). The output characteristics in Fig. 1h further provide a complementary I_{ds}–V_{ds} from V_g = 0 to 10 V. It is seen that the channel conductance scales in the low-bias region and approaches quasi-saturation by V_{ds} ~ 4 to 5 V, with the top trace at V_g = 10 V consistent with watt-class dissipation at V_{ds} = 10 V. These data collectively establish the device structure and material integrity, and they verify sustained one-watt operation in a single MoS_2 n-type transistor (also see Figure S5 in the ESM).

2.2 Characterizations of watt-level MoS_2 transistors

We now perform characterizations including high-voltage scaling, contact extraction, benchmarking, and switching behavior of lateral watt-level MoS_2 FETs constructed using above methods. Fig. 2a illustrates the I-V breakdown characteristics measured at fixed width W = 50 μm and channel lengths L = 1, 2, 3, 4, 5 μm. A nearly linear rise of breakdown voltage (indicated by the abrupt drops in the I_{ds}) with L is observed, suggesting a lateral breakdown field E_{BD} ~ 30 V/μm ≈ 0.3 MV cm^{-1}. The drain current remains low until a sharp increase signals soft breakdown (negligible gate leakage currents can be found in ESM Fig. S6); extending L delays this onset to higher V_{ds} and defines the design window for high-tension operation in atomically thin channels. The inset optical micrograph outlines the structure that defines L and W across the device. The scale bar in the inset is 20 μm. ESM Fig. S7 shows a representative cm-sized die carrying an array of test structures.

Figure 2b benchmarks this work against other typical non-silicon thin-film transistor platforms including poly-Si-UTB [38], poly-Si-C [38], IGZO [39], ZnO [40], and IGO [41] using a pentagon chart of thickness, minimum bend radius ρ, on–off ratio I_{on}/I_{off}, maximum drain current I_{ds}, and delivered power in the corresponding systems (the radial axis for thickness decreases outward, in contrast to the ascending scales of the other parameters). The MoS_2 devices studied in this work occupy a favorable regime that combines nanometer-scale thickness and small ρ (which will be introduced in more details in the coming section) with watt-level power delivery.

Figure 2c and d demonstrate temporal behavior of the watt-level MoS_2 switch. Under pulsed gate voltages, the current waveforms $I_{ds}(t)$ at 5 kHz (Fig. 2c) and 10 kHz (Fig. 2d) are stable and rectangular with negligible lagging/deformation within each pulse, indicating that electrostatic modulation dominates over thermal transients on these time scales (20 kHz and 30 kHz can be seen in ESM Fig.8). The repeatability across many cycles and the absence of delayed recovery suggests limited trapping under the employed biases and frequencies, as well. No abrupt degradation or systematic current drift occurs over continuous high-frequency switching within the measured timeframes. Collectively, this dynamic fidelity highlights the electro-thermal resilience and operational reliability of the device platform under sustained high-power driving conditions.

Figure 2e and g plot the statistics of transfer characteristics in our devices. I_{ds}–V_g curves taken at fixed V_{ds} = 8–10 V and increasing total width W = 3, 6, 10 mm reveal

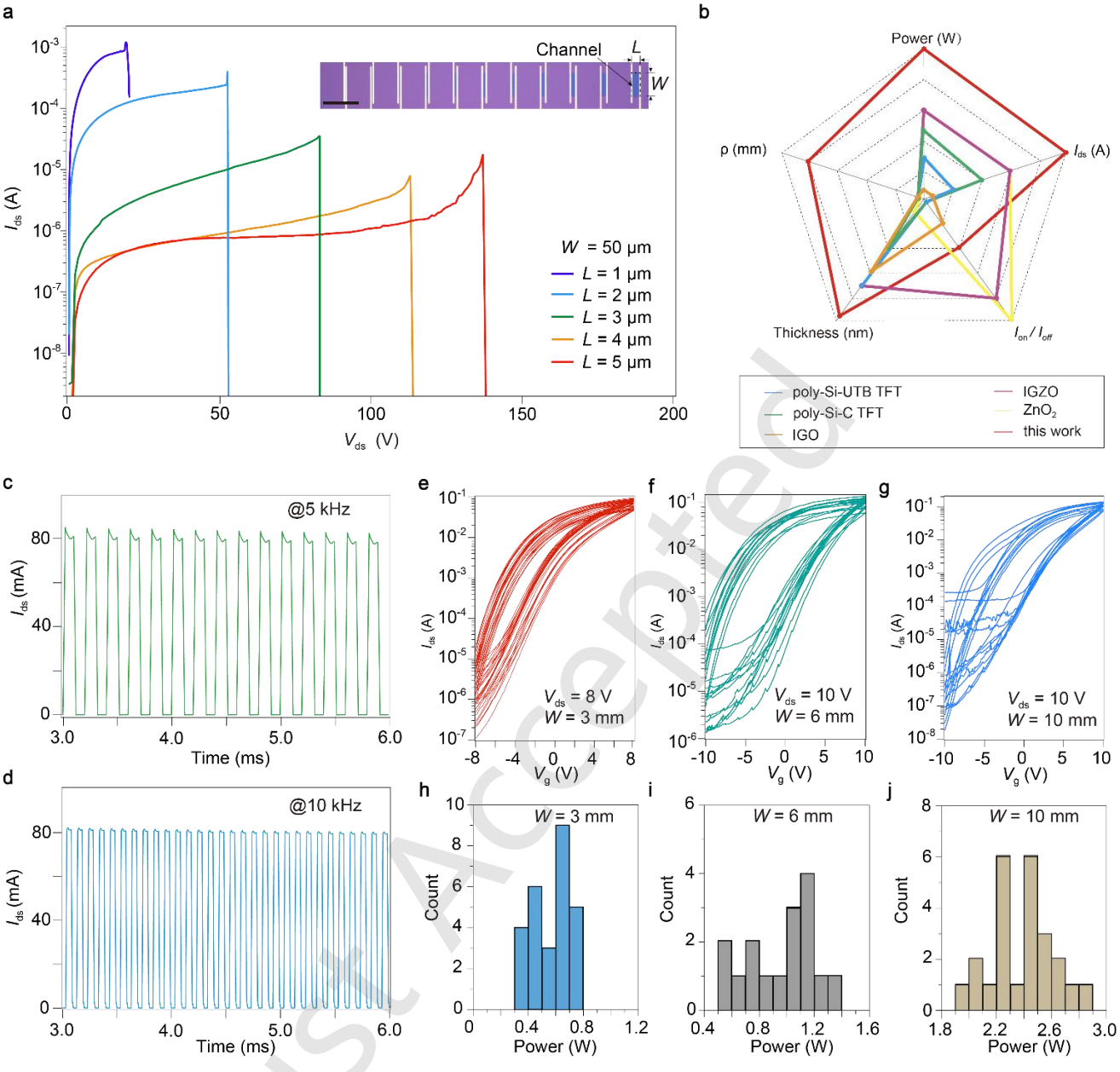

Figure 2 Figure of merits of the watt-level MoS_2 FETs. (a) Lateral breakdown voltage increases with channel length L at fixed width W = 50 μm (b) Benchmark of pentagon-chart of several typical non-silicon thin film FET platforms, including poly-Si UTB, poly-Si-C, IGZO, ZnO, and IGO using a pentagon chart of thickness, minimum bend radius ρ, on–off ratio I_{on}/I_{off}, maximum drain current I_{ds}, and delivered power in the corresponding systems. (c)-(d) Stable temporal behaviors of I_{ds} pulses at 5 and 10 kHz, respectively. (e)-(g) Transfer curves at V_{ds} = 8 – 10 V show on-current scaling with total width W = 3, 6, 10 mm and large I_{on}/I_{off}. (h)-(j) Power histograms shift to higher values with width, confirming watt-class delivery. Samples are tested at ambient conditions unless otherwise noted.

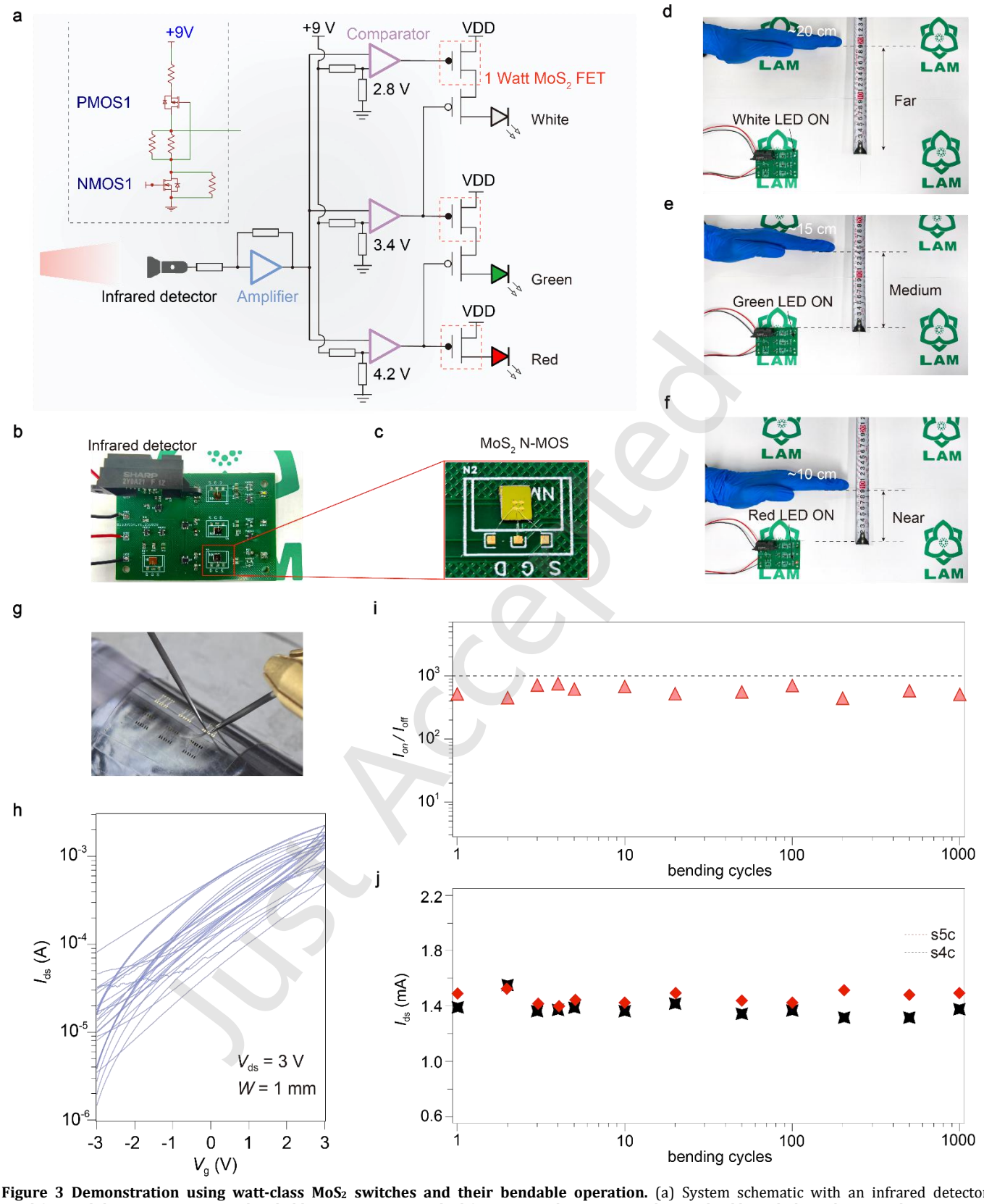

Figure 3 Demonstration using watt-class MoS_2 switches and their bendable operation. (a) System schematic with an infrared detector amplifier, and three comparators at thresholds 2.8, 3.4, 4.2 V supplied from 9 V. Each comparator drives a load branch through a watt-class MoS_2 FET that serves as the low-loss switching element. (b) Assembled printed-circuit board integrating the detector front end, analog stages, and discrete MoS_2 N channel devices. (c) Close-up of the bonded MoS_2 NMOS die on the switching branch. (d) (e) (f) Distance-coded operation: at ~ 20 cm the white indicator is on denoting Far, at ~ 15 cm the green indicator is on denoting Medium, at ~ 10 cm the red indicator is on denoting Near. (g) Bend test setup on a flexible substrate. (h) Transfer characteristics at V_{ds} = 3 V and total width W = 1 mm showing stable gate control across devices. i On off ratio I_{on}/I_{off} versus bending cycles remains near 10^3 up to 1000 cycles. (j) On current I_{ds} at fixed bias for samples s5c and s4c stays within 1.3 - 1.8 mA without systematic drift. Samples are tested at ambient conditions unless otherwise noted.

monotonic on-current scaling with W while preserving large I_{on}/I_{off} (up to 10^5) on a logarithmic axis. The transfer characteristics display pronounced hysteresis, predominantly associated with dynamic charge trapping at

dielectric interfaces and ambient adsorbates typical of non-encapsulated two-dimensional channels. Despite this, time-resolved measurements (Figure 2c,d) reveal that these trap-mediated dynamics do not impair macroscopic switching stability. Instead, under high-frequency pulsed operation, strong electrostatic control governs the device response, enabling stable watt-level power delivery.

Device-to-device dispersion appears mainly at high V_g and is attributed to variations in contact resistance and local defects in the MoS_2 films during growth, transfer, or fabrication process, whereas the subthreshold regime remains tightly clustered. Figure 2h and j summarize maximum sustained power as histograms at the same conditions as Fig. 2e and g, showing a clear upward shift of the distribution from sub-watt to multi-watt as W increases. The trend confirms that geometric current spreading through width scaling is an effective lever for achieving watt-class dissipation in lateral MoS_2 FETs. Device failure beyond the watt-level regime is governed by localized thermal runaway driven by Joule heating. Defect-induced current crowding in large-area CVD-grown MoS_2 leads to hot-spot formation, which, together with constrained heat dissipation and interfacial thermomechanical degradation, culminates in irreversible channel breakdown.

2.3 Watt-level MoS_2 FETs on rigid and flexible substrates

With the successful demonstration of Watt-level MoS_2 FETs, we now examine the watt-class MoS_2 device in an infrared sensing alarm circuit. Such circuits are commonly used in automation safety-distance monitoring (including robotic arms, conveyor lines, and other applications) by detecting infrared in real time and enforcing an ~ 20 cm clearance from the equipment. The implementation comprises a simple step-down stage and a switching element both working at watt level output. Figure 3a depicts the design of the circuitry. The infrared detector delivers a voltage proportional to reflected intensity, which is conditioned by an amplifier and compared against three thresholds at 2.8 V, 3.4 V, and 4.2 V. Each comparator drives a branch through an MoS_2 FET (indicated by the red dashed boxes) that serves as the low-loss switch under a 9 V supply, enabling indicator loads and resistive actuation at watt level. This architecture maps proximity to discrete states so that

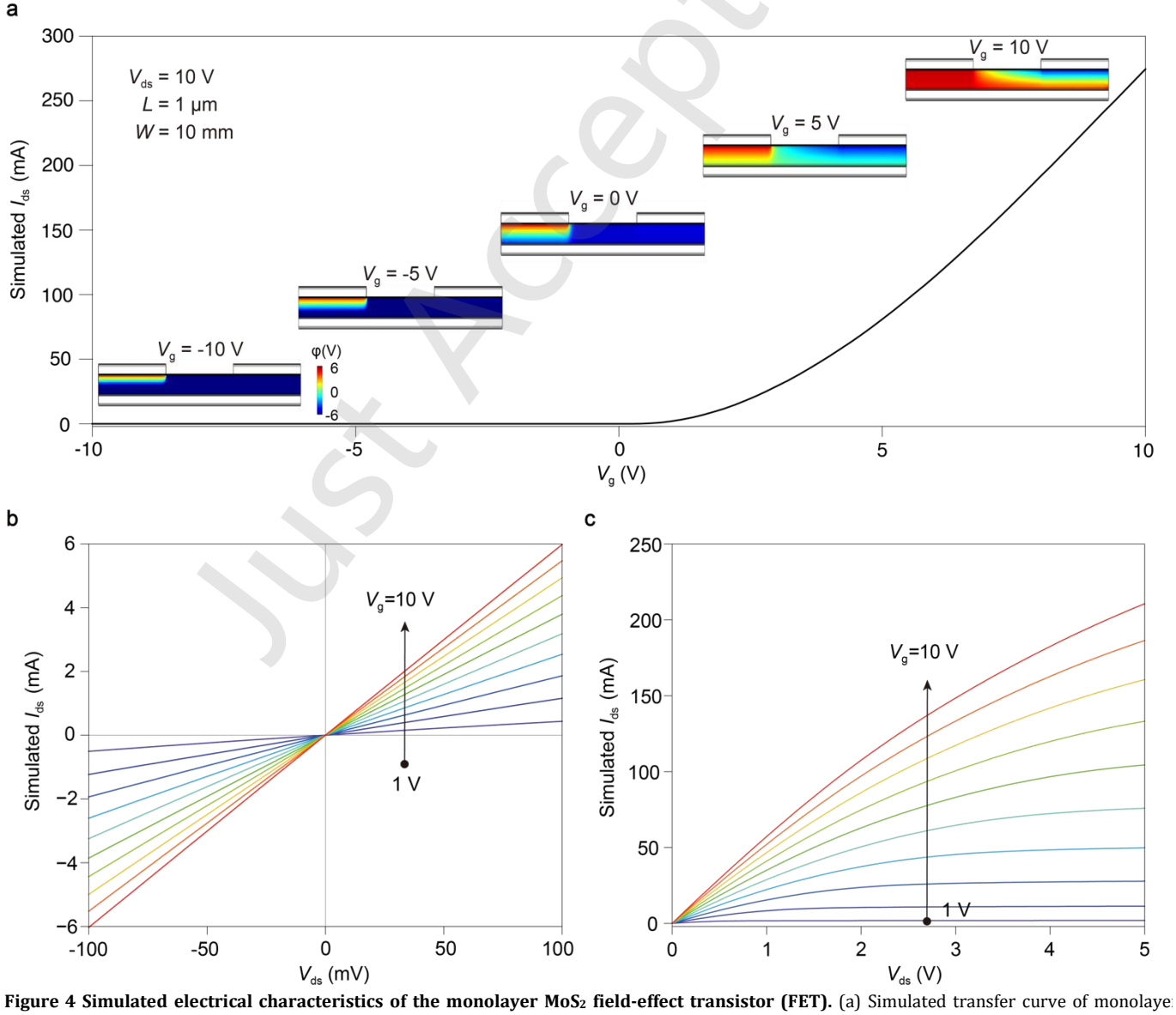

Figure 4 Simulated electrical characteristics of the monolayer MoS_2 field-effect transistor (FET). (a) Simulated transfer curve of monolaye MoS_2 FET with W = 10 mm and L = 1 mm at V_{ds} = 10 V. The insets show electric potential distribution in the MoS_2 and Al_2O_3 layers at representativ gate voltages. Simulated I-V sweeps for gate ranges in 1 and 10 V, at a step size of 1 V, with V_{ds} range of (b) -0.1 to 0.1 V and (c) 0 to 5 V.

rising detector output successively enables the white, green, and red channels, as outlined in Fig. 3a. Video S1 was recorded for the vivid demonstration of the entire infrared sensing alarm process.

Figure 3b shows the assembled printed-circuit board integrating the detector front end, amplifier, comparators, and discrete MoS_2 NMOS devices, while Fig. 3c zooms into the bonded MoS_2 NMOS die that implements the switching element. System demonstrations in Fig. 3d and f validate distance-coded operation: at about ~ 20 cm the white channel is on (Fig. 3d) and the zone is labeled far, at about ~ 15 cm the green channel is on (Fig. 3e) and the zone is labeled medium, at about ~ 10 cm the red channel is on (Fig. 3f) and the zone is labeled near. The transitions are crisp and repeatable, confirming that the MoS_2 switch sustains watt-level drive without visible lag.

Mechanical compliance and electrical stability on flexible substrates are then investigated. A typical device array on a flexible substrate (PI, see more details in ESM Fig. S9 and S10) is shown in Fig. 3g. Transfer characteristics in Figure 3h taken at V_{ds} = 3 V and total width W = 1 mm retain steep gate modulation across the array, with on-current scaling that is consistent from device to device. The on-off ratio in Figure 3i remains near 10^3 over repeated bending up to 1000 cycles, indicating minimal degradation of channel control. Figure 3j tracks I_{ds} at fixed bias through the same bending-cycling for two samples labeled s5c and s4c, which remain clustered around 1.3–1.8 mA without systematic drift (more details can be found in ESM Fig.S11 and ESM Note 1). These results establish that watt-class MoS_2 switches can be in principle integrated into a practical infrared safety alarm while preserving performance under repeated bending. Collectively, these results highlight the robustness and reproducibility of the proposed device platform for conformal, high-power applications based on two-dimensional semiconductors.

2.4 Finite element simulation

To theoretically evaluate the optimal performance of the MoS_2 FET, we constructed an idealized model with identical geometrical dimensions to the experimental devices (W = 10 mm, L = 1μm) and performed finite element simulations using COMSOL Multiphysics. Further details are provided in the Methods. As shown in Fig. 4a, the simulated transfer curve at V_{ds} = 10 V demonstrates excellent agreement with experimental data, showing a similar trend and an on-state current of the same magnitude, with the simulated value being marginally higher. Although a peak on-state current of 300 mA was observed in some experimental devices at the same bias, their elevated off-state leakage meant the overall performance remained within the ideal boundaries defined by the simulation. The insets show electric potential distribution in the MoS_2 and Al_2O_3 layers at representative gate voltages. Fig. 4b and c present the simulated output characteristic curves of the device in the low bias range of V_{ds} = ±100 mV and in the range of V_{ds} = 0–5 V, respectively. The simulated output characteristics show good agreement with the experimental data, and their linear behavior further confirms the ohmic contact between Ag/Au and MoS_2. However, the simulated current values are consistently higher than the experimental ones across all bias conditions, quantitatively reflecting the performance degradation caused by non-ideal factors in the current fabrication process and material quality. Therefore, with subsequent process optimization and improved material quality, there is clear room for further enhancement of device performance. Model predictions indicate that, under ideal conditions, the channel dimensions employed in this work have the potential to enable MoS_2 FETs to achieve an output power close to 3 W.

3 Conclusion

To conclude, we have demonstrated that atomically thin power transistors can operate in the watt regime while retaining the defining advantages of two-dimensional semiconductors. A lateral MoS_2 FET that combines a buried gate, meander-line width scaling, and a MOSFET-like overall architecture that sustains V_{ds} = 10 V and I_{ds} ≈0.1 A, yielding ~ 1 W with on/off ~ 10^5. We mapped high-voltage scaling consistent with lateral breakdown fields ~ 30 V μm^{-1} and verified stable pulsed switching at 5–10 kHz. Based on this testbed, we showcased a compact infrared safety-distance alarm where a watt-class MoS_2 switch enforces ~ 20 cm standoff from a 9 V rail. Further, we showed robust operation on flexible substrates with I_{on}/I_{off} ~ 10^3 retained after 1000 bend cycles and steady Ids under repeated deformation. Together, our results establish a leap forward in 2D power electronics, providing a quantitative foundation for future optimization in thermal pathways, field-managed lateral drift regions, and to extend the operating voltage toward ~ 100 V and beyond. It thus holds promise in flexible point-of-load converters, distributed sensor nodes, and conformal drivers that bridge laboratory 2D devices to mechanically compliant power systems.

4 Methods

4.1 Transfer of wafer-scale MoS_2

The polymethyl methacrylate (PMMA) was spin-coated at a speed of 600 rpm for 6 s and 2000 rpm for 1 min on MoS_2/sapphire, then baked at 180 ℃ for 1 min. After coating the PMMA layer, samples were immersed in KOH solution at 110 ℃ for half an hour. The samples were then picked up from the solution and transferred into deionized water to release the PMMA/MoS_2 layer from the sapphire. The MoS_2/PMMA was transferred to fresh deionized water twice, to remove the potassium hydroxide residue. The cleaned MoS_2/PMMA stack was transferred to the target substrate and the excess deionized water was air-dried naturally for more than 8 hours. Further annealing at 140 ℃ for 10 min enhanced the adhesion between the MoS_2 and the substrate. The PMMA was removed by soaking for 30 min with fresh acetone, with this being done at least three times.

4.2 Fabrication of Watt-level MoS_2 transistors

Monolayer MoS_2 film was fabricated using the wet-transfer method on flexible PI or Si/SiO_2 (300 nm) substrates with bottom local gate (more details see ESM Fig.S12 and Fig.S13). Atomic layer deposition system was then used to deposit 60 nm Al_2O_3 on substrates at 80 ℃ with

trimethyl aluminum (TMA) and oxygen plasma. The channels, local bottom gates and source/drain contacts were defined by electron-beam lithography (Zeiss Sigma 300 & Raith ELPHY Quantum). The electrodes were deposited by a thermal evaporator, with typical Cr/Au (or Ag/Au) thickness of ~5/30 nm (or 25/25 nm).

4.3 Atomic layer deposition

During the PEALD-Al_2O_3 preparation process, high-purity Ar gas (99.999%) was employed as both the carrier gas and precursor cleaning gas, with a flow rate of 90 sccm. TMA (99.999%) was maintained at room temperature, and an oxygen plasma was generated using 15 sccm oxygen at 100 W RF power. PEALD-Al_2O_3 growth employed a multi-step short pulse (MSP) [42] process configured as follows: TMA pulse 0.03 s, TMA purge 80 s, TMA pulse 0.03 s, TMA purge 80 s, oxygen plasma pulse 10 s, oxygen plasma purge 100 s. ALD fundamentally involves the reaction between precursor molecules and surface groups on the substrate. Depending on the size of the precursor molecules and the density of surface groups, certain reaction sites may become physically obstructed during the process, preventing contact and reaction with subsequent precursor molecules. This phenomenon is termed ALD steric hindrance. Following the purge stage in the ALD process, a portion of precursor molecules may remain within the chamber. These residual molecules consume part of the subsequent precursor introduced into the chamber, triggering CVD reactions within the chamber. This results in the formation of particles that deposit onto the film surface, thereby compromising the film's forming density. Moreover, under low-temperature deposition conditions, the thermal motion velocity of molecules decreases, prolonging the relaxation time of both precursor and by-product molecules. This also induces transient steric hindrance before and after the reaction, termed transient steric hindrance. Byproduct gas molecules generated during ALD reactions may similarly obscure active sites before departing the film surface, causing transient steric hindrance. The MSP process represents an optimized ALD deposition technology. It mitigates Volmer-Weber growth and transient steric hindrance effects arising from excess precursor residues generated during adsorption, thereby exposing additional active sites previously obscured by transient steric hindrance from precursors bound via van der Waals forces and other interactions. This enhances precursor adsorption onto active sites, consequently improving film forming density.

4.4 Finite element simulations.

Finite element simulations were performed based on COMSOL Multiphysics software using the 2D Semiconductor Module. The simulated structure comprised a 25 nm Ag source–drain electrode, a monolayer MoS_2 channel, a 60 nm Al_2O_3 dielectric layer (relative dielectric constant ε_r = 9.1) [43], and a 30 nm Au gate electrode. Ag electrodes were treated as ohmic contact, and the MoS_2 channel dimensions matched the fabricated devices (W = 10 mm, L = 1 μm) and received the experimentally extracted doping concentration n = 1.5 × 10^{17} cm^{-3} for model simulation converging. COMSOL simulation was performed at 300 K, and all remaining material parameters were taken from the built-in COMSOL materials database without modification [44].

Electronic Supplementary Material: Supplementary material (please provide the brief detail of the ESM) is available in the online version of this article at https://doi.org/10.26599/NR.2026.94908826.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and/or the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request."

Acknowledgements

This work is supported by the National Key R&D Program of China (2022YFA1203903) and the National Natural Science Foundation of China (NSFC) (Grant Nos. 92265203, 12104462, 11974357, U1932151, 12204287, 12304237, 92464105, and 11974027). Z. V. H. acknowledges the support of the Fund for Shanxi "1331 Project" Key Subjects Construction, and the Innovation Program for Quantum Science and Technology (grant no. 2021ZD0302003).

Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

Y.W., Z.H., Y.D., D.S., and H.W. conceived the experiment and supervised the overall project. C.L. and Y.W. performed the device fabrications and electrical measurements; C.Y., C.L., Y.W. and H.W. performed the circuit designs; G.W. and Y.D. contributed to atomic layer deposition in the device fabrications; Y.B., X.S., M.Z., N.R., D.S., and H.W. contributed to sample fabrications; Y.B. performed finite element simulations; Y.W., C.L., and H.Z. analyzed the experimental data. The manuscript was written by Y.W., Z.H. and C.L. with discussion and inputs from all authors.

Use of AI statement

None.

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Electronic Supplementary Material

Watt-level transistors based on molybdenum disulphide

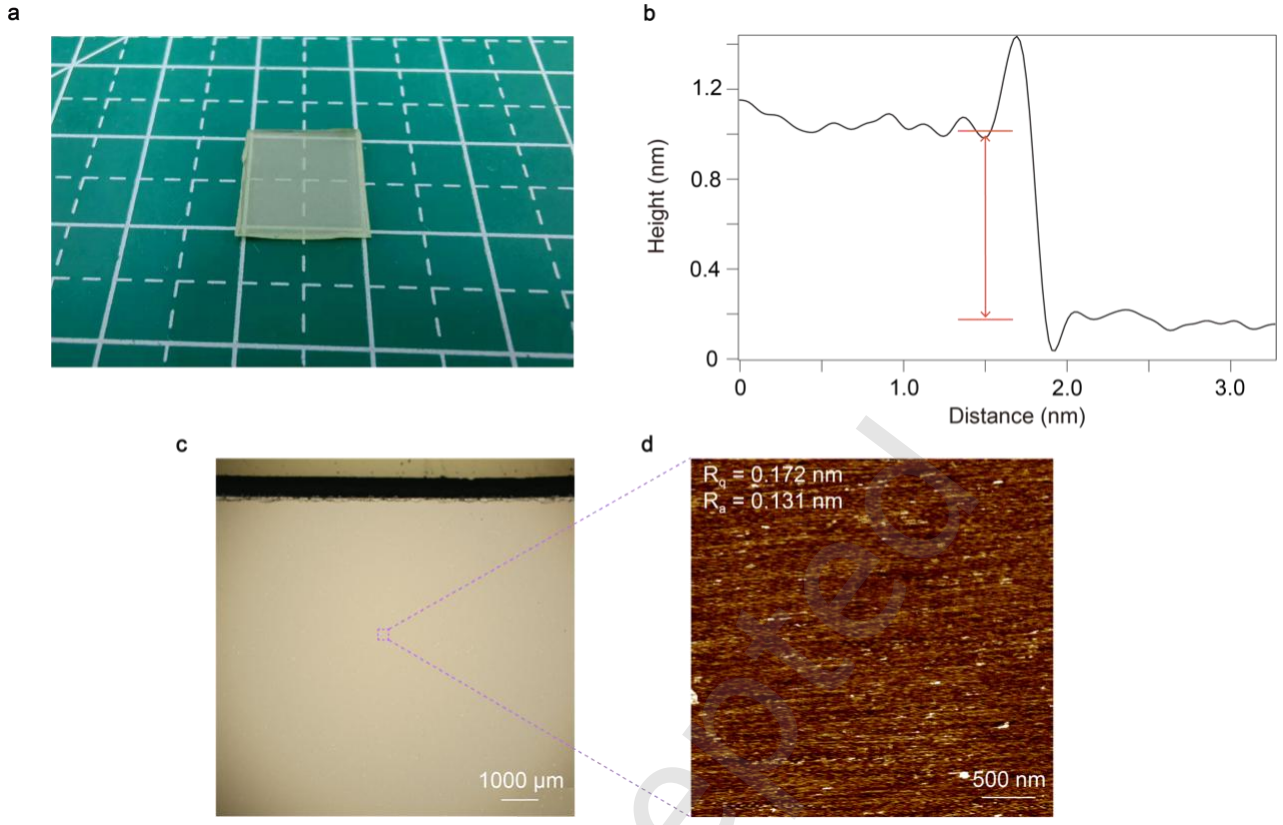
Chengyuan Li[1,2,3,§], Chen Yan[4,§], Guanran Wang[5,§], Yu Bai[3,§], Hanwen Wang[3], Xuanzhe Sha[6,7], Meng Zhang[6,7], Naijie Ren[6,7], Hong Wang[4]✉, Dongming Sun[1]✉, Yu Duan[5]✉, Zheng Vitto Han[3,6,7]✉, and Yaning Wang[3]✉

[1] *Shenyang National Laboratory for Materials Science, Institute of Metal Research, Chinese Academy of Sciences, Shenyang 110016, China*
[2] *School of Material Science and Engineering, University of Science and Technology of China, Hefei 230026, China*
[3] *Liaoning Academy of Materials, Shenyang 110167, China*
[4] *State Key Laboratory of Wide Band Gap Semiconductor Devices and Integrated Technology, School of Microelectronics, Xidian University, Xi'an 710126, China*
[5] *State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun 130012, China*
[6] *State Key Laboratory of Quantum Optics and Quantum Optics Devices, Institute of Optoelectronics, Shanxi University, Taiyuan 030006, China*
[7] *Collaborative Innovation Center of Extreme Optics, Shanxi University, Taiyuan 030006, China*
[§] *Chengyuan Li, Chen Yan, and Guanran Wang and Yu Bai contributed equally to this work.*

✉Address correspondence to Hong Wang, hongwang@xidian.edu.cn; Dongming Sun, dmsun@imr.cas.cn; Yu Duan, duanyu@jlu.edu.cn; Zheng Vitto Han, vitto.han@gmail.com Yaning Wang, ynwang@lam.ln.cn

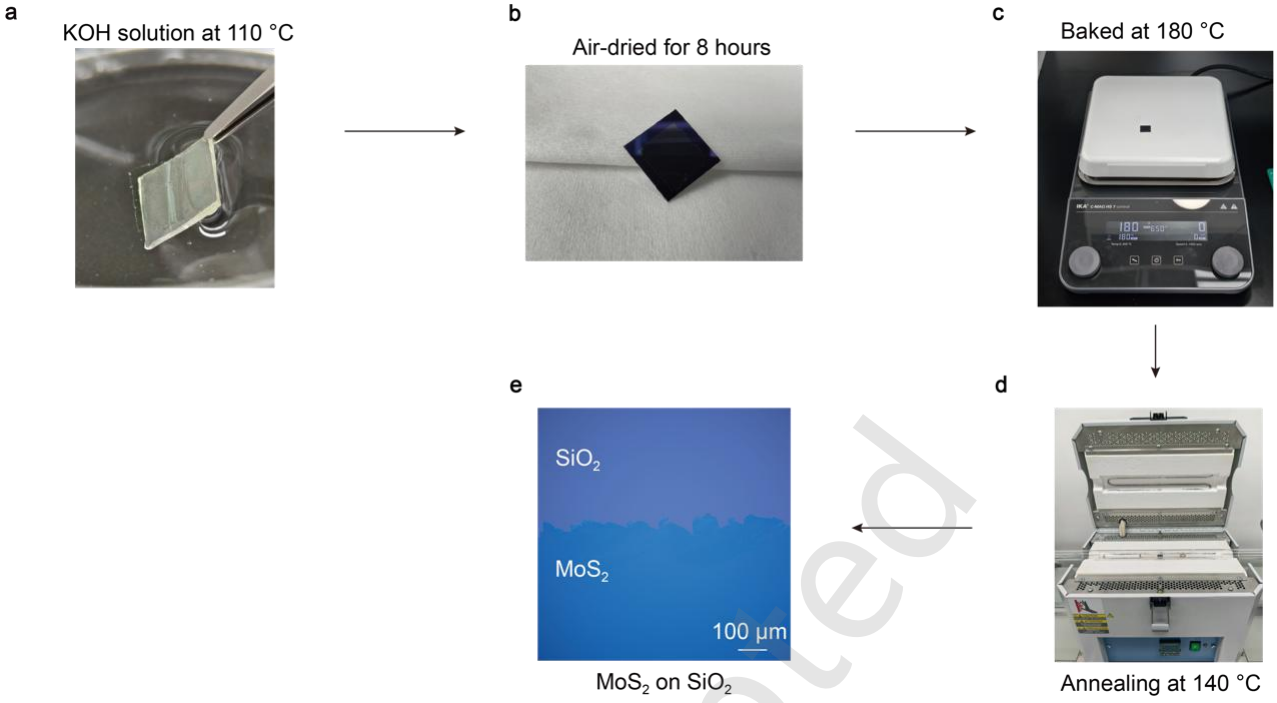
Supporting information to https://doi.org/10.26599/NR.2026.94908826

1. Characterizations of high-quality monolayer MoS_2 film.



S1. Characterizations of high-quality monolayer MoS_2 film. (a) Photograph of 1 × 1 cm^2 monolayer MoS_2 film on sapphire substrate. (b) AFM height profile of the MoS_2 layer with a thickness of approximately 0.92 nm. (c) Local optical image of monolayer MoS_2 film. (d) Surface roughness of monolayer MoS_2 film. The average roughness (R_a) and the root mean square roughness (R_q) were 0.172 nm and 0.131 nm, respectively.

2. Optical images of the wet-transfer process.

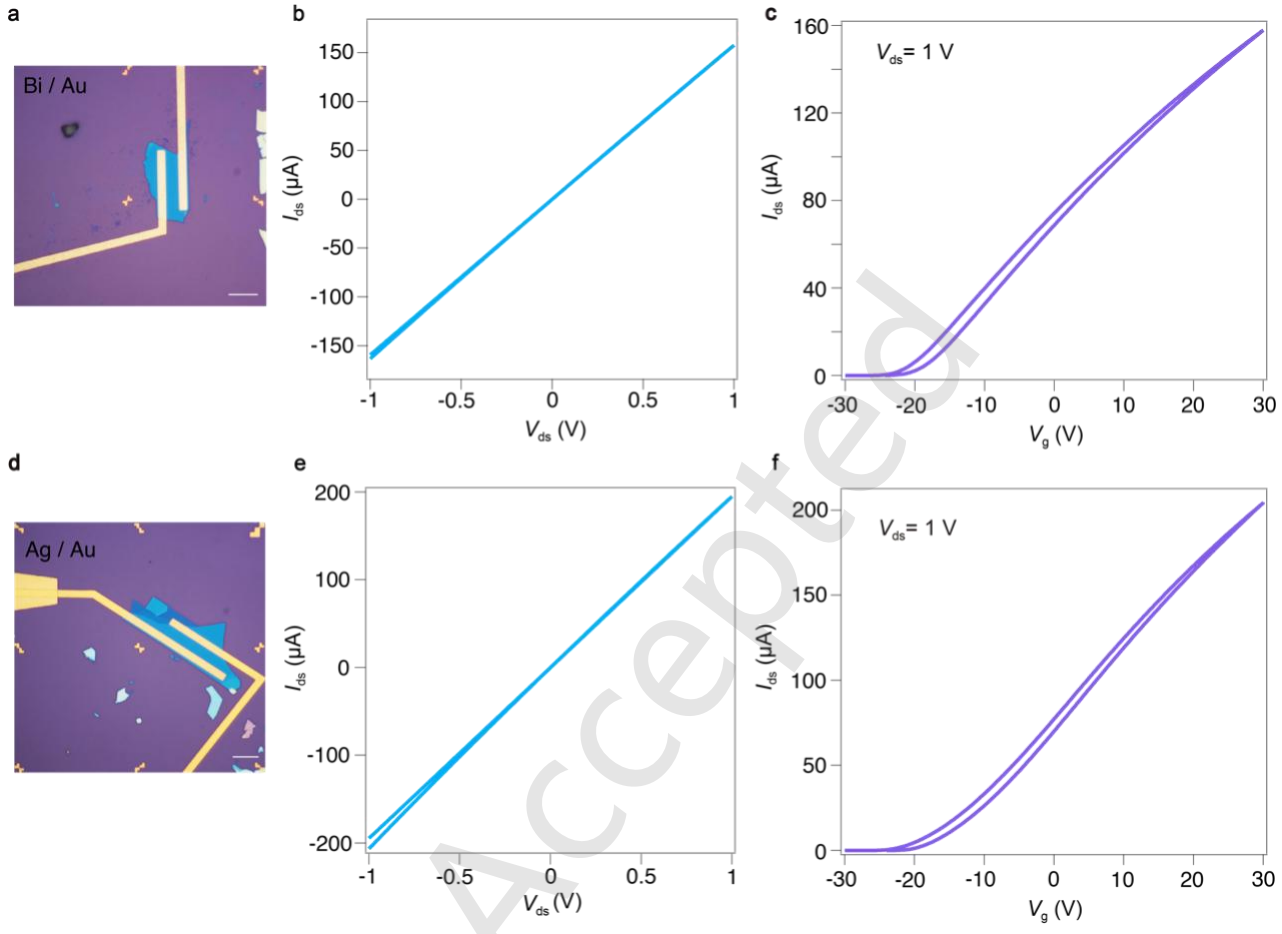


S2. Wet transfer process involves the following steps: (a) The MoS_2 film with PMMA was immersed in KOH solution at 110 °C for half an hour. (b) The MoS_2/ PMMA stack was transferred to the Si/ SiO_2 substrate and air-dried naturally for more than 8hours. (c) The sample was then baked at 180 °C for 30 mins. (d) Annealing at 140 °C for 10 min enhanced the adhesion between the MoS_2 and the substrate. (e) Optical image of the MoS_2 on Si/ SiO_2 substrate, the white scale bars in the bottom right corners represent 100 μm.((a) and (e) are same as Fig.1(d)-(e) in the paper)

Address correspondence to First A. Firstauthor, email1; Third C. Thirdauthor, email2

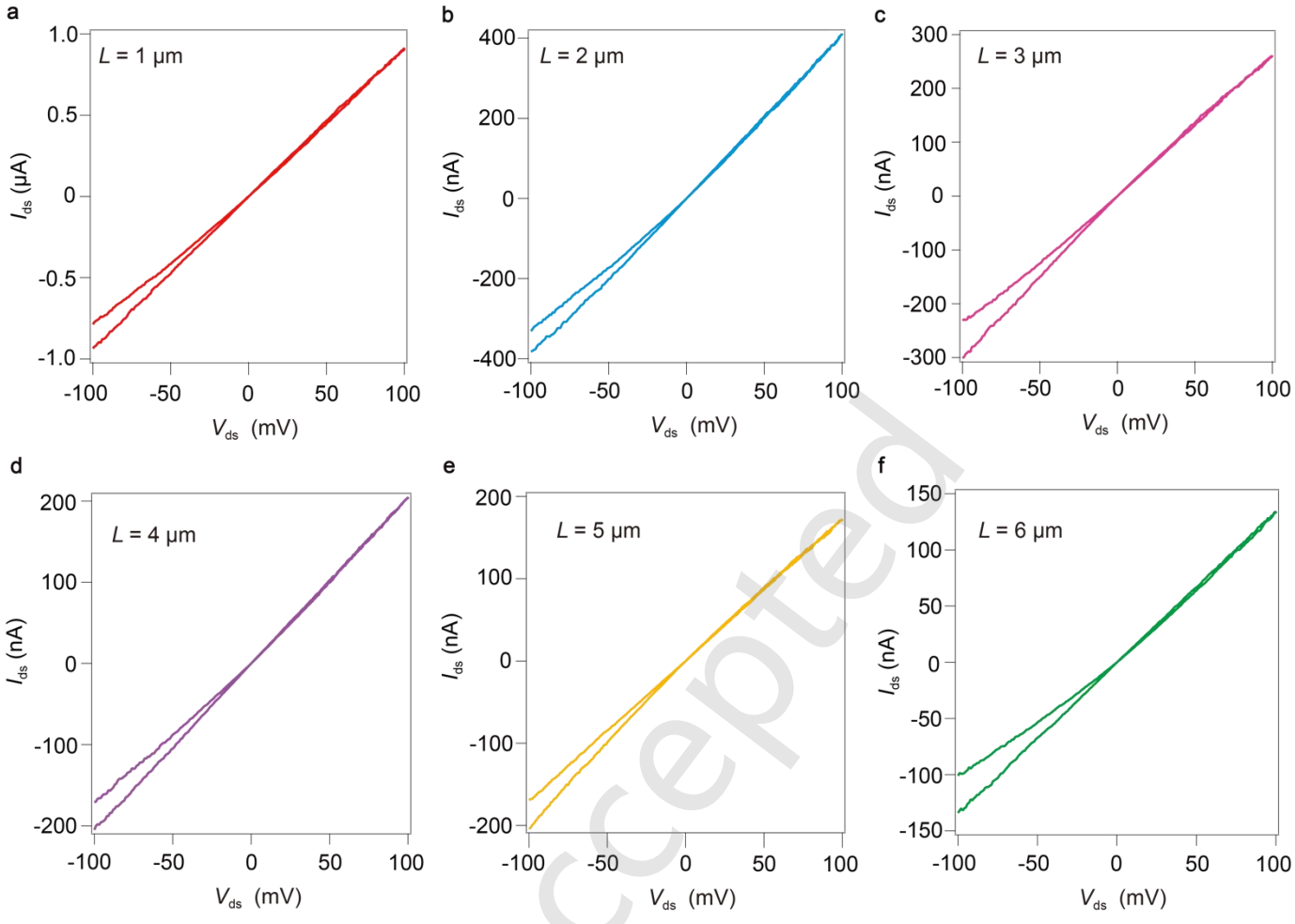
3. Electrical performance of MoS_2 withdifferent contact electrodes.

Recently, low-melting-point metals have emerged as potential candidates for forming ohmic contacts with the MoS_2 channel. Here, we investigated the electrical properties of mechanically exfoliated MoS_2 with Bi and Ag contact electrodes at room temperature. The results indicate that both the *I*–*V* curves and field-effect characteristics exhibited no discernible differences as shown in Fig.4b. Owing to the inherent thermal instability of Bi, Ag was adopted as the contact electrode to ensure improved reliability in device fabrication.



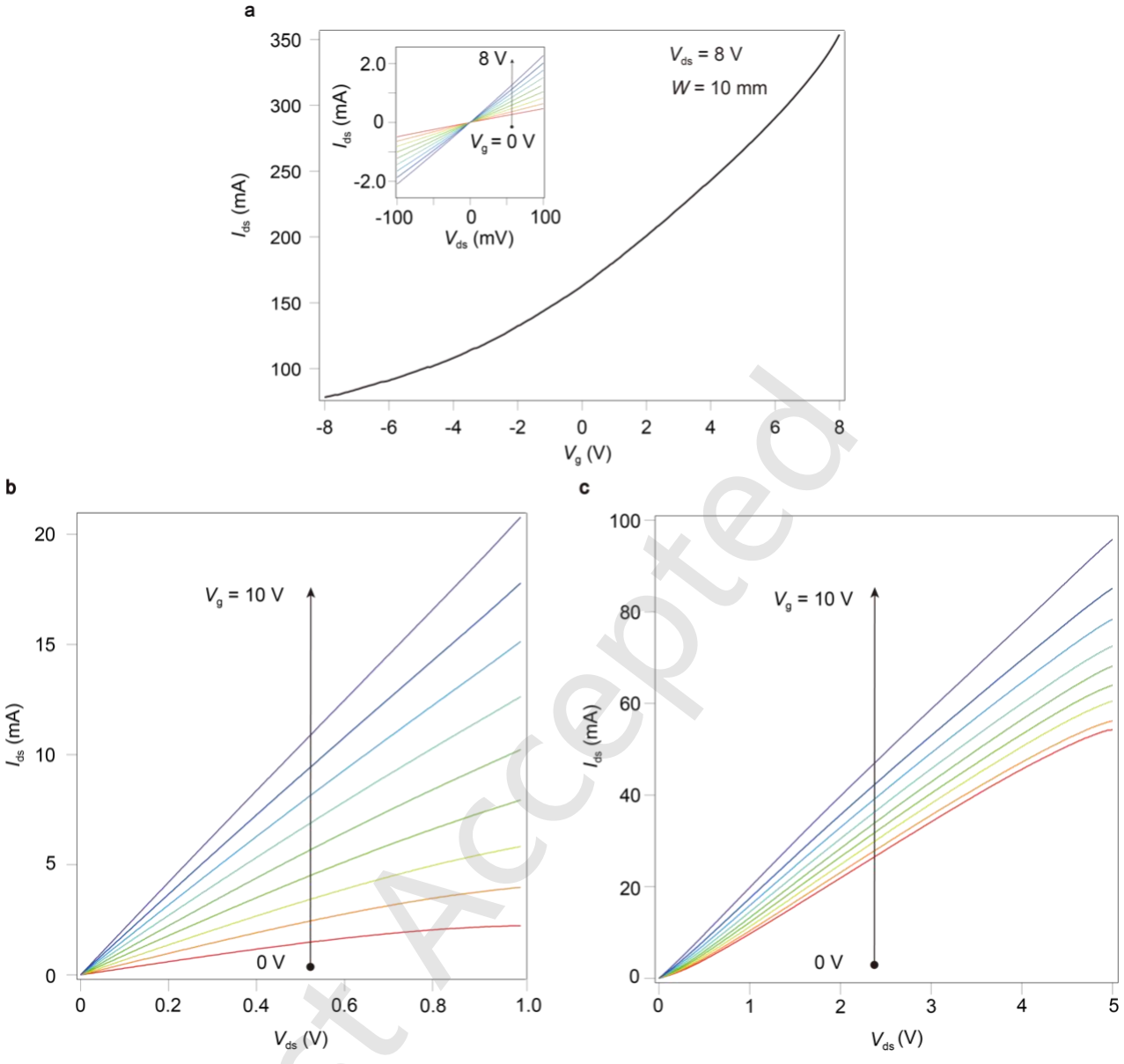
S3. Electrical performance of MoS_2 with Bi and Ag contact electrodes at room temperature. (a)and (d)are optical images of devices based on mechanically exfoliated few-layer MoS_2. The white scale bars in the bottom right corners represent 5 μm. (b) and (e) are the linear I_{ds}-V_{ds} curves at V_g =0 V. (c) and (f) are transfer curves measured for a typical n-type MoS_2 under V_{ds} =1 V.

4. Output characteristics of MoS_2 FET.



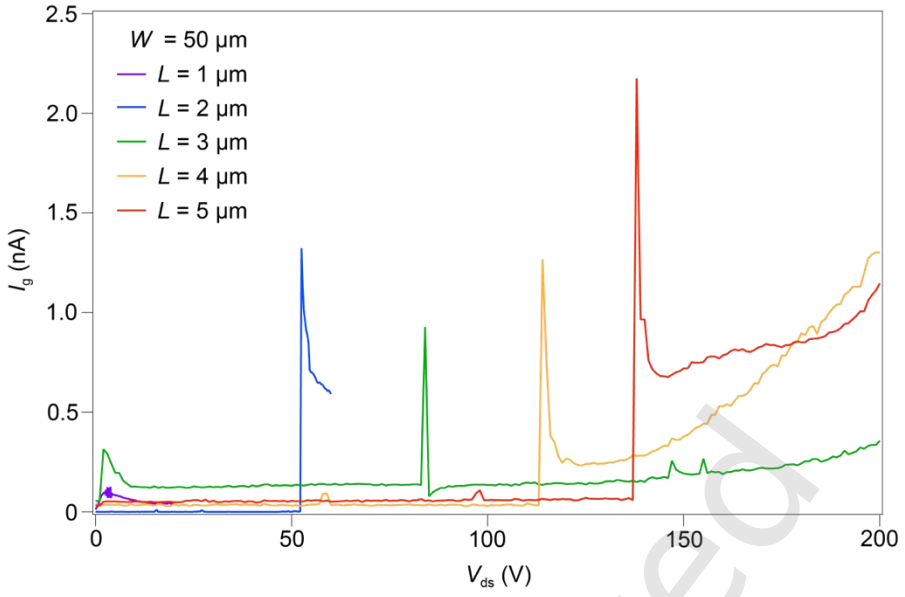
S4. Output characteristics of MoS_2 FET with SiO_2 serving as gate dielectric. Data obtained with 2-probe configuration and standard DC measurements in ambient conditions. The linear I_{ds} -V_{ds} curves of MoS_2 at V_{tg} = 30 V with W= 50 μm.

5. Transfer curve and output characteristics of a typical MoS_2 watt-level transistor.



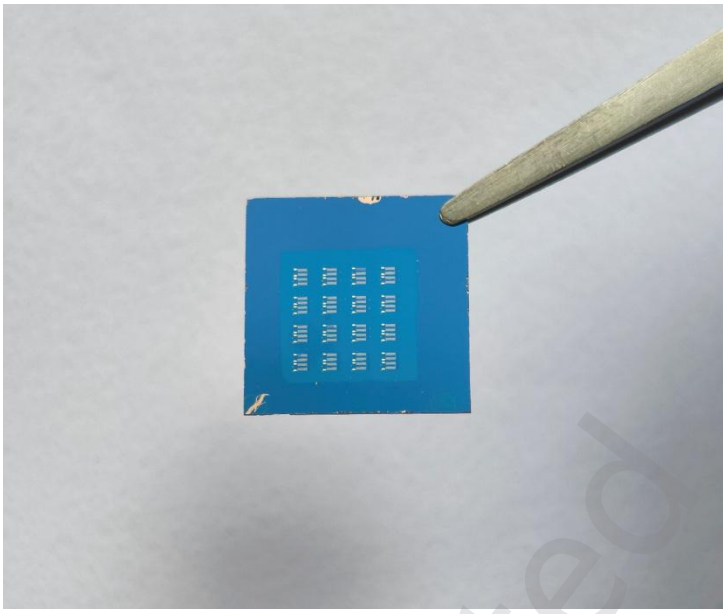
S5. Transfer curve and output characteristics of a typical MoS_2 watt-level transistor with W= 10 mm. (a) Gate-dependent power I_{ds} at V_{ds}= 8 V and channel width W = 10 mm. Inset in (a) shows ±100 mV I-V sweeps for gate ranges in 0 and 8 V, at a step size of 1 V. Output I_{ds}–V_{ds} for V_g= 0 –10 V, in the V_{ds} range of 0 to 1 V and 5 V as shown in (b) and (c).

6. Negligible gate leakage currents in breakdown devices.



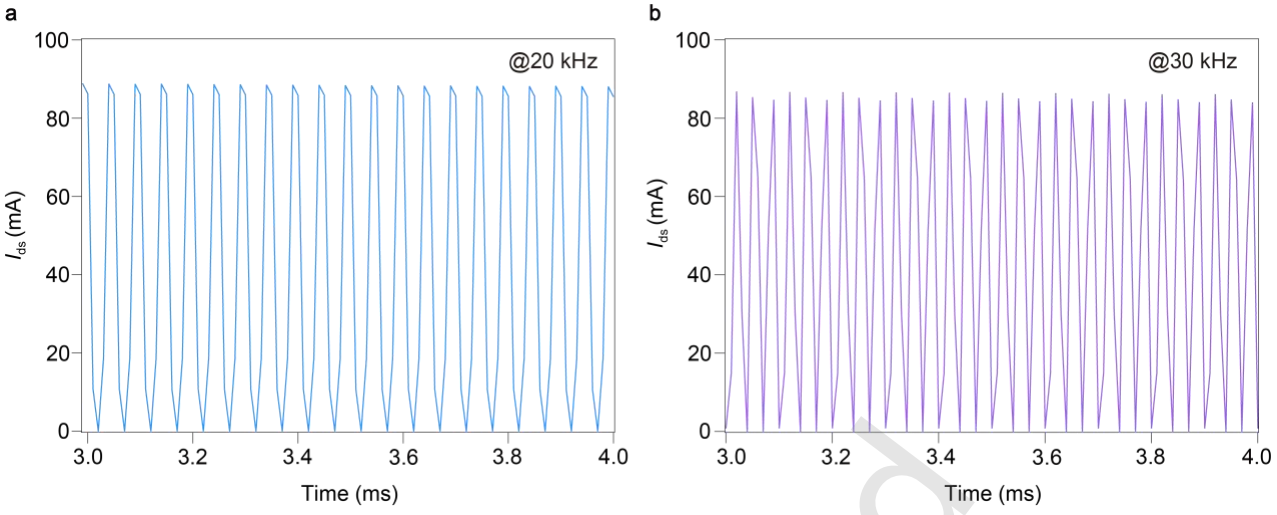
S6. Negligible gate leakage currents in breakdown devices with *W*= 50 µm and channel lengths *L*= 1, 2, 3, 4, 5 µm.

7. A representative cm-sized die carrying an array of test structures.



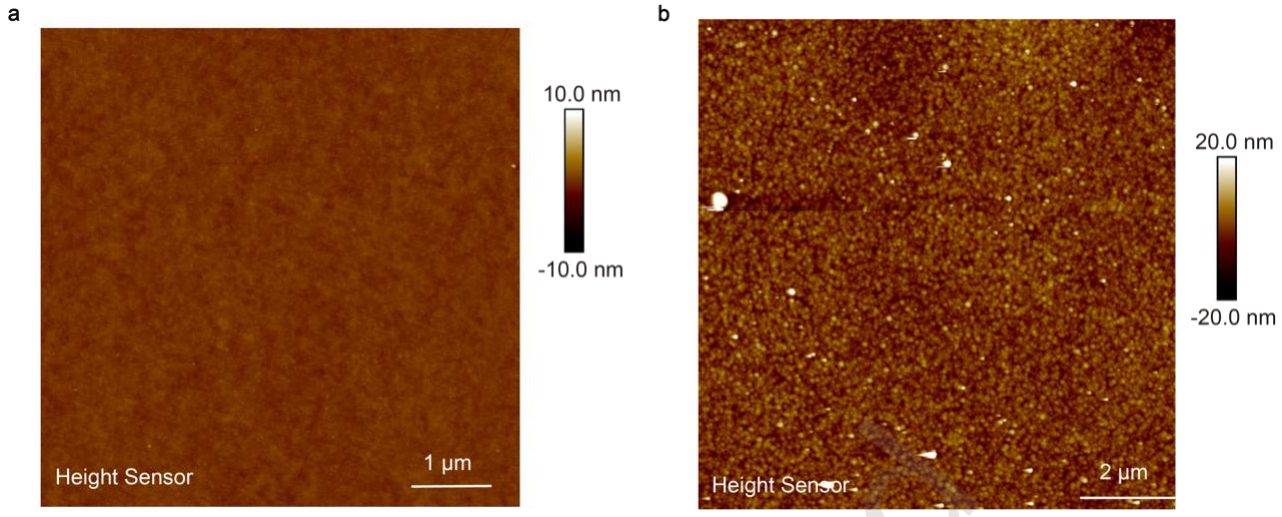
S7. A representative cm-sized die carrying an array of test structures.

8. Stable temporal behaviors of I_{ds} pulses at 20kHz and 30 kHz.



S8. Stable temporal behaviors of I_{ds} pulses at 20 kHz and 30 kHz. The drain current was measured at terminal Keithley 2902A under V_{ds}= ± 5 V square-wave excitation provided by Function Generator.

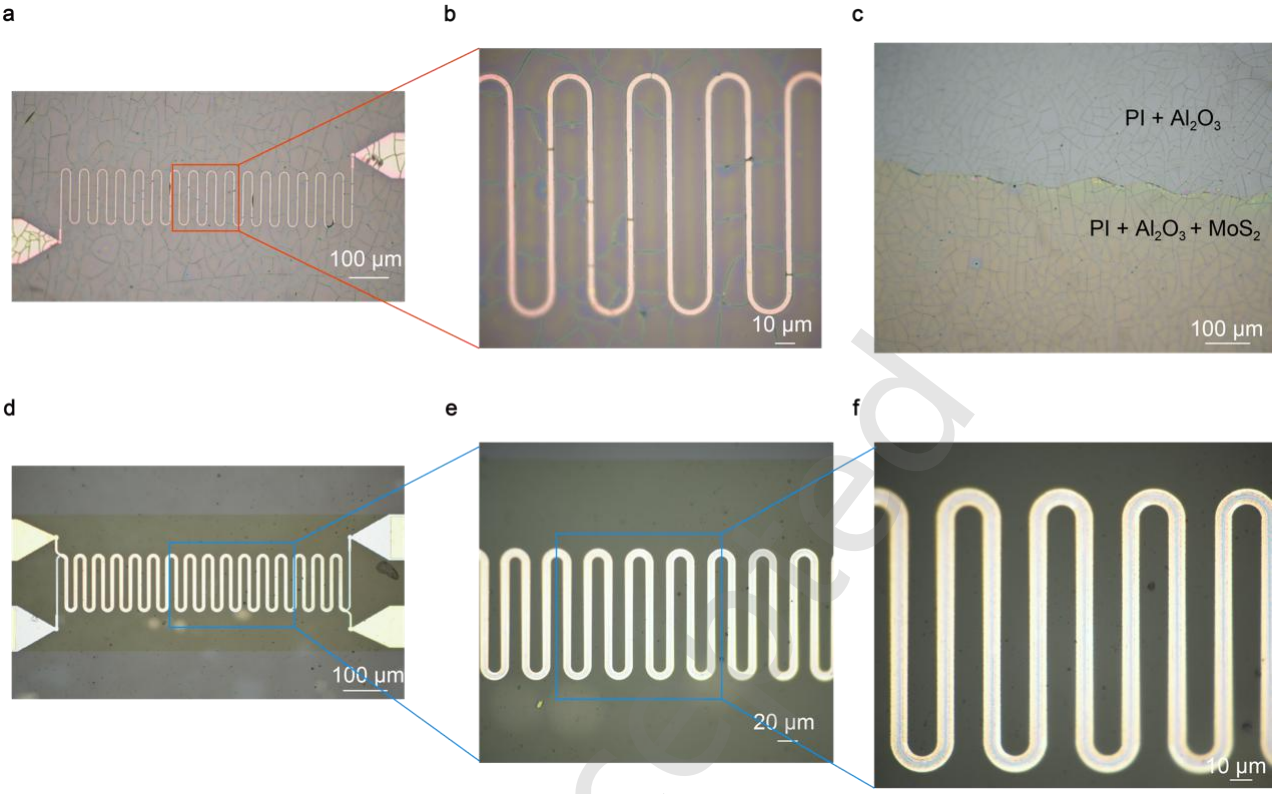
9. The AFM image of the surface roughness.



S9. The AFM image of the surface roughness. AFM images of (a) PI substrate and (b) Al_2O_3/ PI.

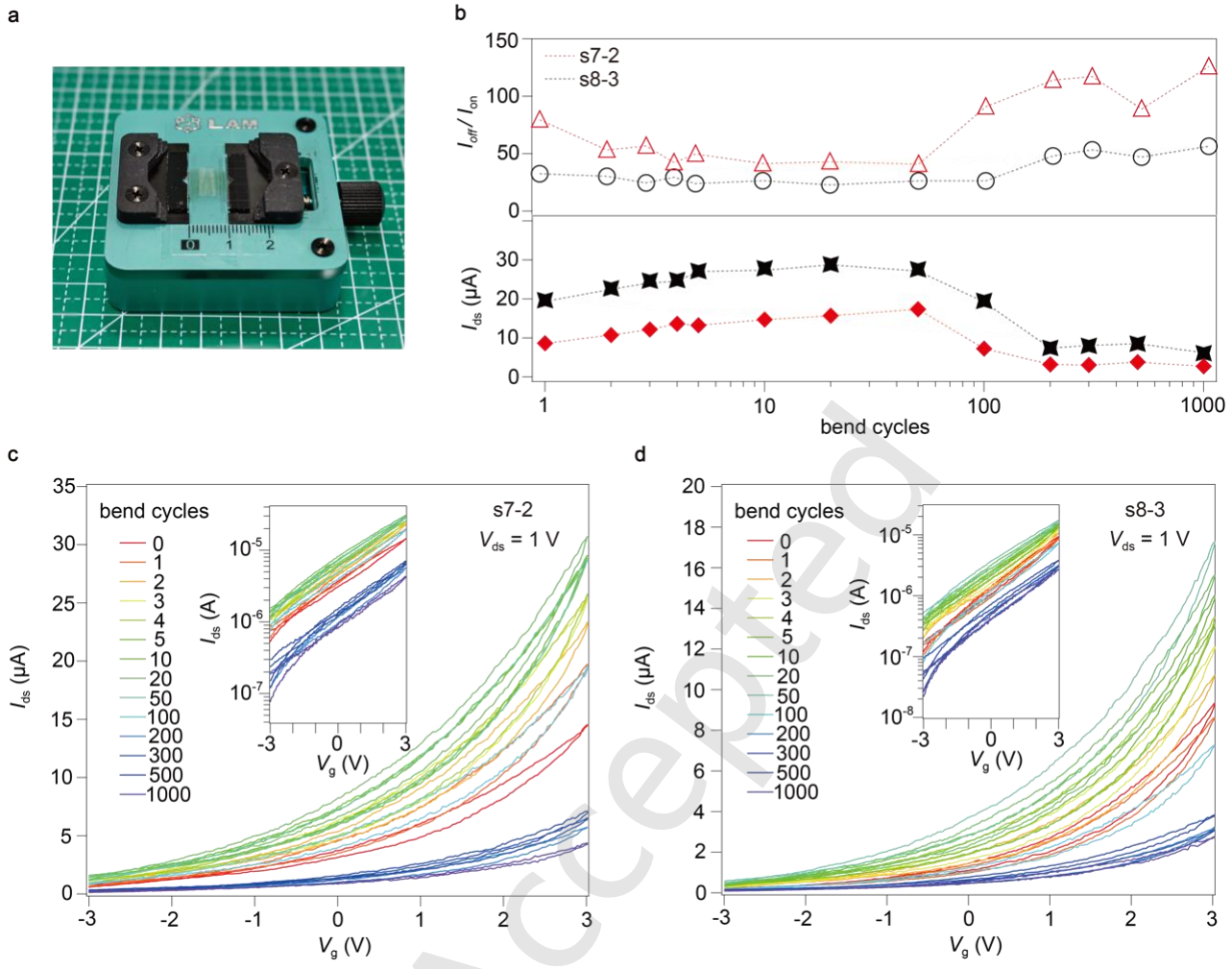
10. Challenges of surface fissures in flexible substrates.

A dielectric layer was deposited on the top surface of PI substrate, and due to stress or the mismatch in thermal expansion coefficients, surface fissures formed in the dielectric layer during the subsequent fabrication process. In this work, we employed a bilayer dielectric to address the issue described above.



S10. Challenges of surface fissures in flexible substrates. Optical micrograph of MoS_2 FET with W = 1mm and L = 1 μm. Surface fissures formed in the dielectric layer after the wet-transfer process as shown in (a)-(c). (d)-(e) The surface of is flat and smooth after adopted a bilayer dielectric growth process.

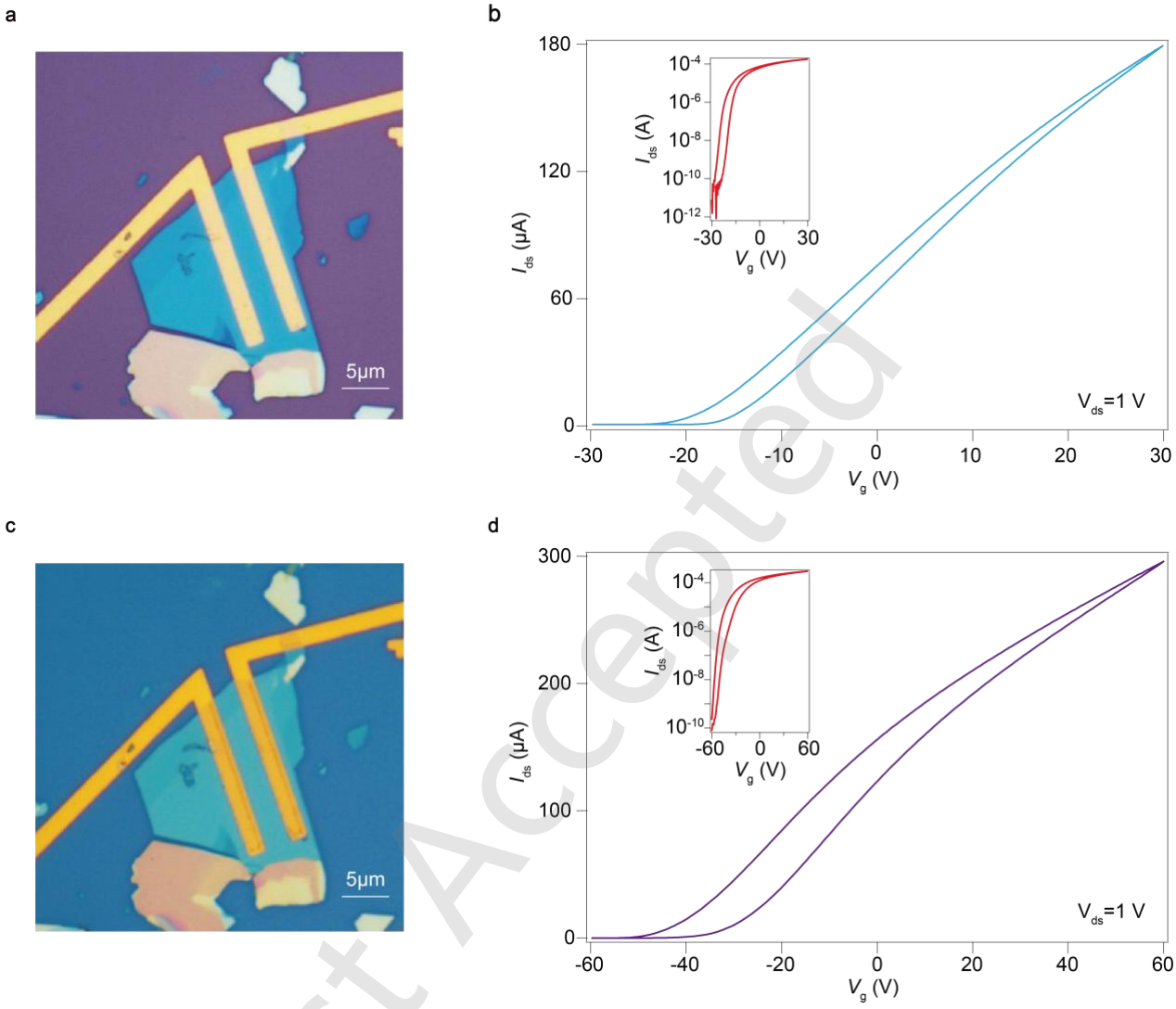
11. Electrical performance of bending operations.



S11. Electrical performance of bending operations. (a) Photograph of the flexural mold. (b) On-off ratio I_{on}/I_{off} and on current I_{ds} versus bend cycles up to 1000 cycles. (c)-(d) Transfer curves of the devices with different cycles at V_{ds}= 1 V.

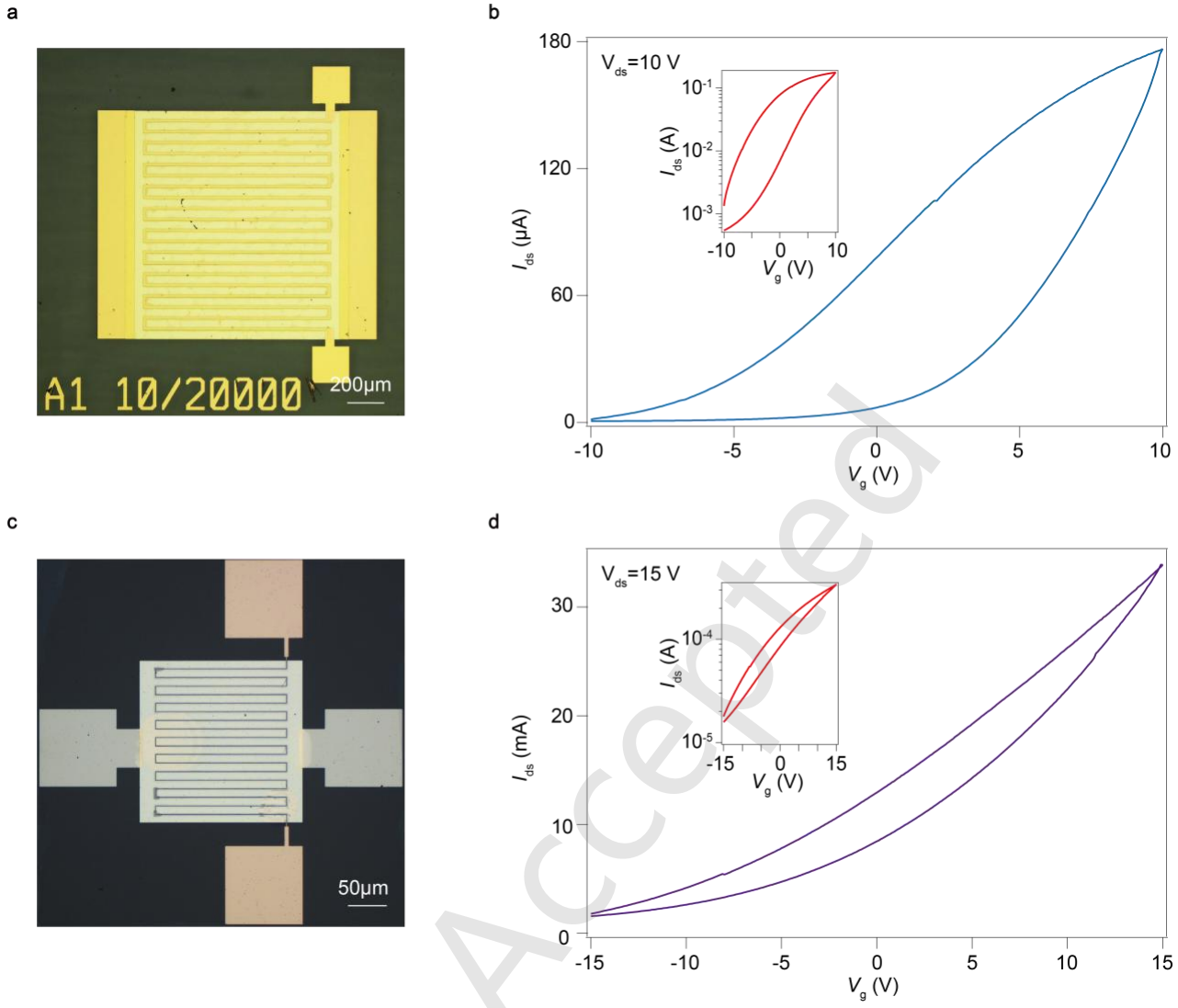
12. Doping Effect of HfO_2 Thin Films Deposited on MoS_2

The atomic layer deposition (ALD) of an HfO_2 dielectric layer on MoS_2 induces n-type doping, resulting in a moderate increase in the on-state current (I_{on}), a negative shift in the threshold voltage (V_{th}), and a reduction in the on/off ratio (I_{on}/I_{off}) of the transistor.



S12. Doping effect of HfO_2 thin films deposited on MoS_2. (a)and(c)are optical images of a device based on mechanically exfoliated few-layer MoS_2 before and after the deposition of the HfO_2 layer via ALD, respectively. (b) and (d) are transfer curves measured under V_{ds} =1 V.

13. Top-Gate Tunable Transistors Fabricated with Different Processes



S13. Top-gate tunable transistors fabricated with different processes. (a) and (c) Optical microscopy images of top-gate tunable transistors with interdigitated electrodes fabricated by photolithography and electron-beam lithography (EBL), respectively. (b) and (d) are transfer curves measured under V_{ds} = 10 V and 15 V with L = 10 μm and 1 μm, W = 20 mm and 3 mm, respectively.

Note 1. The curvature radius and surface strain of flexible devices based on MoS_2.

The arc length is defined as

$$L = R \cdot \theta \tag{1}$$

where R is curvature radius, and θ is central angle corresponding to L.
The chord length is defined as

$$C = 2R \cdot sin\frac{\theta}{2} \tag{2}$$

The curvature radius is given by

$$f(R) = 2R \cdot sin\frac{L}{2R} - C = 0 \tag{3}$$

In this paper, L = 12.5 mm and C = 11 mm, we can get the curvature radius is 7.2 mm and curvature of bend is 0.139 mm^{-1} based on $\kappa = {}^{1}/_{R}$.

The surface strain of the film can be determined based on the curvature radius, is defined as

$$\varepsilon = \frac{h}{2R} \tag{4}$$

where h is the thickness of the thin film. Considering the thicknesses of the substrate and dielectric layer, the strain at the surface is derived as ε = 0.35 %.