

Low-power monofilament-based semiconducting single-walled carbon nanotube solid-state electrolyte gated transistors for scalable woven electronics

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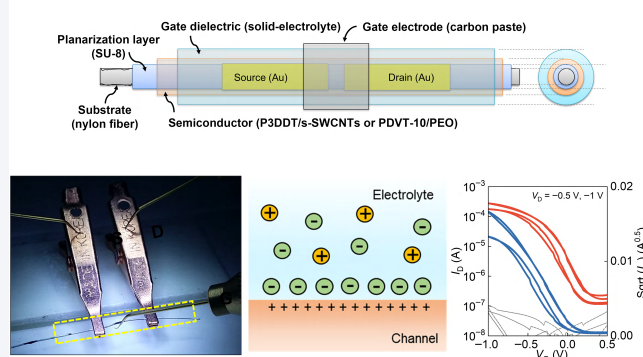
ABSTRACT: The development of high-performance and low-power active components directly integrated onto fibrous substrates is essential for the realization of next-generation wearable e-textiles. Here, we demonstrate high-performance monofilament fiber-based field-effect transistors (FETs) utilizing high-purity semiconducting single-walled carbon nanotubes (s-SWCNTs) and solid-state electrolyte gate dielectrics. To overcome the challenges of patterning on curvilinear fiber surfaces, we developed a fine-thread shadow mask technique, enabling the precise definition of micro-scale channel gaps without complex photolithography. The s-SWCNTs, isolated via a selective conjugated polymer wrapping method, exhibited robust ambipolar transport and high purity, as confirmed by ultraviolet–visible–near infrared (UV–Vis–NIR) and Raman spectroscopy. By integrating a [EMIM][BF₄]/PVDF-HFP ([EMIM][BF₄] = 1-ethyl-3-methylimidazolium tetrafluoroborate, PVDF = polyvinylidene fluoride, and HFP = hexafluoropropylene) solid-state electrolyte, the monofilament fiber-based FETs achieved ultra-low voltage operation (< 1 V) with high areal capacitance (> 1.05 μF·cm⁻²). The resulting fiber transistors exhibited a high hole mobility of 14.7 cm²·V⁻¹·s⁻¹ and a transconductance (g_m/W) of 0.3 S·m⁻¹. This synergistic approach combining textile-compatible fabrication and high-mobility nanomaterials provides a scalable pathway for energy-efficient and in-cloth signal processing and logic circuitry.

KEYWORDS: s-SWCNTs, solid-state electrolyte, fiber transistor, low voltage, wearable electronics

1 Introduction

Electronic textiles (e-textiles) represent a promising frontier for large-area and fiber-integrated functionality, encompassing physical sensors, energy harvesters, and optoelectronic displays [1–8]. Given that humans interact with fibrous materials such as garments, upholstery, and medical bandages for more than 60% of their daily

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lives, fibers serve as a natural building block for ubiquitous electronics [9–12]. Textiles offer exceptional mechanical advantages: low bending radius (less than 1 mm), high strain recovery, and excellent drape capability. By knitting or weaving functional fibers, one can achieve multi-directional stretchability (often exceeding 30% strain) while maintaining structural integrity [13–18]. However, the true realization of an “all-textile” electronic system remains elusive. This is primarily due to the difficulty of fabricating high-performance active components, particularly field-effect transistors (FETs), on curvilinear and high-roughness monofilament surfaces.

To date, several strategies have been explored to integrate transistors into fibers, including organic field-effect transistors (OFETs) and electrolyte-gated configurations [19–25]. However,

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conventional thin-film architectures often suffer from high operating voltages and complex and multi-step vacuum deposition processes that are difficult to scale on fibrous substrates [26–29]. While electrolyte-gated fiber transistors offer the advantage of high capacitance and low-voltage operation, they are frequently plagued by slow switching kinetics and electrochemical instability under ambient conditions [30–34]. Furthermore, the performance of existing fiber transistors often falls short of the requirements for high-fidelity signal processing, such as amplifying weak bio-signals (e.g., electrocardiogram (ECG) or electroencephalogram (EEG)) which typically have amplitudes in the millivolt range [35]. To overcome these limitations, it is imperative to employ active materials with high carrier mobility and mechanical robustness, such as single-walled carbon nanotubes (SWCNTs), while simultaneously simplifying the device architecture.

In this work, we demonstrate high-performance and low-power monofilament fiber-based FETs utilizing high-purity semiconducting SWCNTs (s-SWCNTs) for woven logic circuits. The primary challenge of leakage current caused by metallic SWCNTs was addressed via selective dispersion using conjugated polymer wrapping with regioregular poly(3-dodecylthiophene-2,5-diyl) (rr-P3DDT). This approach facilitates the isolation of high-purity s-SWCNTs, enabling balanced charge transport and high on/off current ratios, key requirements for complementary-like circuitry. By employing an innovative fine-thread shadow mask for the micro-patterning of source/drain electrodes directly onto the monofilament, we circumvented the need for complex photolithography on non-planar surfaces. Furthermore, by integrating a solid-state electrolyte gate dielectric, we achieved stable transistor operation at ultra-low voltage (< 1 V). This synergetic combination of solution-processed nanomaterials and textile-compatible fabrication provides a scalable pathway toward fully integrated and low-power in-cloth electronic systems, paving the way for next generation of hyper-connected wearable devices.

2 Experimental section

2.1 Materials

To sort high-purity s-SWCNTs, a polymer-assisted selective dispersion method was employed. The s-SWCNT dispersion was prepared by mixing 10 mg of rr-P3DDT (1-Material) and 10 mg of HiPco SWCNTs (NanoIntegris, diameter: 0.8–1.2 nm) in 10 mL of toluene (resulting in an initial concentration of $1 \text{ mg}\cdot\text{mL}^{-1}$ for both components). The mixture was ultrasonicated for 30 min at 25°C to ensure uniform dispersion. To isolate the semiconducting nanotubes, the suspension was subjected to high-speed centrifugation at 15,000 rpm for 60 min. The supernatant, containing the pure s-SWCNTs wrapped by P3DDT, was carefully collected for subsequent device fabrication. The concentrations of P3DDT and s-SWCNTs in the dispersion were determined using ultraviolet–visible–near infrared (UV–Vis–NIR) absorption spectroscopy based on the Beer–Lambert law. In order to determine the concentrations of s-SWCNTs in solution, the absorption cross-section was used for the E_{11} absorption peak of s-SWCNT. The total concentration of s-SWCNTs was approximately $4.88 \text{ }\mu\text{g}\cdot\text{mL}\cdot\text{cm}^{-1}$ for solution [36]. The concentration of P3HT was calculated from the maximum absorbance ($A \approx 1.0$) in the visible range (400–600 nm). Utilizing a mass extinction coefficient (α_{mass}) of $60 \text{ L}\cdot\text{g}^{-1}\cdot\text{cm}^{-1}$ for P3DDT and an optical path length of 1 cm, the

concentration was determined to be approximately $16.7 \text{ }\mu\text{g}\cdot\text{mL}^{-1}$. To prepare the semiconducting PDVT-10:PEO ink, PDVT-10 (1-Material) was dissolved in chloroform at a concentration of $10 \text{ mg}\cdot\text{mL}^{-1}$. PEO (Aldrich) was added to the solution at a weight ratio of 10 wt.% relative to the PDVT-10. The mixture was stirred thoroughly to ensure a homogeneous blend prior to the dip-coating process. The solid-state electrolyte ink was prepared by blending PVDF-HFP (Aldrich), acetone, and the ionic liquid 1-ethyl-3-methylimidazolium tetrafluoroborate ([EMIM][BF₄]) (Aldrich) in a weight ratio of 1:7:4. The mixture was stirred at room temperature until a transparent and homogeneous precursor solution was obtained, which was subsequently used for the formation of the high-capacitance electric double layer (EDL) dielectric.

2.2 Characterization

The optical and structural properties of the s-SWCNT dispersions and films were thoroughly characterized. UV–Vis–NIR absorption spectra were recorded using a Cary 5000 spectrophotometer (Agilent Technologies) to evaluate the purity and chirality of the P3DDT-wrapped SWCNTs. The structural integrity and sorting efficiency of the nanotubes were investigated via confocal Raman spectroscopy (NTEGRA Spectra, NT-MDT) employing excitation wavelengths of 532 and 633 nm. Furthermore, the surface morphology and network density of the solution-processed s-SWCNT films were examined using field-emission scanning electron microscopy (FE-SEM, S-4800, Hitachi).

2.3 Device fabrication and electrical characterization

For FETs and inverters on glass substrates, interdigitated source and drain electrodes ($W/L = 1000/10 \text{ }\mu\text{m}$, where W is the channel width and L is the channel length) were patterned on glass substrates using standard photolithography. A 5 nm Ni adhesion layer and a 15 nm Au layer were deposited via thermal evaporation, followed by a lift-off process. Before semiconducting layer deposition, the substrates were sequentially cleaned via ultrasonication in deionized water, isopropyl alcohol, and acetone, followed by UV/ozone treatment for 15 min and nitrogen drying. All fabrication steps were conducted within a nitrogen-filled glovebox. The s-SWCNT ink was spin-coated onto the substrates at 700 rpm. For the gate dielectric, either PMMA or the solid-state electrolyte ink was spin-coated onto the s-SWCNT film and baked at 60°C for 10 min. Finally, an 80 nm-thick aluminum gate electrode was thermally evaporated through a shadow mask to complete the top-gate/bottom-contact (TG/BC) configuration. Monofilament-based FETs were fabricated in a TG/BC configuration using commercial nylon fibers as substrates. To mitigate the intrinsic surface roughness of the monofilament, a surface planarization process was performed on commercial nylon fibers ($200 \text{ }\mu\text{m}$ in diameter). The fibers were first cleaned via ultrasonication in acetone and isopropyl alcohol (IPA) and dried in a convection oven. The layers were deposited onto the fiber substrates using a programmable dip-coater (EF-5100, E-Flex Co., Ltd., Republic of Korea). This equipment allows for precise control of the withdrawal speed, which is critical for ensuring a uniform coating thickness across the fiber's curved surface. For planarization, SU-8 2005 (Microchem) was applied using a dip-coating method at a constant pulling speed of $3 \text{ mm}\cdot\text{s}^{-1}$. The coated fibers underwent a soft-baking step at 95°C for 30 min, followed by UV exposure at a dosage of $1000 \text{ mJ}\cdot\text{cm}^{-2}$. After a post-exposure bake at 95°C for 30 min, the fibers were subjected to a final hard-

baking process at 150 °C for 60 min in a vacuum oven to ensure an atomically smooth and chemically stable interface for subsequent device integration. Micro-scale source and drain electrodes were defined using an innovative fine-thread shadow mask technique. A micro-filament thread ($\sim 20 \mu\text{m}$ in diameter) was precisely wrapped around the planarized fiber to serve as a physical mask during the thermal evaporation of gold (Au), resulting in a well-defined L governed by the thread diameter ($W/L = 1250/25 \mu\text{m}$). The active semiconducting layer (either s-SWCNT or PDVT-10:PEO blend) and the solid-state electrolyte dielectric ([EMIM][BF₄]/PVDF-HFP) were sequentially deposited via controlled dip-coating at a pulling speed of $10 \text{ mm}\cdot\text{s}^{-1}$. Following each coating step, the devices were dried at 50 °C overnight in a vacuum oven to ensure solvent removal and film stability. Finally, the gate electrode was integrated by either applying carbon paste or using a conducting fiber gate line within a textile frame to complete the functional in-cloth transistor. The current-voltage characteristics of the transistors and inverters were measured using a Keithley 4200 SCS in the same glovebox. The field-effect mobility was extracted in both the linear and saturation regimes using the standard gradual channel approximation [37]. All electrical parameters were extracted from forward gate-voltage sweeps unless otherwise stated.

3 Results and discussion

The architecture of the fiber-based FETs employs a TG/BC configuration on a cylindrical monofilament substrate (Fig. 1(a)). We utilized commercial nylon fibers with a diameter of $200 \mu\text{m}$ as the structural template; however, the intrinsic surface roughness of bare nylon poses a significant challenge for the deposition of uniform semiconducting networks and dielectric layers. To mitigate this, a surface planarization strategy was implemented using a dip-coating method with a photo-curable SU-8 resin. As confirmed by

the scanning electron microscopy (SEM) analysis in Fig. 1(b), the surface of the bare nylon fiber exhibits distinct longitudinal striations and irregular micro-defects inherent to the fiber extrusion process. In contrast, the SU-8 coating effectively planarizes these irregularities, resulting in a highly uniform and defect-free surface. This structural refinement provides an ideal and smooth interface for the subsequent layer-by-layer integration, ensuring better interfacial contact and device stability.

A critical bottleneck in fiber electronics is the formation of micro-scale electrode gaps on non-planar and cylindrical geometries. Conventional photolithography is often incompatible with the high curvature of monofilament fibers. To circumvent this, we developed an innovative fine-thread shadow mask technique (Fig. 1(c)). A micro-filament thread with a diameter of $\sim 20 \mu\text{m}$ was precisely wrapped around the planarized nylon fiber to serve as a physical shadow mask during the thermal evaporation of gold (Au) source/drain electrodes. The SEM images in Fig. 1(c) demonstrate the successful deposition of a uniform Au electrode pair with a well-defined micro-gap. Notably, L of the resulting FETs is governed solely by the diameter of the masking thread, allowing straightforward scaling of device dimensions and enabling short-channel devices without complex cleanroom processes. Following the electrode patterning, the semiconducting channel was formed through a controlled dip-coating of the pre-sorted and high-purity s-SWCNT solution, ensuring a percolation network that conforms to the fiber's curvature (Fig. 1(d)). The detailed device fabrication processes and experimental procedures are provided in Section 2.

To realize high-performance and low-power electronic circuits, the elimination of metallic SWCNT species, which induce leakage currents and degrade the on/off ratio, is critical. We employed a selective dispersion strategy based on the π - π interaction between P3DDT and the graphene lattice of SWCNTs (Fig. 2(a)) [38, 39]. The preparation followed a procedure similar to that reported previously [38, 39]. The P3DDT-wrapped s-SWCNTs solution was

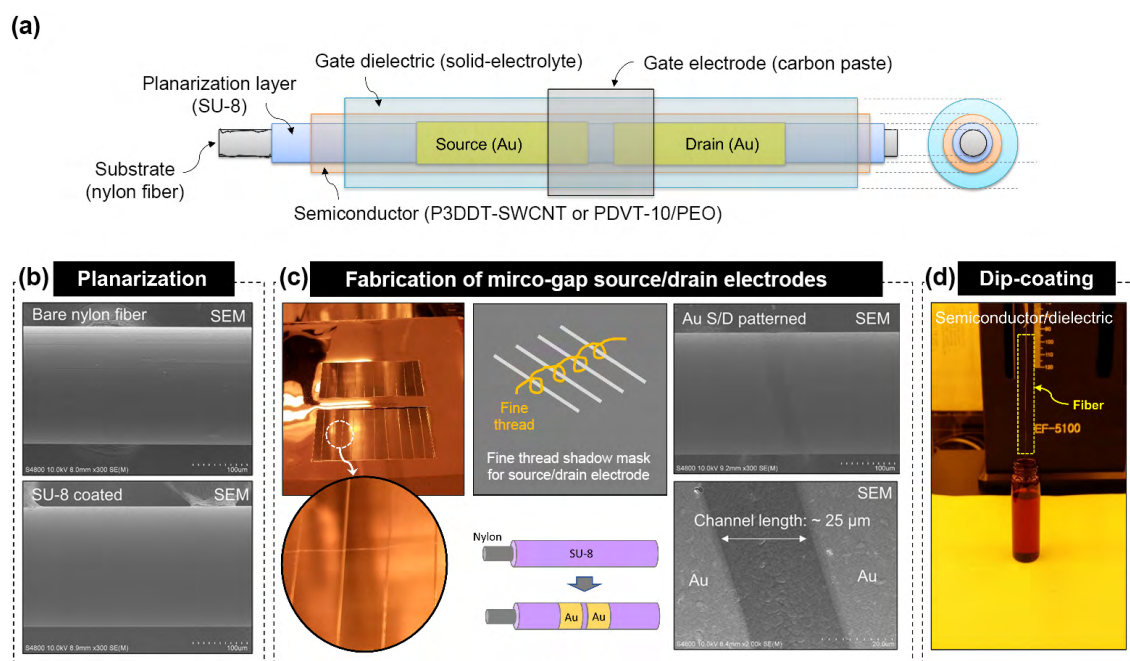


Figure 1 Device architecture and fabrication of solid-state electrolyte-gated fiber FETs using s-SWCNTs or PDVT-10/PEO as the semiconductor. (a) Schematic of the device layout on a monofilament fiber substrate. (b) SEM micrographs of the pristine nylon fiber surface and the planarized surface after SU-8 photo-curable polymer coating. (c) Fabrication of micro-gap source/drain electrodes using a fine-thread shadow mask. SEM images show the resulting Au-patterned fiber. (d) Formation of the active semiconductor channel and electrolyte dielectric layers by a sequential dip-coating process.

spin-coated on a glass substrate or applied to monofilament fibers via dip-coating. Surface morphology and network formation of the s-SWCNTs were investigated via SEM. The as-spun P3DDT-SWCNT composite film exhibited a uniform and smooth surface, where the SWCNTs were fully embedded within the polymer matrix (Fig. 2(b)). To verify the underlying percolation network of the s-SWCNTs, the wrapping polymer was selectively removed via thermal annealing at 500 °C for SEM analysis. It should be noted, however, that in the final device fabrication, the P3DDT matrix was intentionally retained. As a polythiophene-based conjugated polymer, P3DDT functions as a functional semiconducting matrix that complements the s-SWCNTs. Specifically, its high π - π stacking-induced mobility, reversible redox stability under electrolyte gating, and hydrophobic resistance to aqueous environments make the P3DDT/s-SWCNT composite an ideal active layer for high-performance electrolyte-gated transistors. The resulting SEM image (Fig. 2(c)) revealed a dense and interconnected network of s-SWCNTs, ensuring efficient charge transport pathways required for high-mobility fiber-based transistors. The electronic structure and purity of the sorted s-SWCNTs were further validated using UV-Vis-NIR and Raman spectroscopy. The UV-Vis-NIR absorption spectrum (Fig. 2(d)) displays distinct peaks corresponding to the S_{11} ($\lambda = 1000$ –1550 nm) and S_{22} ($\lambda = 600$ –900 nm) optical transitions of semiconducting species, with specific chirality indices (e.g., (7, 5), (8, 4), and (8, 7)) clearly identified. The suppression of the metallic M_{11} ($\lambda = 450$ –600 nm) transitions confirms the high selectivity of the P3DDT-wrapping process [39–41]. Resonant Raman spectroscopy ($\lambda = 633$ nm) confirmed the sorting efficiency, particularly in the radial breathing mode (RBM) region (Fig. 2(e)). In this region, the pristine HiPco SWCNTs exhibited prominent metallic peaks (180–220 cm^{-1}); however, these peaks were completely eliminated in the sorted samples, leaving only the semiconducting signatures. This is further corroborated by the G-band analysis (Fig. 2(f)). After normalization to the G+ peak (~ 1580 cm^{-1}), the sorted SWCNTs showed a dramatic reduction in the Breit-Wigner-Fano (BWF)

line shape, a characteristic feature of metallic carbon nanotubes (CNTs), at approximately 1550 cm^{-1} [41, 42]. The s-SWCNTs sorted by P3DDT exhibit additional vibrational signatures between 1300 and 1500 cm^{-1} that are absent in the unsorted HiPco SWCNTs. These bands are assigned to the thiophene ring vibrations of the P3DDT matrix, including the C=C symmetric stretching at 1450 cm^{-1} and C–C skeletal stretching at 1380 cm^{-1} [42]. The presence of these peaks provides spectroscopic evidence of the intimate interaction between the P3DDT chains and the SWCNT surface, which is crucial for selective semiconducting sorting. These spectroscopic results collectively demonstrate that the P3DDT-assisted sorting yields high-purity s-SWCNTs, providing an ideal active material for low-power woven electronic circuits.

To evaluate the electrical performance, we first characterized the FETs on a standard glass substrate to establish a baseline performance, followed by the evaluation of monofilament-based FETs. As illustrated in Figs. 3(a) and 3(b), the s-SWCNT FETs fabricated on a glass substrate with a poly(methyl methacrylate) (PMMA) gate dielectric exhibit pronounced ambipolar transport behavior. Subsequently, the device architecture was transitioned to the fiber platform, as detailed in Fig. 4. At drain voltages (V_D) of ± 1 , ± 3 , and ± 5 V, the devices show symmetric current modulation for both hole and electron injection. We extracted appreciably high field-effect mobilities (μ) of 1.37 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for holes and 0.87 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for electrons, with relatively low threshold voltages (V_{Th}) of -1.2 and 20.7 V, respectively. Intrinsic ambipolarity is a hallmark of high-purity s-SWCNTs, with quasi-transport of both carriers through the delocalized π -electron system [43, 44]. While many CNT-based transistors are restricted to p-type unipolar characteristics due to extrinsic factors, such as oxygen-induced doping or electron trapping at the dielectric interface, our devices maintain robust n-channel performance [45, 46]. This suggests that the P3DDT-SWCNT composite architecture effectively passivates the CNT surface, reducing the density of electron trap sites that typically hinder electron transport in ambient conditions thus

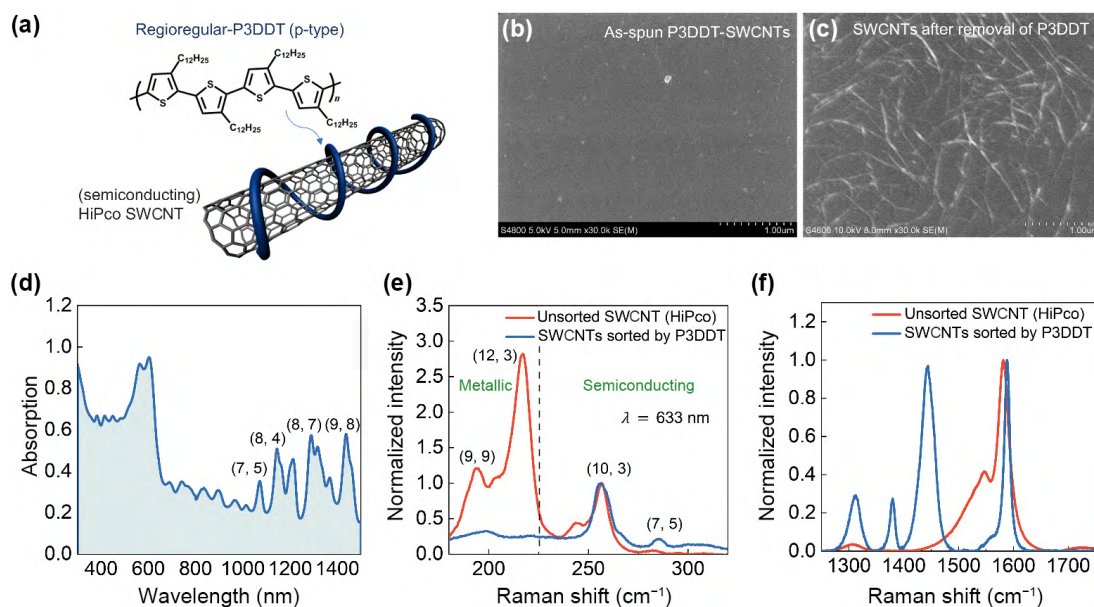


Figure 2 Morphology and spectroscopic properties of sorted s-SWCNTs. (a) Schematic of conjugated polymer-wrapped s-SWCNTs. (b) and (c) SEM micrographs of solution-deposited s-SWCNT networks in (b) the as-spun state and (c) after P3DDT removal by thermal annealing. (d) UV-Vis-NIR absorption spectra of the sorted s-SWCNTs. (e) Raman spectra of unsorted and P3DDT-sorted SWCNTs. (f) G-mode for using excitation wavelength 633 nm.

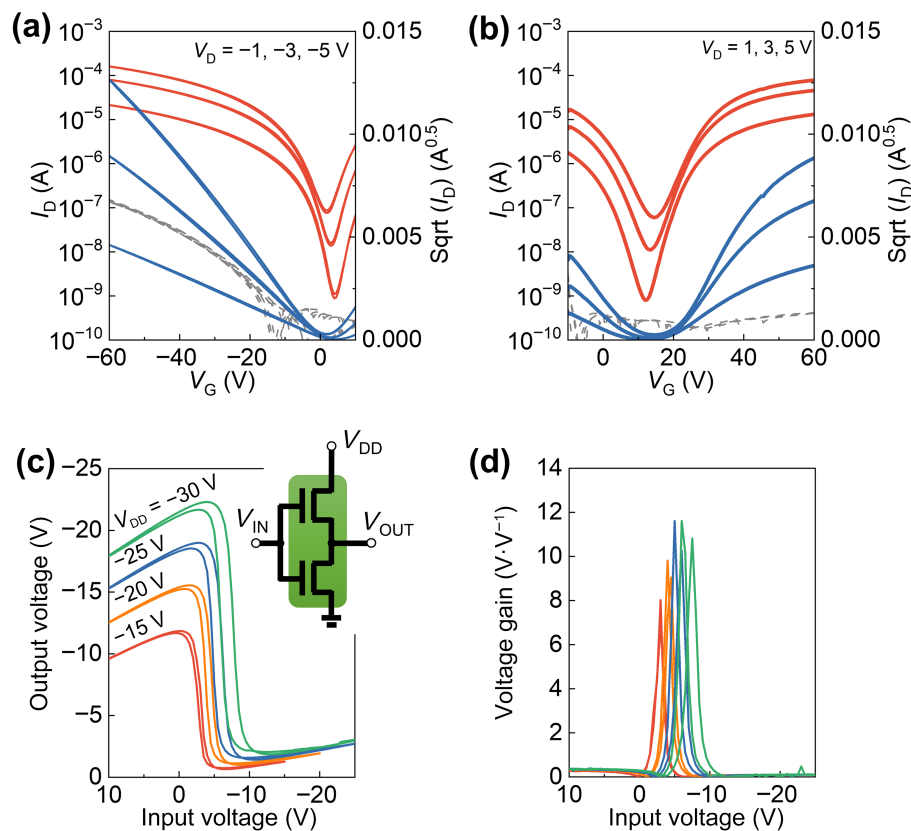


Figure 3 Electrical performance and logic applications of ambipolar s-SWCNT FETs with PMMA gate dielectrics on glass substrates. ((a) and (b)) Transfer characteristics showing (a) p-channel operation at $V_D = -1, -3$, and -5 V and (b) n-channel operation at $V_D = 1, 3$, and 5 V. ((c) and (d)) Complementary-like inverter performances based on ambipolar s-SWCNT FETs, showing (c) V_{TC} and (d) corresponding voltage gains at various supply biases $V_{DD} = -15, -20, -25$, and -30 V).

enabling n-type transport. Although the active layer consists of a polymer-nanotube composite, the primary charge transport is governed by the percolating s-SWCNT network, as the pristine P3DDT matrix contributes negligibly to overall carrier mobility.

Our s-SWCNT devices exhibit robust ambipolar transport. Bottom-contact gold electrodes typically have a relatively low work function (~ 4.7 eV) due to the push-back effect of electron tails on the metal surface by adsorbed hydrocarbons [47–49]. This enables the injection of both charge carriers from the same metal electrode into the frontier molecular orbitals of the SWCNT. Moreover, these charge carriers could be injected from the relatively larger top-surface contact area of the metal electrode compared with coplanar devices. The contact resistance (R_c) was obtained using the Y-function method, with the detailed extraction procedure provided in Fig. S1 and Table S1 in the Electronic Supplementary Material (ESM). The s-SWCNTs exhibit low contact resistance for both electrons and holes, enabling efficient charge injection into the active channel (Table S1 in the ESM). A hydroxyl-free polymer gate dielectric, PMMA, on active semiconductor also significantly contributes to the ambipolar charge transport behavior. Many reports indicate that intrinsic n-type behavior can be suppressed by electron trapping, e.g., due to hydroxyl groups on the dielectric surface [50, 51]. A top-gate configuration is preferable to preserve the intrinsic properties of semiconductors, including organic materials and carbon nanotubes. Hydroxyl-free polymer dielectric enables transport of both charge carriers without electron trapping. Moreover, self-encapsulated dielectric layer and top-gate electrode passivate the device and maintain stability under air or light exposure. Notably, P3DDT ensures stable ambipolarity by serving

as both an active transport medium and a protective barrier. The electronic interaction between P3DDT and s-SWCNTs facilitates efficient charge transfer, while the polymer matrix simultaneously shields the nanotubes from oxygen and moisture, thereby maintaining robust n-channel characteristics in ambient conditions [52].

The fabricated s-SWCNT FETs demonstrate robust ambipolar transport, characterized by well-balanced hole and electron injection, which is a fundamental requirement for high-efficiency logic applications. As shown in Figs. 3(a) and 3(b), the devices exhibit high on-currents and sharp switching characteristics in both p-channel and n-channel regimes. Utilizing this balanced performance, we implemented a complementary-like inverter, which offers a significant advantage over traditional complementary metal-oxide-semiconductor (CMOS) technology. While standard CMOS circuits necessitate distinct p-type and n-type semiconductor patterning, increasing process complexity and cost, our ambipolar-based architecture enables the fabrication of both pull-up and pull-down components using a single active material and a simplified processing route. The voltage transfer curves (V_{TC}) in Fig. 3(c) show nearly ideal rail-to-rail output voltage swings with a sharp transition. Although a slight Z-shaped characteristic is observed, attributed to the off-state leakage current inherent in ambipolar transistors, the signal inversion remains robust. The corresponding voltage gain (~ 12 V·V⁻¹), as detailed in Fig. 3(d), is sufficient to ensure signal integrity and reliable switching in integrated digital/analog systems. This performance underscores the potential of our s-SWCNT platform as a scalable and cost-effective solution for future printed and flexible microprocessors.

However, it is noted that most wearable devices including electronic skin and in-textile devices require very low voltage operation [53, 54]. Electric power has to be supplied by external battery or integrated energy harvesting systems, such as textile photovoltaics and triboelectric nano-generators [55, 56]. Thus, textile or fiber transistors must operate at low power to be compatible with wearable energy constraints. Figure 4(a) illustrates

a schematic comparison between a conventional dielectric-gated FET and an electrolyte-gated FET, highlighting the EDL formation at the interface. Also shown are the chemical structures of the PMMA dielectric and the solid-state electrolyte components. The electrolyte consists of PVDF-HFP with the ionic liquid [EMIM][BF₄] used in this work. In a standard FET architecture, the organic semiconductor channel is capacitively coupled to the gate

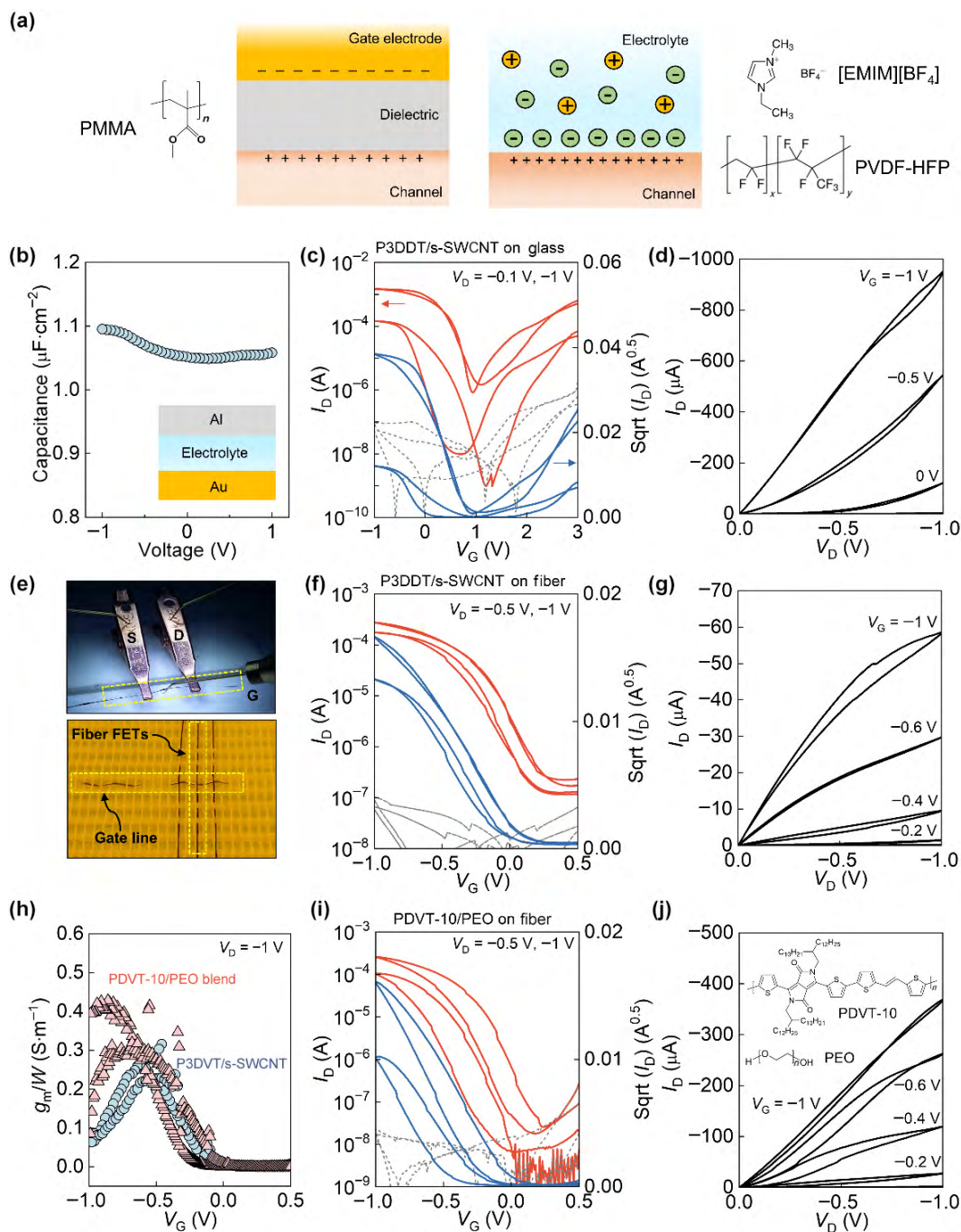


Figure 4 Electrical characterization of electrolyte-gated FETs on glass and monofilament substrates. (a) Schematic of a conventional dielectric-gated FET and an electrolyte-gated FET, highlighting EDL formation. Chemical structures of the PMMA dielectric and components of the solid-state electrolyte ([EMIM][BF₄] and PVDF-HFP). (b) Areal capacitance of the solid-state electrolyte as a function of applied voltage measured at 10 Hz. (c) Representative transfer and (d) output characteristics of s-SWCNT FETs on a glass substrate using the solid-state electrolyte. (e) Optical micrographs showing monofilament-based s-SWCNT FETs and gate lines incorporated into a textile frame. (f) Representative transfer and (g) output characteristics of the low-power monofilament fiber s-SWCNT FETs. (h) Normalized transconductance (g_m/W) of monofilament fiber FETs using P3DDT/s-SWCNT or PDVT-10/PEO blends. ((i) and (j)) Transfer and output characteristics of monofilament fiber PDVT-10/PEO blend FETs.

electrode via a solid-state dielectric layer, where the induced charge density (Q) follows $Q = CV$. Since the geometric capacitance (C) is inversely proportional to the dielectric thickness, conventional devices often necessitate high operating voltages to achieve sufficient carrier accumulation. Conversely, electrolyte-gated FETs enable ultra-low-voltage operation (< 1 V) through the formation of an EDL at the electrolyte–channel interface. This mechanism serves as an extreme scaling limit for FETs, as the effective separation between the ionic and electronic charge sheets is reduced to the molecular dimensions of an ionic radius[33].

We employed solid-state electrolytes to enable low-voltage operation of s-SWCNT in-textile transistors. The s-SWCNT transistor fibers were dip-coated in a PVDF-HFP/[EMIM][BF₄] electrolyte solution, followed by drying in a vacuum oven at 50 °C overnight. As shown in Fig. 4(b), the polymer electrolyte thin film exhibits a high dielectric capacitance of more than 1.05 $\mu\text{F}\cdot\text{cm}^{-2}$, measured by voltage sweep from +1 to −1 V at 10 Hz. Figures 4(c) and 4(d) show the transfer and output characteristics of electrolyte-gated s-SWCNT transistors fabricated on planar glass substrates with Au bottom-contact electrodes ($W/L = 600/10$ μm). These results show that electrolyte-gated s-SWCNTs also exhibit intrinsic ambipolar transport with high channel currents in both p- and n-channel regimes. The extracted electron and hole mobilities were 18.5 and 55.6 $\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$, with corresponding threshold voltages of 1.80 and 0.75 V, respectively. Moreover, these devices were operated under very low voltages (< 1 V) with a high on/off current ratio of 10^5 . This ambipolar behavior arises from efficient transport of both anions and cations in the solid-phase polymer electrolyte, combined with the intrinsic ambipolar transport of the s-SWCNT composite active layer.

Next, to demonstrate the practical utility of our solid-phase polymer electrolyte in wearable electronics, we fabricated in-textile fiber transistors using a dip-coating process. Following the deposition of Au source/drain electrodes on a monofilament fiber substrate ($W/L = 1250/25$ μm), the active semiconductor layer and the polymer electrolyte were sequentially deposited via a controlled dip-coating method at a pulling speed of 10 $\text{mm}\cdot\text{s}^{-1}$. Electrical measurements were conducted either through direct probe contact or via a conducting fiber gate line integrated into a textile frame, as illustrated in Fig. 4(e). Consistent with the planar benchmarks, the fiber transistors exhibited excellent operation at ultra-low voltages

(< 1 V). While electron transport was largely suppressed, likely due to the trapping of mobile electrons by ambient moisture and oxygen during air-processing, the p-channel characteristics remained robust. The P3DDT/s-SWCNT fiber transistors demonstrated high charge carrier mobilities and significant channel currents, with a measured hole mobility of ~ 14.7 $\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$ and a near-zero threshold voltage of 0.07 V (Figs. 4(f) and 4(g)). Furthermore, analysis was conducted via the Y-function method, and detailed derivations are provided in the ESM, confirming relatively low R_c for hole injection, highlighting the efficient charge transfer at the semiconductor–metal interface. To explore the versatility of this platform, we also fabricated fiber transistors using a PDVT-10:PEO blend as the active layer (full chemical name: poly[2,5-bis(2-decyltetradecyl) pyrrolo[3,4-c] pyrrole-1,4(2H,5H)-dione-alt-5,5"-di(thiophen-2-yl)-2,2"-(E)-2-(2-(thiophen-2-yl) vinyl) thiophene]). The incorporation of PEO into PDVT-10 promotes volumetric ion gating by enhancing the ion-solvating properties of the layer, thereby significantly improving the performance of the electrolyte-gated transistors. These devices similarly exhibited reliable low-voltage operation, yielding a hole mobility of ~ 10.4 $\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$ and a threshold voltage of 0.38 V, as derived from the transfer and output characteristics shown in Figs. 4(i) and 4(j), respectively. A comparative analysis of the transconductance (g_m/W) revealed maximum values of 0.3 $\text{S}\cdot\text{m}^{-1}$ for P3DDT/s-SWCNT and 0.4 $\text{S}\cdot\text{m}^{-1}$ for PDVT-10/PEO (Fig. 4(h)), emphasizing the high switching efficiency of our electrolyte-gated architecture. The detailed electrical parameters of all measured transistors based on glass and fiber substrates, including μ , V_{Th} , and on/off current ratios, are summarized in Table 1. These results indicate that when integrated with stable interconnects, these fiber transistors serve as a robust foundation for in-cloth wearable signal processing and switching devices capable of maintaining stable operation under external strain.

4 Conclusions

In summary, we successfully developed a scalable and robust platform for high-performance and low-power electrolyte-gated FETs directly integrated onto monofilament fibers. By implementing a surface planarization strategy and an innovative fine-thread shadow mask technique, we overcame the geometric limitations of conventional lithography, enabling precise micro-gap

Table 1 Key electrical parameters and contact resistance of FETs in this study

Devices (dielectric/substrate)	W/L (μm)	Mobility ^a ($\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$)	V_{Th} (V)	On/off ratio	R_c^b ($\text{k}\Omega\cdot\text{cm}$)
HiPco SWCNT-P3DDT (PMMA/glass)	1000/10	$\mu_{\text{FET,h}}: 1.37$ $\mu_{\text{FET,e}}: 0.88$	$V_{\text{Th,h}}: -1.2$ $V_{\text{Th,e}}: 20.7$	$\sim 10^4$	5.2 8.3
HiPco SWCNT-P3DDT (electrolyte/glass)	600/10	$\mu_{\text{FET,h}}: 55.6$ $\mu_{\text{FET,e}}: 18.5$	$V_{\text{Th,h}}: 0.75$ $V_{\text{Th,e}}: 1.80$	$\sim 10^5$	0.2 1.9
HiPco SWCNT-P3DDT (electrolyte/fiber)	1250/25	$\mu_{\text{FET,h}}: 14.3$ $\mu_{\text{FET,e}}: \text{NA}$	$V_{\text{Th,h}}: 0.07$ $V_{\text{Th,e}}: \text{NA}$	$\sim 10^4$	~ 5.0 NA
PDVT-10/PEO (electrolyte/fiber)	1250/25	$\mu_{\text{FET,h}}: 10.5$ $\mu_{\text{FET,e}}: \text{NA}$	$V_{\text{Th,h}}: 0.38$ $V_{\text{Th,e}}: \text{NA}$	$\sim 10^5$	~ 3.0 NA

^aLinear mobility at $V_D = \pm 1$ (PMMA/glass), ± 0.1 (electrolyte/glass), and ± 0.5 V (electrolyte/ fiber).

^bContact resistance was obtained by Y-function method in the linear region. “NA” indicates not applicable.

electrodes on cylindrical substrates. High-purity s-SWCNT networks, facilitated by P3DDT wrapping, ensured efficient charge transport. In parallel, the solid-state electrolyte enabled stable transistor operation at voltages below 1 V, a critical requirement for battery-powered wearable electronics. The resulting fiber FETs demonstrated not only high carrier mobility but also significant transconductance. Furthermore, the compatibility of this platform with various active materials, such as PDVT-10/PEO blends, underscores its versatility. Our findings suggest that these fiber-based transistors can serve as the fundamental building blocks for fully integrated, all-textile electronic systems capable of high-fidelity signal amplification and logic operations in next-generation wearable and distributed electronic environments.

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Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

D. K.: Supervision, conceptualization, methodology, investigation, data curation, formal analysis, writing. W. B.: Methodology, writing. J. M. L.: Experimental support. A. D. K.: Methodology, investigation. C. L. T.: Validation, review. H. B. S.: Validation, review. Z. H. Y.: Resources, technical support. K.-J. B.: Conceptualization, supervision, methodology, writing. All the authors have approved the final manuscript.

Use of AI statement

None.

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