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Research Article

Sub-fJ programming in ferroelectric reconfigurable homojunctions for photovoltaic in-sensor computing

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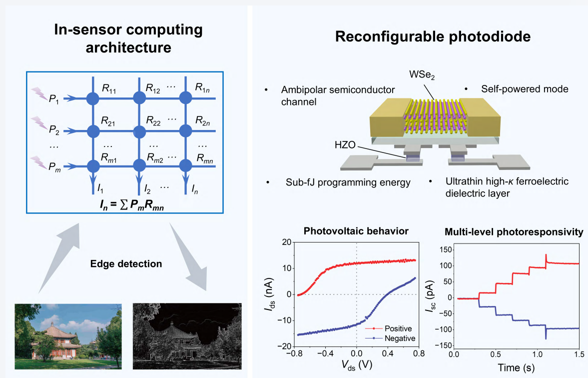

ABSTRACT: Conventional vision systems encounter data bottlenecks and high-power consumption in emerging applications due to the separation of sensing and computation. In-sensor computing architectures address this limitation by integrating reconfigurable, self-powered photodiodes at the pixel level to enable *in-situ* visual preprocessing. However, existing devices are constrained by high programming energy, poor weight retention, or complementary metal-oxide-semiconductor (CMOS) incompatibility, hindering simultaneous optimization of power efficiency, speed, stability, and integrability. Here, we demonstrate a self-powered reconfigurable photodiode based on a bipolar WSe_2 channel and a sub-20-nm ferroelectric $Hf_xZr_{1-x}O_2$ (HZO) layer. The device employs a split-gate architecture to generate polarity-switchable short-circuit photocurrent under photovoltaic mode, achieving ultralow programming energy (< 1 fJ), a switching speed of 50 μs, and weight retention exceeding 100 s. When deployed as a physical convolution kernel, the device performs in-sensor matrix-vector multiplication on incident light. In simulated edge-detection tasks, it achieves a remarkably low normalized mean squared error (~ 3.2×10^{-4}), producing edge maps nearly indistinguishable from ideal software results. This work establishes an energy-efficient and self-driven hardware platform that unifies sensing, memory, and computation, realizing a practical framework for in-sensor computing.

KEYWORDS: ferroelectricity, reconfigurable photodiode, in-sensor computing, $Hf_xZr_{1-x}O_2$ (HZO), WSe_2

1 Introduction

Conventional vision systems, in which CMOS image sensors are separated from digital processing units, struggle to simultaneously achieve real-time performance and energy efficiency in emerging applications such as high-frame-rate imaging, low-latency processing, and adaptive perception [1–5].

Recently, in-sensor computing architectures have provided a transformative paradigm to mitigate these bottlenecks by embedding neural network processing units within the pixel array [6–9]. This device-level integration of sensing and computation reduces hardware complexity, lowers energy consumption, and enables ultra-low-latency responses [4, 10–13]. Realizing this paradigm requires co-design of hardware and neural network algorithms, allowing each pixel to dynamically reconfigure its photoresponse according to the computational tasks [14–16]. At the device level, such programmability facilitates the direct

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implementation of neuron- or synapse-like preprocessing operations, including weighted summation and inhibitory responses [17–20].

However, most existing optoelectronic devices are limited to unidirectional photocurrent generation (typically positive) and require external power supplies, making it challenging to simultaneously achieve low power consumption and reconfigurability [11, 21–23]. Reconfigurable photodiodes offer a promising route to overcome this limitation by enabling dynamic control of photoresponse polarity in photovoltaic mode, thereby supporting inherent self-powered operation and neuromorphic functionalities [20, 24–26]. Such photovoltaic reconfigurability has been demonstrated using diverse physical mechanisms. For instance, reconfigurable Schottky barriers enable photocurrent polarity switching by modulating the metal-semiconductor interfacial barrier height with an applied programming voltage [24, 26]. In ferroelectric systems, polarity-switchable photoresponse arises from bulk photovoltaic effects driven by reversible polarization [25, 27, 28]. Non-volatile control of rectification polarity has also been achieved in reconfigurable p-n junctions based on ambipolar two-dimensional (2D) semiconductors (e.g., WSe_2 and $MoTe_2$) through integration of split-gate electrodes with ferroelectric dielectrics [20, 29].

Despite their promise, the first two strategies are generally hampered by high programming voltages, slow write speeds, and insufficient non-volatility, collectively resulting in excessive programming energy consumption and poor weight retention [24, 25, 30]. In contrast, the third approach offers both excellent non-volatility and low programming energy; however, it relies on ferroelectric gate dielectrics such as $CuInP_2S_6$ (CIPS) or poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) [20, 29, 31]. These materials suffer from weak remnant polarization and low dielectric permittivity, which limit thickness scalability and compromise device reliability. Moreover, their poor compatibility with standard CMOS technology further impedes their applicability in scalable integration into machine vision systems.

Notably, hafnium zirconium oxide ($Hf_xZr_{1-x}O_2$ (HZO)), a ferroelectric material rooted in advanced CMOS technology nodes, has demonstrated exceptional performance in recent years [32–34]. It exhibits not only a high dielectric constant ($\kappa > 20$) [35, 36] and robust ferroelectric polarization ($2P_r > 50$ μC/cm^2) [37–39], but also stable ferroelectricity down to ~ 1 nm thickness [33]. Moreover, recent advances in low-temperature HZO growth have enabled compatibility with standard back-end-of-line (BEOL) CMOS integration processes [40–42]. Despite these advantages, reconfigurable photodiodes based on HZO have rarely been reported, and their potential for in-sensor computing remains largely unexplored.

In this work, we report a reconfigurable photodiode based on a bipolar WSe_2 channel, in which a sub-20-nm ferroelectric HZO layer defines a reconfigurable in-plane p-n junction. Integration of this HZO film with a split-gate architecture enables polarity-switchable photocurrent generation under zero external bias, achieving low programming energy below 1 fJ, a switching speed of 50 μs, and weight retention exceeding 100 s. This self-powered device intrinsically supports visual information preprocessing, such as matrix-vector multiplication (MVM) of incident optical signals, without requiring external power or analog-to-digital conversion. Furthermore, when employed as a convolutional kernel in simulated edge-detection tasks, the device achieves a low normalized mean squared error (NMSE) of approximately 3.2×10^{-4} at its optimal weight state, yielding edge maps nearly indistinguishable from ideal software predictions. This work establishes a CMOS-compatible device paradigm toward next-generation energy-efficient, reconfigurable intelligent vision systems.

2 Experimental

2.1 Device fabrication

The fabrication of the device began with the sputtering and patterning of a 30 nm TiN bottom electrode on a Si/SiO_2 substrate. Next, a ~ 19 nm HZO film was deposited by atomic layer deposition (ALD) at 250 °C. A second TiN layer, also 30 nm thick, was sputtered and patterned, followed by rapid thermal annealing at 550 °C for 60 s to crystallize the underlying HZO film. Subsequently, a 10 nm Al_2O_3 insulating layer was deposited via ALD at 150 °C. Photolithography and inductively coupled plasma (ICP) etching were applied to selectively etch through the Al_2O_3 and HZO layers, exposing the underlying TiN electrodes. Few-layer WSe_2 flakes, exfoliated from bulk crystals, were transferred onto the patterned substrate. Finally, source and drain electrodes were defined using electron-beam lithography (EBL), deposition of a 100 nm Ti/Au bilayer, and a standard lift-off process.

2.2 Device characterization

All electrical and optoelectronic characterizations were carried out on a Signatone probe station integrated with an Agilent B1500A semiconductor parameter analyzer, under monochromatic laser illumination at 650 nm to evaluate the device's photoresponse.

2.3 Material characterization

Raman spectra of mechanically exfoliated WSe_2 flakes were acquired using a Horiba Jobin Yvon LabRAM HR800 system with a 532 nm laser as the excitation source. Optical absorption spectra were measured with an Excipolar Trion spectrometer illuminated by a white light source. For structural and compositional analysis, cross-sectional transmission electron microscopy (TEM) samples of WSe_2 devices were prepared by focused ion beam (FIB) etching using a dual-beam FEI Helios NanoLab 600i system. High-resolution TEM (HRTEM) imaging was subsequently performed on an *ex situ* Talos F200e microscope (Thermo Fisher Scientific) operated at 200 kV, while energy-dispersive X-ray spectroscopy (EDS) elemental mapping was acquired using an integrated Oxford X-MaxN 80 detector. Surface morphology was characterized by atomic force microscopy (AFM) on a Bruker Dimension Icon platform, operating in PeakForce Tapping mode with a ScanAsyst-Air probe.

2.4 Edge detection

The simulation employed a neural network based on the Tiny and Efficient Edge Detector (TEED) architecture [43], whose backbone consists of three blocks. The output of each block was processed by a dedicated USNet branch to generate a multi-scale edge prediction, and these results were fused by the dual-fusion (Dfuse) module to produce the final edge map.

For hardware mapping, the pre-trained weights of the early convolutional layers in the backbone were directly programmed into a reconfigurable photodiode array. The photoresponse of each pixel was modeled by Eq. (1)

$$I_n = \sum_{i=1}^{m} P_m \cdot R_{mn} \quad (1)$$

where P_m is the illumination power incident on the m^{th} pixel, R_{mn} is the corresponding pre-trained convolutional weight of the mn^{th} device. This analog-domain operation performs convolution *in situ*, eliminating the need for analog-to-digital conversion or off-sensor data transfer.

Simulations were conducted using natural scene images sourced from the Peking University Photo Gallery, resized to a resolution of 900 × 550 pixels, under six distinct device weight state (states I–VI). All outputs were spatially aligned with the ideal software inference results and quantitatively evaluated using the NMSE, as given in Eq. (2)

$$\text{NMSE} = \frac{\sum_{i,j}(I(i,j) - I_{\text{gold}}(i,j))^2}{\sum_{i,j}(I_{\text{gold}}(i,j))^2} \quad (2)$$

where I denotes the edge map generated by the simulated photodiode array, I_{gold} is the corresponding ground-truth output from ideal software inference. Difference maps ($|I - I_{\text{gold}}|$) were further provided to assess structural fidelity visually.

3 Results and discussion

3.1 In-sensor computing architecture based on a reconfigurable photodiode

In the pursuit of enhanced computational efficiency and reduced energy consumption, in-sensor computing architectures represent a significant advancement by integrating optical sensing, weight storage, and analog computation within a single integrated platform, as shown in Fig. 1(a). When a trained array of such devices is illuminated by incident light, the resulting photocurrents can be directly read out to perform MVM operations in the analog domain. This approach not only simplifies circuit design but also enables on-chip preprocessing of optical signals, thereby supporting low-power operation and significantly accelerating vision tasks such as edge detection.

Central to this framework is the reconfigurable photodiode. As shown in Fig. 1(b), the device features a split-gate architecture, with each gate integrating an independent HZO ferroelectric capacitor. These capacitors enable non-volatile electrostatic doping, which locally modulates the carrier polarity in different regions of the ambipolar semiconductor WSe_2, thereby forming reconfigurable in-plane homojunctions. Depending on the ferroelectric polarization states of the two HZO capacitors, the junction can be dynamically programmed into p-i-p, p-i-n, n-i-p, or n-i-n configuration. Notably, when a p-i-n or n-i-p junctions is established, the photovoltaic effect generates a short-circuit current (I_{SC}) and an open-circuit voltage (V_{OC}) with opposite polarities. The short-circuit current follows the relationship $I_{\text{SC}} = P \cdot R$, where P denotes the incident optical power and R is the photoresponsivity, a tunable parameter determined by the non-volatile ferroelectric polarization state. This programmable photoresponsivity effectively emulates synaptic weights in artificial neural networks, enabling highly energy-efficient and accelerated in-sensor computing.

3.2 Structural and material characterization of the reconfigurable photodiode

We systematically characterized the key components of the reconfigurable photodiode to elucidate its underlying structural and material properties. Figure 2(a) illustrates the AFM characterization of the device channel, which is divided into three sections by two split gates and reveals a continuous and uniform surface. Regions I

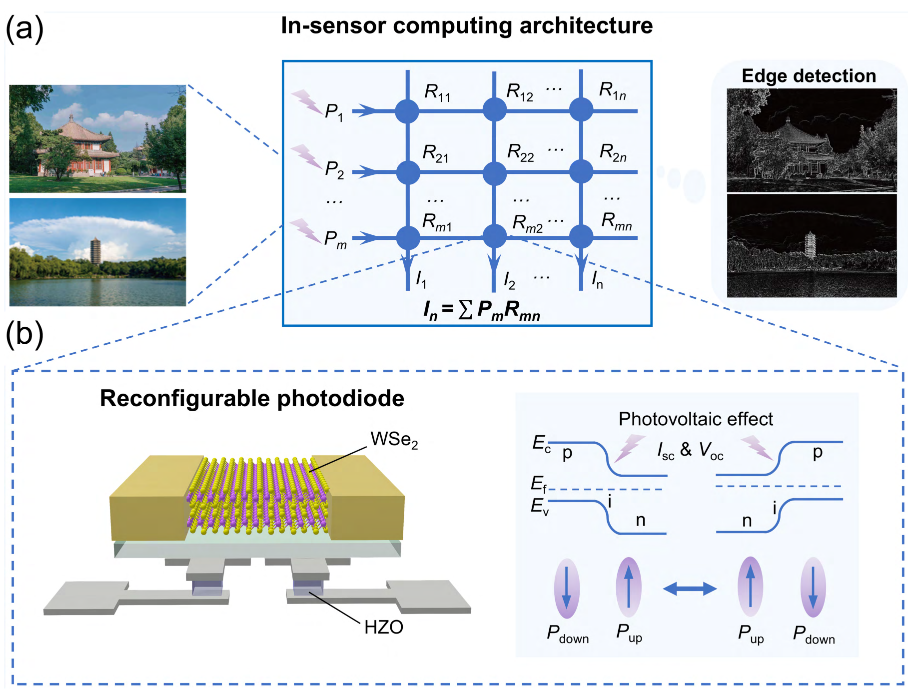

Figure 1 Demonstration of in-sensor computing using a reconfigurable photodiode. (a) Schematic illustration of the in-sensor computing architecture. (b) Device structure of the reconfigurable photodiode in a split-gate configuration with integrated HZO ferroelectric capacitors. Ferroelectric polarization enables non-volatile modulation of carrier polarity in the WSe_2 channel, thereby dynamically forming reconfigurable in-plane homojunctions.

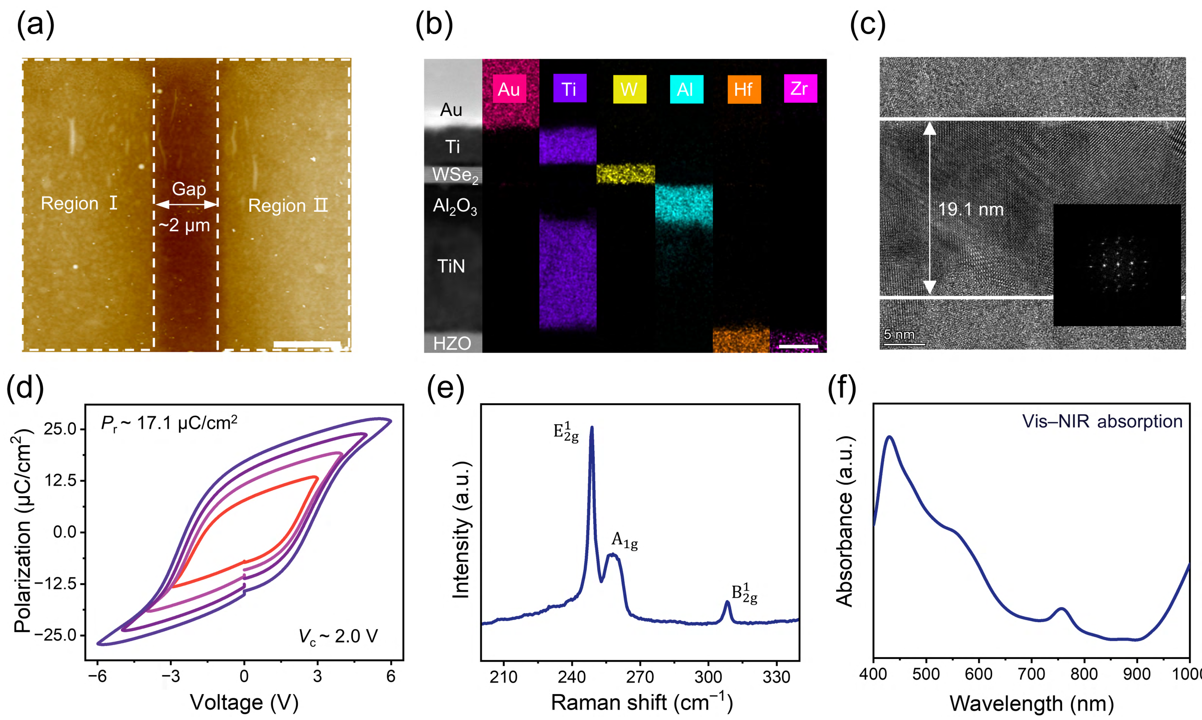

Figure 2 Structural and material characterization of the WSe_2 channel and HZO ferroelectric layer. (a) Surface morphology of WSe_2 channel. Scale bar, 2 μm. (b) Cross-sectional TEM image and corresponding EDS mapping of the device. Scale bar, 10 nm. (c) HRTEM image of the polycrystalline HZO layer. (d) *P–V* hysteresis loop of the HZO film, exhibiting low leakage and strong remanent polarization. (e) Raman spectrum of WSe_2. (f) Optical absorption spectrum of WSe_2.

and II are utilized for electrostatic doping to form reconfigurable in-plane homojunctions, with a gap of approximately 2 μm between them. A magnified view of the channel edge shows that the thickness of the WSe_2 flake is approximately 4.8 nm (Fig. S1 in the Electronic Supplementary Material (ESM)). Subsequently, a TEM sample was prepared using FIB, and EDS mapping of the source/drain regions confirmed a well-defined layered structure with homogeneous elemental distribution, as shown in Fig. 2(b). Furthermore, HRTEM imaging revealed the polycrystalline nature of the HZO ferroelectric layer, indicating its excellent crystalline quality, as displayed in Fig. 2(c).

The ferroelectric properties of HZO are crucial for the device's functionality. Figure 2(d) presents the polarization–voltage (*P–V*) loop of the HZO film (with a thickness of ~ 19.1 nm), measured by a ferroelectric analyzer. The film maintains a low leakage current at a voltage of 6 V, with a coercive voltage (V_c) of about 2 V and a remanent polarization (P_r) as high as 17.1 μC/cm², fully demonstrating its excellent ferroelectric characteristics. Notably, in contrast to recently explored ferroelectric systems such as CIPS and P(VDF-TrFE), HZO achieves sub-20-nm thickness while maintaining high remanent polarization, low leakage current, and compatibility with standard CMOS fabrication processes.

Meanwhile, the crystal quality and optical properties of the WSe_2 channel itself are equally critical. In Fig. 2(e), the Raman spectrum exhibits sharp, well-defined characteristic peaks, indicating a high-quality single-crystalline structure consistent with the layered features observed by HRTEM (Fig. S2 in the ESM)). Moreover, the absorption spectrum reveals strong optical absorption across a broad wavelength range from 400 to 1000 nm, spanning the visible to near-infrared regions (Fig. 2(f)). Combined with the programmable optoelectronic behavior and the integrated sensing-storage-computing architecture, this broad spectral response endows the device with significant potential for machine vision applications.

3.3 Operating mechanism and programming behavior of ambipolar ferroelectric field-effect transistors (FeFET)

The reconfigurable photodiode can be electrically modeled as two ambipolar FeFETs connected in series. Consequently, its fundamental device characteristics can be effectively interpreted through the behavior of a single-gate FeFET. As shown in Fig. 3(a), the device adopts a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) configuration comprising TiN, HZO, Al_2O_3, and WSe_2. The bottom TiN layer functions as the control gate and, in conjunction with the HZO layer and an intermediate TiN floating gate, forms a ferroelectric capacitor. The Al_2O_3 layer acts as an insulating buffer, providing a high-quality insulator/semiconductor interface that enables stable modulation of channel conductance.

A key advantage of this architecture is its capability to enable tunable voltage distribution between the ferroelectric and insulating layers. The bottom metal-ferroelectric-metal (MFM) stack and the top metal-insulator-semiconductor (MIS) stack function as two series-connected capacitors. By adjusting the area ratio between the MFM and MIS regions (A_{Fe}/A_{De}), the voltage drop across the ferroelectric layer can be precisely controlled. As shown in Fig. 3(b), devices with a smaller A_{Fe}/A_{De} display wider memory windows in their transfer characteristics, indicating enhanced memory performance. Specifically, when the A_{Fe}/A_{De} is decreased from 1.5 to 0.2, the memory window broadens significantly (Fig. S3 in the ESM), attributed to the amplified voltage across the ferroelectric layer that promotes efficient polarization switching (Note S1 in the ESM). Moreover, the device demonstrates excellent cycle-to-cycle (C2C) stability, with a coefficient of variation (C_v) as low as 1.8% over 22 cycles, as shown in Fig. 3(c) and Fig. S4 in the ESM.

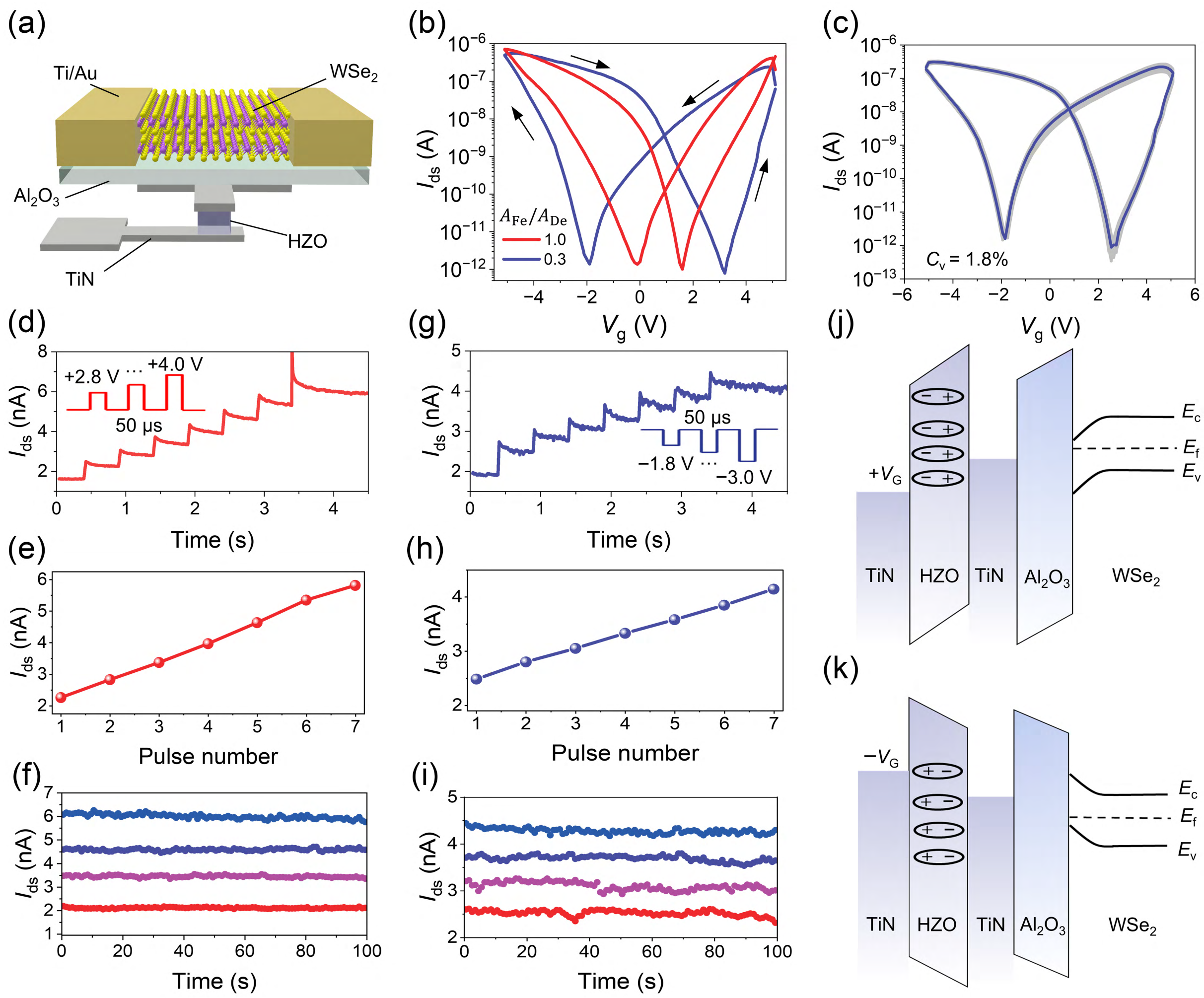

Figure 3 Electrical characterization of the ambipolar FeFET. (a) Schematic of the ambipolar FeFET with an MFMIS structure. (b) Transfer curves of the FeFET with varying A_{Fe}/A_{De} ratios. (c) C2C variability of transfer curves over multiple programming cycles. (d) Stable stepwise increase in channel current under positive voltage pulse programming. (e) Linear conductance tuning achieved using amplitude-increasing positive voltage pulses. (f) Non-volatile retention of programmed conductance states for over 100 s following positive-pulse weight updates. (g) Stable stepwise increase in channel current under negative voltage pulse programming. (h) Linear conductance tuning achieved using amplitude-increasing negative voltage pulses. (i) Non-volatile retention of programmed conductance states for over 100 s following negative-pulse weight updates. (j) and (k) Energy band diagrams illustrating band bending in WSe_2 under opposite polarization states.

The tunable conductance states of the FeFET enable programmable photoresponsivity in the reconfigurable photodiode, forming the basis for its application in MVM. As depicted in Fig. 3(d), the channel current exhibits stable, stepwise increments when subjected to positive voltage pulses with a 50 μs pulse width. To address the inherently non-uniform switching dynamics of ferroelectric polarization under fixed-amplitude pulses, an amplitude-incremental pulse scheme was implemented to achieve a more linear conductance update, as illustrated in Fig. 3(e). Owing to the robust non-volatility of ferroelectric polarization, the programmed conductance states are maintained for over 100 s with high distinguishability (Fig. 3(f)).

Benefiting from the ambipolar transport characteristics of WSe_2, the conductance continued to increase steadily under negative voltage pulses (Figs. 3(g)–3(i)), exhibiting bidirectional programming symmetry with respect to positive voltage pulses. Notably, both long-term potentiation (LTP) and long-term depression (LTD) could be achieved using either polarity of voltage pulse. For instance, after LTP was programmed with positive voltage pulses, the device could be reset to its initial conductance state by applying negative voltage pulses. Subsequently, LTP could be re-established using pulses of either polarity (Fig. S5 in the ESM). This flexibility in implementing LTP and LTD with both positive and negative voltages provides the physical foundation for reconfigurable device operation.

The operational mechanism of the FeFET is elucidated through its energy band diagram in Figs. 3(j) and 3(k). As WSe_2 acts as a non-degenerate semiconductor, the field-induced carrier modulation is primarily localized within the band-bending region near the dielectric interface. Under a positive gate bias, the ferroelectric polarization in the HZO layer aligns toward the semiconductor channel. The resulting bound polarization charges are capacitively coupled through the TiN floating gate, modulating the Al_2O_3/WSe_2 interface and inducing electron accumulation. This leads to downward band bending of the WSe_2 conduction band, bringing the conduction band edge closer to the Fermi level and thereby enhancing the electron concentration, which drives the device into a high-conductance state. Conversely, under a negative gate bias, the ferroelectric polarization reverses direction toward the gate electrode. This induces upward band bending in WSe_2, shifting the conduction band edge away from the Fermi level and depleting electrons in the channel. Owing to the ambipolar nature of WSe_2, hole accumulation concurrently increases, eventually enabling a high-conductance state dominated by p-type carriers. Critically, the non-volatility of ferroelectric polarization ensures that both the polarization orientation and the corresponding conductance state are retained after removal of the gate voltage, thereby enabling data memory.

3.4 Photovoltaic response and weight updating of reconfigurable photodiode

Leveraging the unique characteristics of the ambipolar FeFET, we further investigate its optoelectronic response in the configuration of a reconfigurable photodiode. Figure 4(a) presents an optical micrograph of the device, in which the channel dimensions are significantly larger than the central gap (~ 2 μm). This geometry ensures that the local carrier polarity in regions I and II predominantly governs the overall electrical behavior, while the electrically neutral central gap exerts negligible influence on charge transport.

This operational mode is enabled by the non-volatile remanent polarization of the HZO layer, which sustains carrier modulation without a continuous external gate voltage. As illustrated in Fig. 4(b), by applying programming pulses with a width of 50 μs to the split gates (V_{G1} and V_{G2}), the channel can be reversibly configured into four distinct in-plane homojunction states: p-i-n, n-i-p, p-i-p, and n-i-n. Specifically, the p-i-n state is configured by setting V_{G1} = −3.5 V and V_{G2} = 3.5 V, while the n-i-p state is established by using V_{G1} = 3.5 V and V_{G2} = −3.5 V. For the homopolar configurations, the p-i-p and n-i-n states are achieved by applying $V_{G1} = V_{G2}$ = −3.5 V and $V_{G1} = V_{G2}$ = 3.5 V, respectively.

When configured as a p-i-n or n-i-p junction, the device

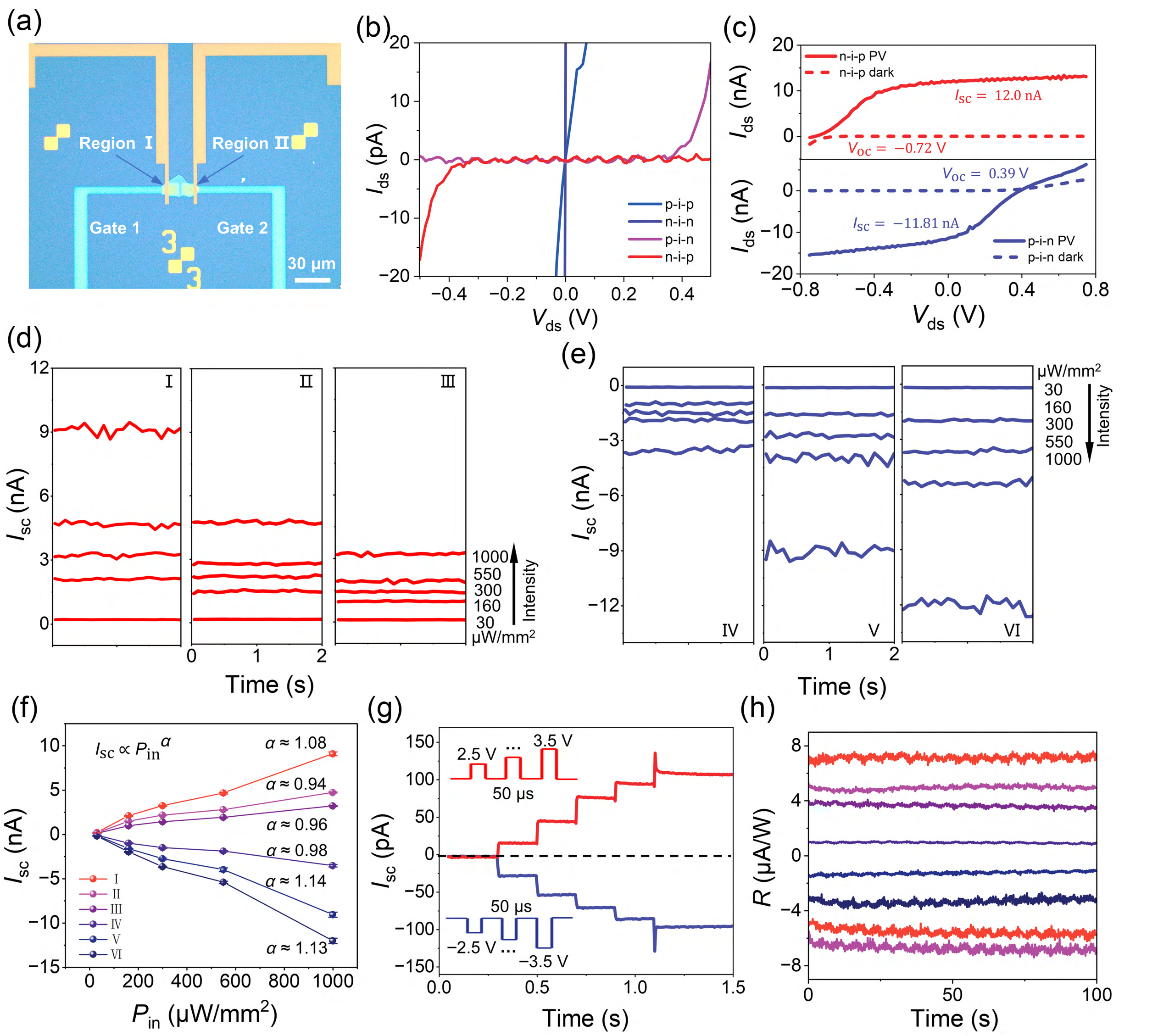

Figure 4 Tunable photovoltaic response and in-sensor weight updating in a reconfigurable photodiode. (a) Optical image of the reconfigurable photodiode. (b) Four programmable in-plane homojunction (p-i-p, p-i-n, n-i-n, and n-i-p) achieved by tuning the ferroelectric polarization state. (c) Photovoltaic effect under 650 nm illumination at a power density of 1000 μW/mm², generating both photocurrent and photovoltage at p-i-n or n-i-p junctions. (d) and (e) Bidirectional photoresponse: positive short-circuit photocurrent states (I–III) from an n-i-p junction and negative states (IV–VI) from a p-i-n junction under varying optical power densities (30–1000 μW/mm²). (f) Short-circuit photocurrent versus power density across multiple programmed photoresponsivity states. (g) Stable stepwise short-circuit photocurrent tuning via positive or negative programming pulses (V_P). (h) Retention of programmed photoresponsivity states over time in the reconfigurable photodiode.

exhibited diode-like rectifying behavior, with a lateral built-in electric field established across the junction. Under 650 nm illumination, this field created an energy barrier that efficiently separated photogenerated electron-hole pairs, thereby generating both photocurrent and photovoltage (i.e., the photovoltaic effect, PV), as shown in Fig. 4(c). Furthermore, owing to the intrinsic broadband absorption of WSe_2, the device achieves reconfigurable positive and negative photocurrents across both the visible and near-infrared (NIR) regions (Fig. S6 in the ESM)), thereby highlighting its potential for multispectral recognition and processing tasks.

The device enables dynamic non-volatile tuning of its optoelectronic response through ferroelectric polarization. By modulating the junction barrier height in the p-i-n or n-i-p configuration, the photoresponsivity (R) can be programmed, allowing tunable photovoltaic behavior (Fig. S7 in the ESM). For instance, in Fig. 4(d), adjusting the barrier height of the n-i-p junction produced multiple positive photoresponse states (states I–III), enabling the generation of a positive short-circuit photocurrent (I_{SC}) under increasing optical power density (P_{in}) from 30 to 1000 μW/mm^2. Conversely, tuning the barrier height of the p-i-n junction produces multiple negative photoresponse states (states IV–VI), resulting in negative I_{SC} under the same illumination range, as shown in Fig. 4(e). This bidirectional switching of photocurrent polarity, between positive and negative, is uncommon in conventional optoelectronic devices. Moreover, the short-circuit current exhibited a nearly linear dependence on incident optical power density, following the relationship $I_{SC} \propto P_{in}{}^{\alpha}$. In this model, the exponent α serves as the linear factor, where a value closer to 1 signifies a more ideal linear response. As illustrated in Fig. 4(f), the extracted α values for states I to VI are 1.08, 0.94, 0.96, 0.98, 1.14, and 1.13, respectively. These results, with the α value consistently remaining near 1, confirm the excellent linearity of the device across all programmed states, which is essential for ensuring high-precision analog MVM operations.

Additionally, owing to the intrinsic characteristics of ferroelectric polarization switching, the optical responsivity was updated using an amplitude-incremental programming scheme. As shown in Fig. 4(g), the device exhibits stable stepwise photocurrents under optimized programming parameters, where the programming voltage V_P is defined as the gate pulse amplitude with a 50 μs width, with the specific configuration set as $V_P = V_{G1} = -V_{G2}$. The low programming voltage and rapid switching speed achieved in this work not only facilitate ultra-low power consumption but also significantly enhance device reliability, demonstrating competitive performance relative to reported reconfigurable optoelectronic devices (Table S1 in the ESM).

This synergy enables highly flexible and reliable tuning of the photoresponsivity, along with excellent retention of the programmed states for over 100 s (Fig. 4(h)). Due to the self-powered nature of the photovoltaic effect, the device consumed negligible energy during optical sensing and inference computation. Moreover, HZO, which combines a high dielectric constant with robust ferroelectricity, enables an ultra-low leakage current below 10 pA (Fig. S8 in the ESM). This resulted in a programming energy as low as 7.5×10^{-16} J, among the lowest reported to date for reconfigurable optoelectronic devices (Table S1 in the ESM). These results underscore the device's potential to serve to as an in-sensor convolution kernel for optoelectronic preprocessing in neural networks, enabling ultra-low energy consumption while performing computation directly at the sensor edge.

To further evaluate the scalability of the proposed architecture, a preliminary assessment of array-level integration is conducted by fabrication dozens of devices on a ~ 1 cm × 1 cm HZO substrate (Fig. S9 in the ESM). Although these scaling efforts are constrained by interfacial impediments and the stochastic variability inherent in commercial polycrystalline WSe_2 films, the mature CMOS compatibility of the HZO gate stack establishes a robust framework for future integration. We anticipate that as high-quality 2D material synthesis and damage-free integration protocols continue to evolve, this architecture will effectively facilitate the realization of high-density optoelectronic systems.

3.5 Reconfigurable photodiodes for in-sensor edge detection

To investigate the suitability of reconfigurable photodiodes within an in-sensor computing framework, we assessed their performance on an edge detection task through simulation. As illustrated in Fig. 5(a), an input image was processed using the TEED architecture [43], which consists of three cascaded backbone blocks. Each block implements two basic processing units of the form: $\zeta = [\text{conv1} + \text{Smish} + \text{conv2} + \text{Smish}]$, where conv1/conv2 are convolutional layers and Smish denotes a smooth, differentiable activation function used in the TEED architecture to improve edge sensitivity. Following each backbone block, a dedicated USNet module produces a coarse edge prediction, and multi-scale feature representations are fused via skip connections across hierarchical levels. These intermediate outputs are subsequently aggregated by the Dfuse module, which adaptively combines cross-scale edge cues to yield a high-fidelity edge map.

In this work, the reconfigurable photodiodes were integrated into the early convolutional layers of the first backbone block, where they functioned as physical convolution kernels. Leveraging their intrinsic photocurrent response: $I_{SC} = P \cdot R$, the photodiode array performed optical convolution optical directly on the incoming light, enabling real-time edge feature extraction at the sensing front-end.

Six distinct weight states (states I–VI), extracted from the experimentally measured photoresponsivity levels in Fig. 4(f), were used to program the reconfigurable photodiodes as convolutional kernels. The resulting edge maps were compared against those from an ideal software prediction (Figs. 5(b)–5(d)), and the quantitative evaluation was performed using the NMSE (see Experimental section). Among the tested states, state IV yielded the poorest performance, exhibiting the highest NMSE and the residual difference is relatively noticeable (Fig. 5(c)). In contrast, state II achieves the best agreement, with the lowest NMSE and an edge map nearly indistinguishable from the ideal software predictions, the residual difference is almost imperceptible (Fig. 5(d)).

Unlike conventional digital systems that separate sensing and computation, the proposed array performs analog MVM to emulate convolution kernels at the sensor edge, enabling efficient extraction of salient edge features. With appropriate weight programming, its performance approaches that of an ideal digital implementation, while its self-powered operation supports low-power, high-efficiency in-sensor computing.

4 Conclusions

In summary, we have demonstrated a reconfigurable, self-powered photodiode based on a bipolar WSe_2 channel and a sub-20-nm

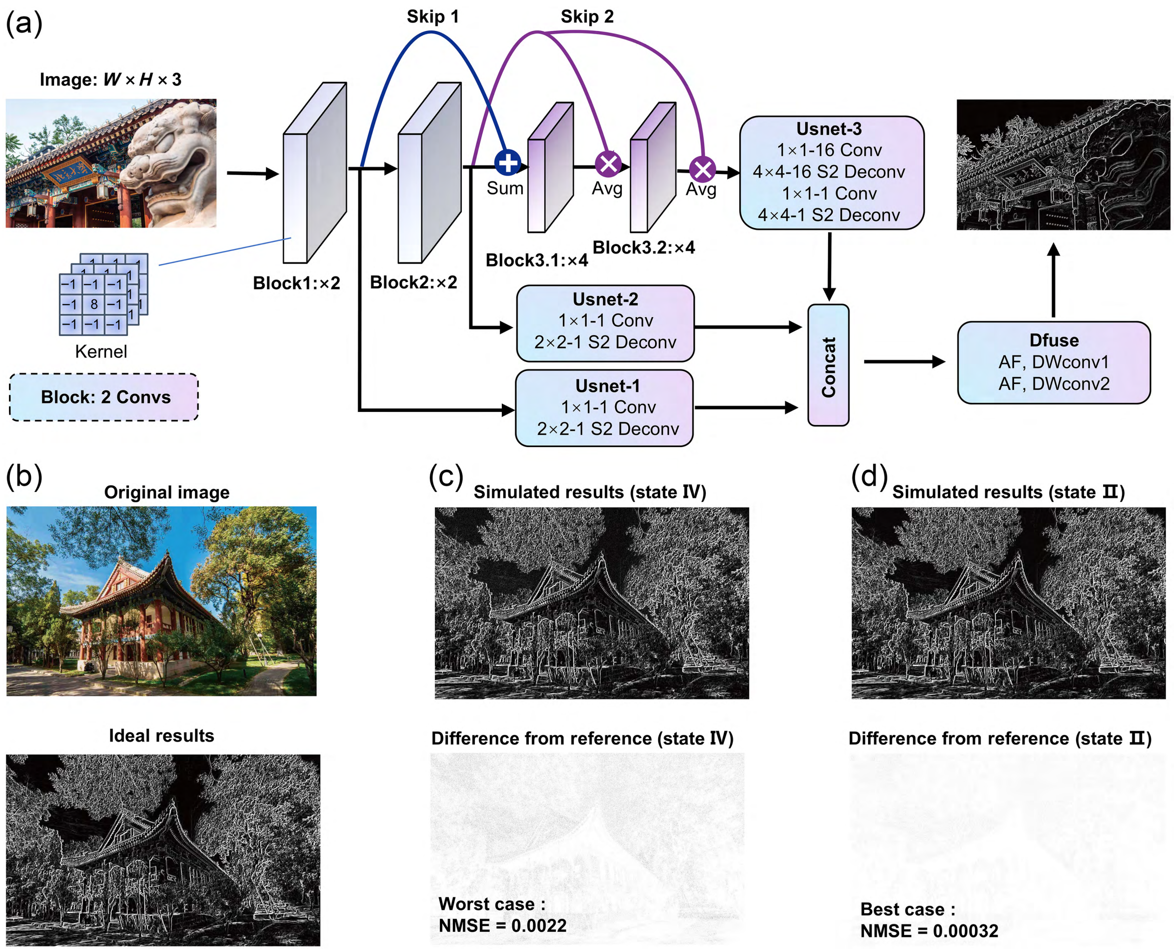

Figure 5 Simulation of edge detection using reconfigurable photodiodes as physical convolution kernels. (a) TEED architecture with photodiodes integrated into the first backbone block. (b) Reference edge map generated by the ideal software implementation. (c) Simulated output using a suboptimal weight state (state IV), the difference map is relatively noticeable. (d) Simulated output using the optimal weight state (state II), the difference map is almost imperceptible.

ferroelectric HZO layer. The device utilizes a split-gate architecture that enables polarity-switchable short-circuit photocurrent in photovoltaic mode, achieving ultralow programming energy (< 1 fJ), fast switching (50 μs), and stable weight retention (> 100 s). When operated as a physical convolution kernel for in-sensor visual preprocessing, the device directly performs analog MVM on incident light. In simulated edge-detection tasks, it yielded an NMSE of ~ 3.2×10^{-4}, producing edge maps nearly indistinguishable from ideal software predictions. Although currently limited to single-pixel devices fabricated from exfoliated WSe_2, this work lays the foundation for future programmable, large-scale optoelectronic arrays capable of online learning and real-time edge vision.

Electronic Supplementary Material: Supplementary material (further details on AFM/TEM characterization of the reconfigurable photodiode, electrical and programming tests of the ambipolar FeFET, photovoltaic test of the reconfigurable photodiode, comparison and discussion of representative reconfigurable photodiodes) is available in the online version of this article at https://doi.org/10.26599/NR.2026.94908610.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

J. R. W.: Experimental design, data curation, project administration, writing manuscript. K. Q. L: Experimental design, formal analysis. J. W. Z.: Investigation, data curation. Y. L. Z.: Investigation, data curation. P. J. T.: Neural network simulation. C. Z. Z.: Experimental design, data curation. W. W. W.: Experimental design, data curation. X. S: Experimental design, data curation. D. W. H.: Project administration, formal analysis. Y. S. W.: Project administration, funding acquisition. Y. Y. T.: Neural network simulation, review manuscript. Y. C. Y.: Supervision, funding acquisition, review manuscript. X. X. Z.: Supervision, funding acquisition, review manuscript. All the authors have approved the final manuscript.

Use of AI statement

None.

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