Nano Research

Open Access

Review Article

The contacts between two-dimensional materials and metal electrodes

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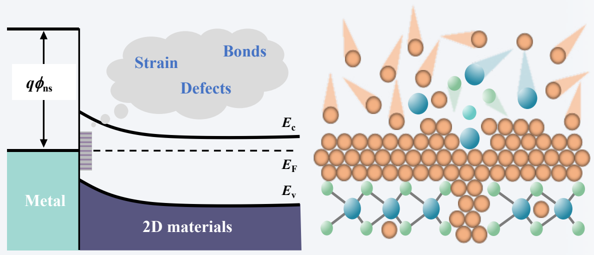
Cite this article: *Nano Research*, **2026**, *19*, 94908584. https://doi.org/10.26599/NR.2026.94908584

ABSTRACT: The advent of two-dimensional (2D) materials has ushered in a new era for electronic and optoelectronic devices. However, their atomic-scale thickness presents a fundamental contact interface challenge: the formation of a Schottky barrier at the 2D material–metal contact interface, which often leads to Schottky barrier and high contact resistance (R_C). While detrimental for conventional transistor scaling, this inherent Schottky barrier is also a critical functional element, actively harnessed in devices like photodetectors. This duality defines the central theme of contact interface engineering in 2D electronics. This review comprehensively examines recent advances in understanding and engineering these critical interfaces. We first elucidate the core physical principles governing contact formation, including Fermi level (E_F) pinning (FLP), charge transfer, and Schottky barrier modulation. We then distinguish strategic pathways for engineering contacts: routes toward ultralow-resistance Ohmic contacts (van der Waals (vdW) integration, interfacial doping, and edge contacts) and methods for tailoring Schottky contacts through barrier-height tuning. Insights from advanced characterization techniques and theoretical models for extracting Schottky barrier height (SBH) and R_C are also integrated. Finally, we outline unresolved challenges and future directions, providing a roadmap toward rationally designed 2D contact interfaces for unlocking full device potential.



Fermi level pinning effect

Defects in 2D materials induced by vacuum-deposited metal electrodes

KEYWORDS: two-dimensional materials, metal electrodes, Ohmic contacts, Schottky contacts, Fermi-level pinning

1 Introduction

1.1 The promise and challenge of two-dimensional (2D) material contacts

Since the successful isolation of graphene via mechanical exfoliation in 2004, 2D materials have undergone rapid development and emerged as a leading research frontier in condensed matter physics, materials science, and nanotechnology [1–7]. Widely regarded as promising candidates for overcoming the scaling limitations of conventional silicon-based electronics, 2D materials offer a versatile platform for constructing next-generation ultrathin, flexible, and high-performance electronic and optoelectronic devices [8–13].

Unlike traditional three-dimensional (3D) semiconductors such as silicon, charge carriers in 2D materials are confined to a plane consisting of only one or a few atomic layers. This structural characteristic endows 2D materials with significant advantages for fabricating transistors with shorter channel lengths and lower power consumption [13, 14], while also making them highly attractive for applications in flexible electronics and wearable devices [15].

However, transitioning from the material level to a functional device architecture introduces a critical and ubiquitous challenge: the interfacial contact between metal electrodes and 2D materials. In any electronic device such as a field-effect transistor (FET) or

Received: January 6, 2026; **Revised:** February 6, 2026
Accepted: February 15, 2026

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photodetector, metal electrodes serve as essential conduits for charge carrier transport. In conventional semiconductors, Ohmic contacts with low resistance can be reliably achieved through heavy doping. Yet, this established methodology is largely inapplicable to 2D materials for several reasons.

The atomic-scale thickness of 2D materials precludes the use of traditional bulk doping techniques like ion implantation. Second, although the absence of dangling bonds on the surface of 2D materials contributes to their environmental stability, it also limits orbital hybridization with metal electrodes. This results in insufficient wavefunction overlap and the formation of a substantial interfacial energy barrier, namely, a Schottky barrier. Moreover, the delicate surfaces of 2D materials are prone to defect generation during metal electrode deposition. Issues such as interfacial stress further induce strong Fermi level (E_F) pinning (FLP), which exacerbates the formation of Schottky barriers and compromises contact performance.

Extensive studies have revealed that the performance of transistors based on 2D materials is often limited not by the intrinsic carrier mobility of the channel material, but rather by high contact resistance (R_C) at the electrode contact interface [16–29]. Consequently, achieving a fundamental understanding and precise control of the contact interface between 2D materials and metal electrodes has become a central scientific and technological challenge in unlocking their full application potential. This endeavor encompasses multiple dimensions, including tailoring the interfacial electronic structure, exploring novel contact geometries, mitigating the FLP effect, and developing stable and reproducible fabrication processes.

1.2 The dual nature of the Schottky barrier: Impediment vs. functional element

The Schottky barrier at the interface between 2D materials and metals exhibits a defining duality in 2D electronics. On the one hand, it represents a significant performance-limiting impediment. The absence of dangling bonds on 2D material surfaces was initially thought to favor ideal Ohmic contacts. In practice, however, factors such as interface defects, metal-induced gap states (MIGS), and impurities induce strong FLP. This makes the Schottky barrier height (SBH) largely insensitive to the metal work function, leading to prevalent Schottky contact behavior. In this regime, charge transport predominantly relies on inefficient thermionic emission over the barrier, which requires external energy injection. These contacts are often characterized by high reverse leakage current, poor reproducibility, and unstable device performance. Furthermore, the weak van der Waals (vdW) interaction at the interface often leaves a physical gap that reduces wave function overlap and increases tunnel resistance. Collectively, these effects degrade performance and increase manufacturing complexity, making the Schottky barrier a major bottleneck for scalable and high-performance logic transistors and integrated circuits.

Conversely, this inherent potential barrier is simultaneously a critical functional element in many devices. In applications such as photodetectors, photovoltaic cells, and sensors, the Schottky junction serves as an active component. Its built-in electric field efficiently separates photogenerated electron–hole pairs and governs carrier collection. The diode-like rectifying I–V characteristic, in which current increases exponentially under forward bias while remaining minimal under reverse bias, forms the physical basis for signal detection, rectification, and modulation. By strategically tuning the barrier height and width, engineers can optimize key device metrics, including the on/off ratio, spectral responsivity, and response speed. Therefore, the central challenge of contact engineering has evolved from merely eliminating the barrier to making a strategic choice: pursuing ultralow-resistance Ohmic contacts for transistor scaling while also intelligently harnessing and tailoring Schottky contacts to unlock the full potential of 2D materials in next-generation optoelectronic and multifunctional devices.

1.3 Scope and outline of the review

This review systematically summarizes key recent advances in the study of 2D materials-metal contacts. We begin by examining the fundamental physical mechanisms governing contact interface formation and Schottky barrier modulation. Next, we survey a range of strategies for R_C reduction, alongside the theoretical models, mathematical approaches, and experimental techniques used to characterize and quantify Schottky barriers. Finally, we outline future challenges and promising research directions, with the aim of providing theoretical insight and practical pathways for the design and fabrication of high-performance 2D electronic devices.

2 2D materials and the electrode contacts

2.1 The emergence of two-dimensional materials

Silicon-based devices are approaching their physical limits, making it increasingly difficult to further reduce transistor sizes while maintaining low power consumption. Globally, it is widely projected that at the 1 nm technology node, the pitch will shrink to around 40 nm, requiring both the gate length and the contact length to be less than 20 nm [30]. Moreover, maintaining low-resistance Ohmic contacts at this scale remains a core challenge in device fabrication. Existing contact technologies often suffer from a sharp increase in resistance at such dimensions, hindering their transition to industrial applications. In contrast, 2D materials with their atomic-level thickness, tunable bandgap, flexible stacking configurations, and high effective mass are compatible with silicon-based technology and can compensate for its limitations, thereby effectively advancing the development of next-generation devices.

After years of development, 2D materials have formed a large family, including graphene, transition metal dichalcogenides (TMDs; MX_2, M: transition metal element, X: chalcogens element), MXenes ($M_{n+1}X_nT_x$, M: transition metal element, X: C element or N element; T_x: terminated functional groups, –O, –OH, or –F; n = 1–4), group IV Xenes (silicene, germanene, or staniene), group V Xenes (phosphorene, arsenene, antimonene, and bismuthene), oxides, and hydroxides (Figs. 1(a)–1(d)). For example, 2D TMDs can effectively suppress short-channel effects and are promising for fabricating next-generation integrated circuits and chips with reduced footprint and lower power consumption (Fig. 1(e)) [24, 31, 32]. Moreover, TMDs have also been employed in high-performance neuromorphic computing, electrochemical energy storage, solar cells, and numerous other applications, where significant improvements in device performance have been demonstrated [32–34]. Furthermore, the synthesis of large-area 2D TMDs with controllable rhombohedral structures has endowed them with enhanced stability, higher effective carrier mobility, and novel ferroelectric properties, among other advantages, revealing potential that surpasses that of many conventional devices [35–37].

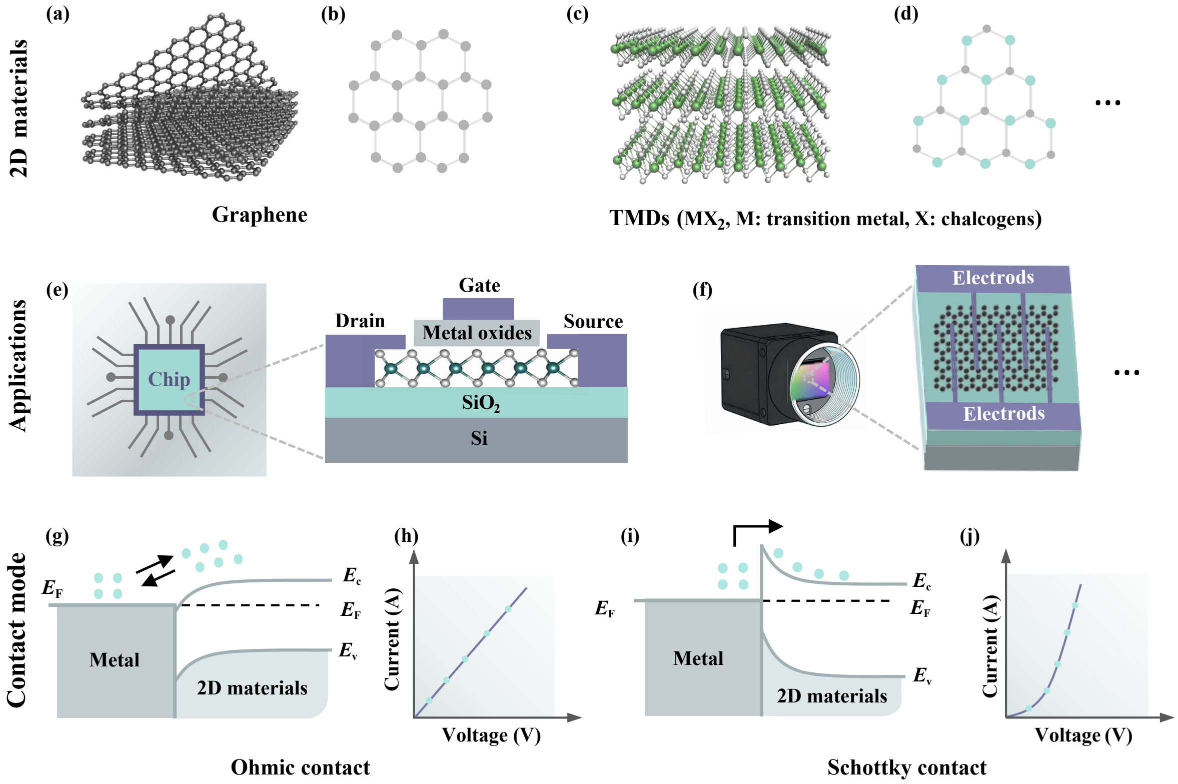


Figure 1 Contact mode of 2D materials-metal electrodes. ((a) and(c)) Side views of the atomic structure schematic diagram of selected 2D materials, graphene, and TMDs. ((b) and(d)) Top views of the atomic structure schematic diagram of graphene and TMDs. ((e) and(f)) Schematic diagram of the chip, FET, and photoelectric detector. (g) Simplified electronic band diagram and Ohmic contact mode at the interface of metal–2D materials. (h) *I*–*V* curve of Ohmic contact mode. (i) Simplified electronic band diagram and Schottky barrier at the interface of metal–2D materials. (j) *I*–*V* curve of Schottky contact mode.

Graphene production has become mature and stable in laboratories, enabling the preparation of large-scale and high-quality single crystal graphene [3, 6, 38–41]. Moreover, graphene exhibits excellent photoelectric properties, flexibility, transparency, etc., which is widely used in high-performance photodetectors, flexible electronic devices, terahertz intelligent surface, and supercapacitors [8–11, 31, 32, 42]. For instance, graphene photodetectors, due to their good stability and strong light absorption capacity, have the advantages of high speed and high sensitivity (Fig. 1(f)) [5, 6, 11, 12, 38, 39, 43–45]. Furthermore, due to its conductive properties similar to those of conductors and its extremely high carrier mobility, graphene is often used as the electrode material for various devices [46–48].

Due to their outstanding properties, 2D materials exhibit high sensitivity, selectivity, and rapid response in many applications. More importantly, they have demonstrated the ability to replace silicon-based devices. However, for integrated circuits and practical applications, the performance of 2D material devices is significantly affected by the contact mode (Ohmic contact mode or Schottky contact mode) between the materials and metal electrodes, which directly affects their switching speed, power consumption, heat generation, and performance limit [18, 49, 50].

2.2 Two fundamental types of 2D material–metal contact interfaces

The operation of the device depends on whether electrons can be efficiently injected or extracted into the 2D material channel. When the Ohmic contact mode is established between the 2D material and the metal electrode, the potential barrier is very low or non-existent, charge carriers can be efficiently injected or extracted (Fig. 1(g)), and the current–voltage (*I*–*V*) characteristics are a straight line passing through the origin, showing constant resistance at different voltages (Fig. 1(h)). Ohmic contact enables efficient power transmission and signal transmission, ensuring the reliability and stability of the device, and is a prerequisite for the size reduction of modern microelectronics technology.

The absence of dangling bonds on 2D material surfaces was initially thought to favor the formation of ideal Ohmic contacts. In practice, however, interface defects, MIGS, and impurities cause strong FLP. This easily leads to the formation of a Schottky barrier with a height that is not readily tunable, despite the selection of a metal with a matching work function (W_m). As a result, the contact interface typically behaves as a Schottky contact. In this regime, charge carrier transport predominantly relies on thermionic emission over the barrier (Fig. 1(i)), which requires external energy injection. Such contacts often exhibit high reverse leakage current, poor reproducibility, and unstable device performance, collectively increasing manufacturing cost and complexity. Obviously, the *I*–*V* curve of Schottky contact is significantly different from that of Ohmic contact. The *I*–*V* curve of Schottky contact is similar to a diode, where the current increases exponentially with voltage under forward bias and is very small under reverse bias (Fig. 1(j)). What's more, due to the surface inertness of 2D materials, metal deposition may not form tight chemical bonds, but instead leave a "vdW gap". This gap weakens wave function overlap, increases tunnel resistance, and makes carrier transport inefficient, which will also affect device performance.

The rise of 2D materials has opened up endless possibilities for future electronics, but the contact interface between them and metals is crucial for device performance. A deep understanding of the formation mechanisms, characteristics, and differentiation between Schottky and Ohmic contacts, along with addressing the unique FLP and vdW gap issues inherent in 2D materials, is crucial for advancing high-performance 2D material devices from the laboratory to practical applications. We will now explore these issues in detail.

2.3 Determination of 2D material-metal electrode contact type via *I–V* curves

In electrical testing, metal electrodes are fabricated on both ends of the 2D material under test, and the *I–V* curve is measured. Analysis of this curve can preliminarily indicate whether the 2D material–metal electrode interface exhibits Ohmic or Schottky contact behavior. The key lies in observing the linearity, symmetry, and rectification characteristics of the *I–V* relationship.

If the *I–V* curve within the test voltage range is a straight line passing through the origin, it suggests Ohmic contact. If it shows a clear diode-like curve, it indicates Schottky contact. In ambiguous cases, a comprehensive judgment that combines test temperature, logarithmic scale analysis, and other factors is necessary (details are summarized in Table 1).

2.3.1 Ohmic contact

No significant barrier exists at the metal–semiconductor interface, or the barrier is extremely low and thin (carriers can easily tunnel through). Carriers pass bidirectionally, unobstructed, and linearly, resembling a pure resistor.

I–V Characteristics: A straight line passing through the origin, perfectly symmetric under positive and negative voltages.

Non-ideal cases: If symmetric but not perfectly linear, it may still be an Ohmic contact with non-ideal factors such as R_C variation, Joule heating, or carrier mobility changes under high field.

2.3.2 Schottky contact

A significant Schottky barrier exists at the metal–semiconductor interface, and exhibits rectification characteristics, similar to a diode: easy conduction in the forward direction (barrier lowering) and difficult conduction in the reverse direction (barrier raising).

I–V characteristics: Diode-like curve with rapid increase in forward current and small and saturated reverse current.

2.3.3 Mixed contact scenarios

Double Schottky contacts: Regardless of voltage polarity, one contact is always reverse-biased, resulting in a symmetric but nonlinear *I–V* curve (current suppressed at low voltage, possibly dominated by tunneling or thermionic emission at high voltage). This can be easily confused with imperfect Ohmic contacts and requires consideration of the semiconductor type.

One Ohmic contact & one Schottky contact: The measured result is a standard Schottky diode *I–V* curve.

2.4 Characterization and modeling of contact properties

The SBH and R_C are pivotal parameters that define the electronic properties of metal–2D material interfaces. The SBH represents the energy barrier that charge carriers must surmount when transitioning between the metal and the 2D semiconductor. It governs key device characteristics such as rectification behavior in diodes, carrier injection efficiency in transistors, and ultimately impacts switching speed and power consumption. Conversely, R_C quantifies the ease with which current flows across the contact interface. Elevated R_C not only limits on-state current but also increases energy dissipation and degrades effective carrier mobility, often causing device performance to be dominated by interfacial properties rather than the intrinsic channel material. Therefore, accurate and reliable measurement of both SBH and R_C is essential for evaluating contact interface quality and guiding the design of high-performance 2D electronic devices.

2.4.1 The experimental techniques for SBH extraction

2.4.1.1 Temperature-dependent *I–V* method

A commonly adopted method for extracting the SBH involves measuring the current–voltage (I–V) characteristics of the device at different temperatures and analyzing the data within the framework of thermionic emission theory for Schottky diodes. This method is called the temperature-dependent *I–V* method, thermionic emission–Arrhenius plot analysis, or barrier height extraction via temperature-dependent current–voltage measurements.

According to this model, the current in a Schottky barrier diode under forward bias can be described by the relation [51]

$$I_{DS} = A^{*}AT^{\frac{3}{2}}\exp\left[-\frac{q}{k_B T}\left(\Phi_B - \frac{V_{DS}}{n}\right)\right] \quad (1)$$

where A^* is the 2D equivalent/ effective Richardson constant, A denotes the contact area of the junction, n represents the ideality factor that accounts for deviations from pure thermionic emission, V_{DS} is the applied drain–source voltage, q is the elementary charge, k_B is the Boltzmann's constant, T is the absolute temperature, and $q\Phi_B$ is the Schottky barrier height. The traditional Richardson constant (for 3D materials) is associated with T^2 as the exponent of temperature. However, for 2D materials, the density of states and the thermionic emission model must be modified, leading to a temperature dependence of $T^{3/2}$ in the current expression. By measuring *I–V* curves at different temperatures and fitting them to this expression, one can extract both the $q\Phi_B$ and the ideality factor n, providing insight into the contact interface quality and carrier transport mechanism.

Table 1 The judgment basis for the *I–V* curve of the Schottky contacts and Ohm contacts

Contact type	*I–V* curve feature	Symmetry	Rectification	Typical scenario
Ohmic contact	Straight line through origin	Symmetric	No	Heavily doped semiconductor, tunneling contact
Schottky contact	Diode curve (forward conducting, reverse blocking)	Asymmetric	Yes	Lightly doped semiconductor, classic barrier contact
Double Schottky	Symmetric but nonlinear	Symmetric	Yes (bidirectional suppression)	Both contacts are Schottky type
One Ohmic & One Schottky	Standard diode curve	Asymmetric	Yes	Hybrid contact structure

Taking the natural logarithm of both sides yields a linearized Arrhenius-type relation

$$\ln\left(\frac{I_{DS}}{T^{\frac{3}{2}}}\right) = \ln(A^*A) - \frac{q}{k_B T}\left(\Phi_B - \frac{V_{DS}}{n}\right) \quad (2)$$

This form enables the extraction of the SBH and ideality factor from the slope and intercept of $\ln(I_{DS}/T^{3/2})$ versus $1/T$ plots at fixed bias voltages. Experimentally, the device is characterized in a variable-temperature probe station to acquire I–V curves over a controlled temperature range (Fig. 2(a)). From these measurements, Arrhenius plots are constructed with $1000/T$ on the horizontal axis and $\ln(I_{DS}/T^{3/2})$ on the vertical axis for several applied voltages (Fig. 2(b)). The slope S of each fitted line is given by

$$S = -\frac{q}{1000k_B}\left(\Phi_B - \frac{V_{DS}}{n}\right) \quad (3)$$

By plotting S as a function of V_{DS} and performing a linear regression, the y-intercept S_0 yields the zero-bias SBH (Fig. 2(c))

$$S_0 = -\frac{q\Phi_B}{1000k_B} \quad (4)$$

This approach provides a direct means to quantify the SBH and evaluate the contact interface quality, though it assumes the dominance of thermionic emission and may require additional modeling if other transport mechanisms contribute significantly.

This method relies on the validity of the thermionic emission model within the temperature and bias ranges where it dominates the carrier transport. In cases where pronounced interface states, tunneling effects, or non-ideal factors are present, it is often necessary to combine the capacitance–voltage method (C–V method) or internal photoemission (IPE) spectroscopy method for cross-validation, in order to obtain more accurate SBH and interface characteristics.

2.4.1.2 Capacitance–voltage method

Another way to extract the SBH is through the C–V method [52]. A series of different bias voltages V are applied to the metal electrodes of the device using a capacitance–voltage tester, and the corresponding capacitance C is record. The relationship between $1/C^2$ and V in the low bias region can be expressed by Eq. (5) [16]

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_s n}(\Phi_B - V) \quad (5)$$

where ε_s is the dielectric permittivity, n is the carrier concentration, and q is the electron charge. The curve of $1/C^2$ versus V is plotted, and the intercept voltage of the curve is Φ_B.

2.4.1.3 IPE spectroscopy method

The physical principles of measurement of photocurrent [53] at the junction are the photoelectric effect. The energy of photons is directly used to excite carriers to cross the Schottky barrier at the 2D materials–metal contact interface. When photons with energy $h\nu$ strike a metal electrode, if $h\nu > q\Phi_B$ (the photon energy is greater than the barrier energy), electrons would be excited and have the opportunity to cross the barrier and enter the 2D materials, forming a photocurrent. The critical threshold for the generation of photocurrent corresponds to the SBH, that is, $h\nu_0 = q\Phi_B$. By determining this threshold energy, $q\Phi_B$ can be directly obtained. This method requires that the metal be thin enough to ensure light penetration. The ratio of the photocurrent to the absorbed photon flux is given by [16]

$$Y = B(h\nu - q\Phi_B)^2 \quad (6)$$

where B is a constant. Taking $Y^{1/2}$ as the Y-axis and the photon energy $h\nu$ as the X-axis, a curve is plotted and linear fitting is performed. The intercept $h\nu_0$ of the curve on the X-axis is the height of the Schottky barrier $q\Phi_B$.

2.4.2 *The experimental techniques for contact resistance extraction*

The magnitude of the R_C plays a critical role in determining the electrical performance of devices based on 2D materials. In most practical applications, minimizing R_C at the metal–2D material contact interface is essential, as high R_C can severely limit charge injection efficiency, degrade carrier mobility, and obscure the intrinsic properties of the 2D channel. Therefore, accurate quantification of R_C is not only vital for evaluating device performance but also serves as a key metric for assessing interface quality and the effectiveness of contact engineering. To this end, several established experimental techniques are commonly employed for extracting R_C in 2D material-based devices. In this section, we introduce three widely used methods [16]: the Y-function method, the four-point probe measurement, and the transport length method.

2.4.2.1 Y-function method

The Y-function method is a widely utilized technique for extracting the R_C in FETs based on 2D materials, where the 2D material serves as the channel, and the SiO_2/Si serves as the insulator layer and back-gate electrode. Its fundamental principle lies in decoupling the contribution of R_C from the total device resistance R through analysis of the transistor's I–V characteristics. Prior to electrical characterization, the 2D material is fabricated into a FET structure (see device parameters in Table 2). The total resistance R of the device comprises the R_C at both source and drain contacts ($2R_C$) and the channel resistance (R_{CH})

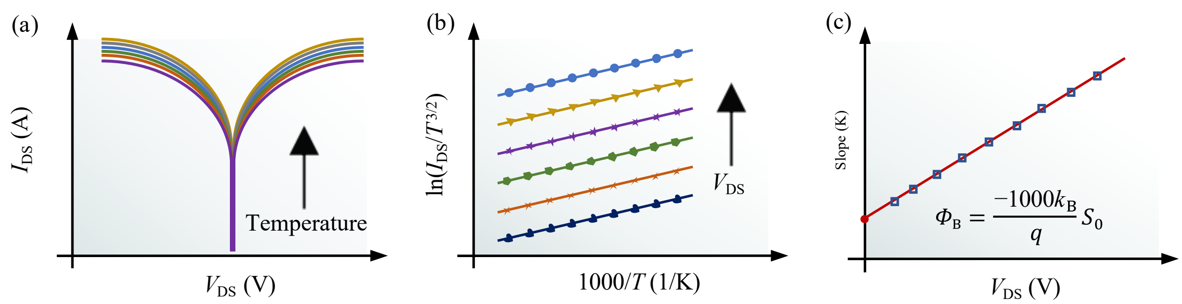


Figure 2 The extraction process of SHB. (a) I–V curves of the FET device from different temperatures. (b) Arrhenius plot $\ln(I_{DS}/T^{3/2})$ vs. $1000/T$ at different V_{DS}. (c) The slope extracted from the Arrhenius plot in (b). The y-intercept value represents SBH.

$$R = 2R_C + R_{CH} \tag{7}$$

Assuming a long-channel gradual-channel approximation in the linear regime, the drain–source current can be expressed as

$$I_{DS} = \frac{V_{DS}}{2R_C + R_{CH}} = \frac{V_{DS}}{2R_C + \dfrac{L}{\mu C_{OX} W (V_G - V_T)}} \tag{8}$$

where C_{OX} is the gate dielectric capacitance per unit area (for a typical SiO_2 dielectric, C_{OX} of SiO_2 is about from 11 to 12 $nF \cdot cm^{-2}$), μ is the field-effect mobility, L and W are the channel length and width, respectively, V_G is the gate voltage, V_T is the threshold voltage, and V_{DS} is the drain–source voltage. The transconductance g_m is obtained by differentiating the drain–source current I_{DS} with respect to the V_G

$$g_m = \frac{dI_{DS}}{dV_G} = \frac{\dfrac{W}{L} \cdot \mu \cdot C_{OX} \cdot V_{DS}}{\left[1 + \dfrac{W}{L} \cdot \mu \cdot C_{OX} \cdot 2R_C \cdot (V_G - V_T)\right]^2} \tag{9}$$

The Y function is then defined as

$$Y = \frac{I_{DS}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} \mu C_{OX} V_{DS}} \, (V_G - V_T) \tag{10}$$

Experimentally, FET devices are electrically characterized, and both g_m and Y are computed from the measured I_{DS}–V_G data. A linear fit of Y versus V_G yields a slope denoted as k_1. Similarly, the slope k_2 is obtained from a linear fit of Y versus I_{DS}. The total R_C is then determined as

$$2R_C = k_1^{-1} k_2 V_{DS} \tag{11}$$

This method provides a straightforward and parameter-extraction-based approach for evaluating R_C without requiring specific test structures such as four-point probe measurement patterns, making it particularly convenient for early-stage device screening and comparative contact studies in 2D material FETs.

2.4.2.2 Four-point probe measurement

The four-point probe method is a widely adopted technique for accurately extracting R_C in 2D material devices. The total device resistance comprises both the R_{CH} and R_C. In conventional two-probe measurements, when R_{CH} is relatively small, the contribution of R_C can dominate the measured resistance, leading to significant errors in evaluating intrinsic material properties. The four-point probe method effectively addresses this issue by physically separating the current injection and voltage sensing paths.

A common implementation employs a Hall bar structure (as pictured in the panel in the middle and upper part in Table 2) or a linear four-probe structure (in the panel in the middle and lower part). In a typical configuration, four metal electrodes are deposited onto the 2D material and sequentially labeled 1–4. A known constant current (I_{14}) is applied between the two outer probes (1 and 4), while the voltage drop (V_{23}) is measured between the two inner probes (2 and 3). Assuming a uniform electric field and homogeneous material properties between the probes, the voltage varies linearly with distance along the channel. Under these conditions, the total resistance between the outer contacts can be expressed as

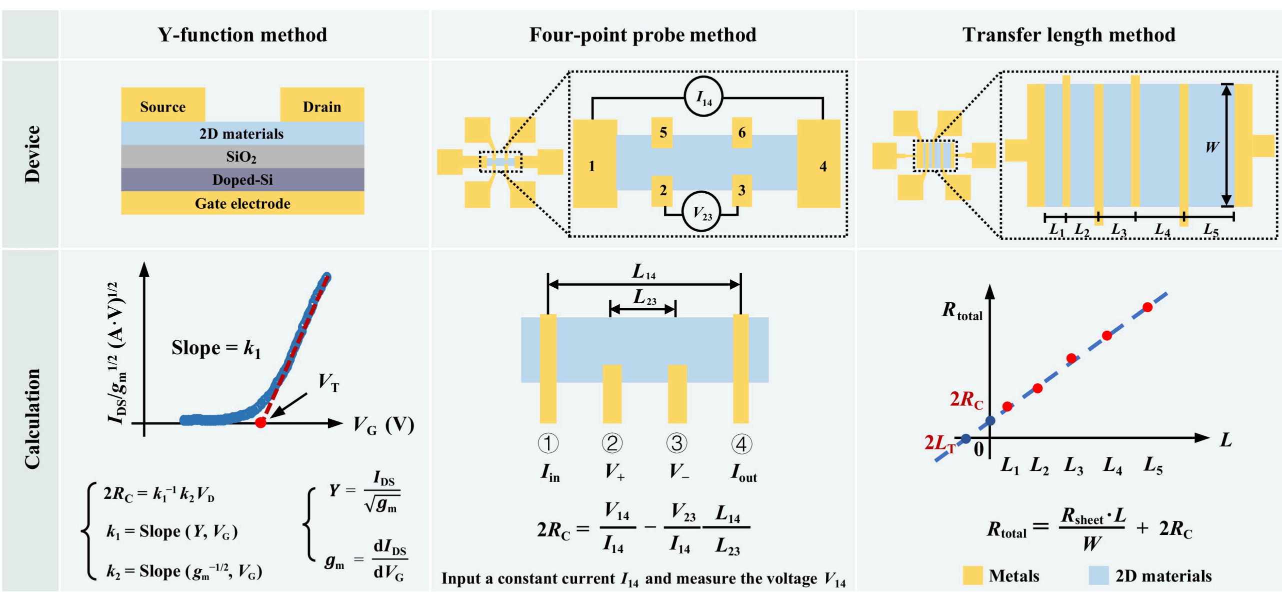
$$2R_C = \frac{V_{14}}{I_{14}} - \frac{V_{23}}{I_{14}} \frac{L_{14}}{L_{23}} \tag{12}$$

where L_{14} and L_{23} represent the distances between probes 1 and 4, and 2 and 3, respectively. To minimize perturbation of the electric field, the voltage probes should ideally be point-like or have dimensions much smaller than the channel length.

2.4.2.3 Transfer length method

The transfer length method is another established approach for determining R_C and the transfer length (L_T), which characterizes the

Table 2 Three methods to extract contact resistance[a]



[a]This table summarizes three commonly used techniques for extracting R_C in 2D material-based electronic devices, including Y-function method, four-point probe method, and transport length method.

spatial extent over which current transfers from the contact into the 2D channel. In the transfer length method, a series of test structures with identical channel width (W) but varying channel lengths (L) are fabricated, as summarized in Table 2. The total resistance R_{total} of each device is given by

$$R_{total} = 2R_C + R_{CH} = 2R_C + \frac{R_{sheet} \cdot L}{W} \tag{13}$$

where R_{sheet} is the sheet resistance of the 2D material. For an ideal Ohmic contact, the R_C can be expressed in terms of the transfer length

$$R_C = \frac{R_{sheet} \cdot L_T}{W} \tag{14}$$

Thus, the total resistance can be rewritten as

$$R_{total} = \frac{R_{sheet}}{W}(L + 2L_T) \tag{15}$$

Experimentally, R_{total} is measured for devices with different L, and a linear fit of R_{total} versus L is performed. The vertical axis intercept yields $2R_C$, while the horizontal axis intercept (i.e., where $R_{total} = 0$) gives $-2L_T$. This method provides direct access to both the R_C and the transfer length, offering valuable insight into the quality and geometry of the metal–2D material contact interface.

3 Fundamental physics of 2D material–metal contacts

3.1 Schottky–Mott rule and its limitations in 2D systems

The Schottky–Mott rule, a cornerstone of conventional metal–semiconductor contact theory for three-dimensional semiconductors, predicts that the SBH at an ideal interface is determined by the difference between the metal work function and the semiconductor electron affinity (χ) or ionization energy. However, this model encounters fundamental challenges and significant limitations in 2D material systems. First, the atomic thinness of 2D materials results in extremely weak electrostatic screening, allowing the electric field from the metal electrode to penetrate the entire channel. This renders the traditional depletion region approximation invalid and drastically alters the physical picture of interface band bending. Second, while the absence of dangling bonds on 2D surfaces was expected to facilitate the realization of the Schottky–Mott ideal limit, in practice, interface defect states, MIGS, the vdW gap, and inevitable FLP strongly disrupt the presumed linear relationship between metal work function and barrier height. Consequently, even with careful selection of a metal whose work function aligns with the band structure of the 2D material, the experimentally measured barrier height often deviates from theoretical predictions. This severely reduces the applicability of the Schottky–Mott rule in guiding contact design for 2D materials, highlighting the urgent need to develop more accurate contact theory models tailored to low-dimensional systems.

The contact types between metals and 2D materials are primarily governed by W_m and the semiconductor types (n-type or p-type) of the 2D materials. The work function, defined as the energy difference between the vacuum level (E_0) and the E_F, is a key parameter. For an n-type 2D material with a work function (W_{2D}), if $W_m > W_{2D}$, the metal E_F lies below that of the semiconductor before contact (Fig. 3(a)). Here, E_c and E_v denote the conduction

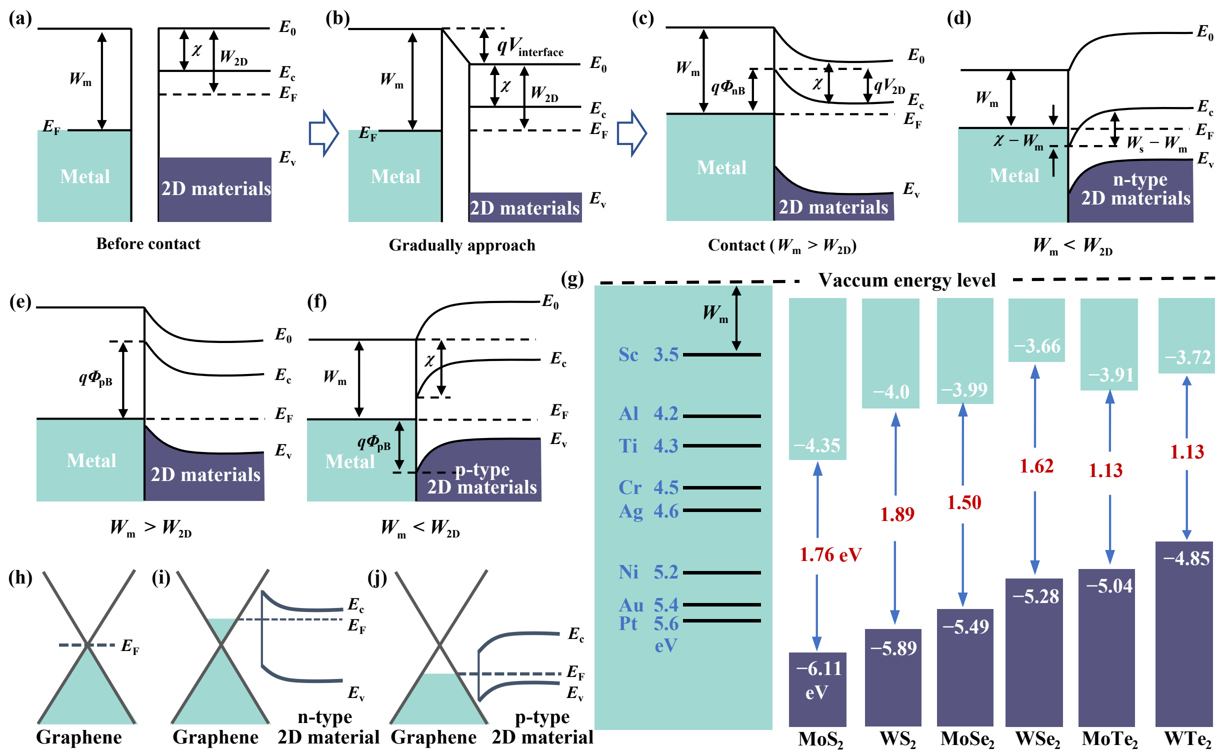


Figure 3 The formation process of the Schottky barrier in 2D materials–metal electrodes. ((a)–(c)) A schematic process of metal–semiconductor contact formed between metals and n-type 2D semiconductors, with $W_m > W_{2D}$. Simple energy level diagrams of metal–2D semiconductor contact, on the condition of (d) $W_m < W_{2D}$ of n-type 2D materials, (e) $W_m > W_{2D}$ of p-type 2D materials, and (f) $W_m < W_{2D}$ of p-type 2D materials. (g) Energy band alignment of different metals and different 2D materials [54–58]. ((h)–(j)) Contact between graphene and 2D materials with different W_{2D}.

band minimum and valence band maximum, respectively, and χ represents the electron affinity of the 2D material, defined as

$$\chi = E_0 - E_c \tag{16}$$

Upon electrical contact, electrons flow from the higher E_F (2D material) to the lower one (metal). This charge carrier transfer causes the energy bands of the 2D material to bend until E_F aligns across the interface, establishing a contact interface potential (denoted as $qV_{interface}$) at the junction (Fig. 3(b)). Upon close contact, a corresponding surface potential V_{2D} (Fig. 3(c)) is also induced within the 2D material. The maximum potential energy difference, known as the built-in potential, is given by

$$qV_D = W_m - W_{2D} \tag{17}$$

The magnitude of this potential difference is typically small and can usually be ignored. The resulting SBH ($q\Phi_{nB}$ or $q\Phi_{pB}$) for electrons on the metal side is defined as

$$q\Phi_{nB} = qV_D + E_c - E_F = W_m - \chi \tag{18}$$

The Φ_{nB} or Φ_{pB} means the electric potential of the SBH of an n-type or p-type 2D material, respectively. Some papers sometimes simply write potential energy $q\Phi_B$ as electric potential Φ_B. A contact characterized by such an energy barrier is termed Schottky contact.

The presence of the Schottky barrier impedes electron transport, as carriers must acquire sufficient energy to overcome it via thermionic emission. This process exhibits a distinct threshold behavior: Once the applied voltage exceeds a critical value, electron transport across the barrier becomes significant, resulting in a rapid increase in current (Fig. 1(i)). This pronounced rectifying characteristic makes Schottky contacts particularly suitable for diodes, photodetectors, and FETs that require rectification or precise barrier control. A key advantage of Schottky contacts lies in their ability to effectively modulate carrier injection by engineering the contact interface barrier height, thereby providing a powerful means to regulate fundamental device electrical characteristics.

Schottky contacts are valuable for their rectifying properties, but they typically exhibit high R_C. This not only impedes carrier injection, reduces conductivity, and increases power consumption, but can also lead to undesirable effects such as pronounced device hysteresis, slower response times, and localized Joule heating, all of which compromise device performance and long-term reliability [59, 60]. To overcome these limitations in applications requiring efficient current flow, the formation of low-resistance Ohmic contacts is essential for the practical integration of 2D material-based electric devices.

It is important to note that the presence of a potential barrier does not completely block electron transport. Due to thermal motion, electrons possess a finite thermal energy given by

$$E_{thermal} = k_B T \tag{19}$$

where k_B is the Boltzmann constant and T is the absolute temperature. At room temperature ($T \approx 300$ K), this energy amounts to approximately 0.0259 eV. This energy enables a fraction of electrons to overcome the Schottky barrier even under low or zero bias, a mechanism central to thermionic emission theory. Although the average electron energy remains below the barrier height, a small subset of electrons in the high-energy tail of the Fermi–Dirac distribution can be thermally excited across the barrier. This process gives rise to a temperature-dependent leakage current, often observed as an increase in dark current in electronic devices.

In contrast, when W_m is less than W_{2D}, on one side of the 2D material, the energy band bends downward, facilitating electron transmission across the 2D materials–metal contact interface, resulting in a low R_C (Fig. 3(d)). Such contacts exhibit a linear I–V curve and adhere to Ohm's law, thus being classified as Ohmic contact. Ohmic contacts offer low-resistance and rectification-free carrier injection, thereby improving device conductivity, energy efficiency, and reliability. They are essential for interface optimization in nearly all electronic and power devices. In the case of p-type 2D materials (Figs. 3(e) and 3(f)), the energy band bending direction aligns with that of n-type materials, solely determined by the work function's relative magnitude, independent of the material's n/p-type. Figure 3(g) presents the energy band alignment between typical metals and 2D materials.

Graphene is frequently employed as an electrode material for 2D semiconductors, owing to its exceptional transparency, high electrical conductivity, remarkable electron mobility, and absence of surface dangling bonds [61]. Furthermore, its unique linear band structure leads to distinctive band alignments at the graphene–2D material interface (Figs. 3(h)–3(j)). Figure 3(h) depicts the band structure of pristine graphene, where the E_F crosses the Dirac point, characteristic of its neutral and undoped state. Figure 3(i) shows the interface formed with a low-work-function 2D material, which induces electron transfer into graphene. This process raises the E_F of graphene, effectively leading to n-type doping. Conversely, Fig. 3(j) illustrates the interface with a high-work-function 2D material, where electrons transfer from graphene to the 2D semiconductor, thereby lowering graphene's E_F and inducing p-type doping. Precise modulation of graphene's E_F through such interfacial interactions is critical for optimizing device performance, enhancing photoresponse characteristics, and expanding the applications of graphene in electronics and optoelectronics.

3.2 Charge transfer and interface dipole formation

Charge transfer and interface dipole formation represent the fundamental microscopic processes that govern the electrical performance at 2D material-metal contacts. In a canonical system such as the contact between a high-work-function metal (e.g., Pt) and an n-type 2D semiconductor like MoS_2, charge transfer (or injection) is primarily governed by two distinct mechanisms: thermionic emission and field emission.

In thermionic emission, electrons must acquire sufficient kinetic energy to surmount the interfacial Schottky barrier. This process dominates under conditions of low gate bias or in the absence of intentional channel doping, with its injection efficiency exhibiting a strong, exponential dependence on temperature. Conversely, field emission relies on quantum tunneling through the barrier. In a FET configuration, for instance, applying a gate voltage can significantly modulate the 2D material's band structure, leading to a pronounced thinning of the barrier width. Coupled with a high lateral electric field and a large interfacial carrier density, this enables direct electron tunneling.

In practical device operation, these mechanisms are not mutually exclusive but often coexist, giving rise to a hybrid thermionic-field emission regime [62]. Here, electrons are thermally excited to an energy level where the remaining barrier width is sufficiently narrow for efficient tunneling through its top portion, representing a crossover behavior between pure thermal activation and pure tunneling. Crucially, these charge transfer processes are not uniform. At the metal–semiconductor interface, the overlap and distribution disparity of electron clouds induce a spatial separation of charge at the atomic scale, spontaneously forming a built-in interfacial electric dipole layer. The internal electric field generated by this dipole layer further modulates the interface band bending and the SBH. Consequently, it emerges as a pivotal and actively tunable physical factor (alongside metal work function and FLP) that ultimately determines the final contact properties.

3.3 Application of Schottky contact and Ohmic contact

In 2D material devices, the quality of contact between metals and 2D materials significantly influences device performance. Schottky contacts and Ohmic contacts serve distinct functions and are selectively utilized in diverse electronic and optoelectronic devices.

Schottky contact is extensively utilized in Schottky diodes, gas sensors, and photodetectors due to their inherent electric fields, which facilitate the spontaneous separation of charge carriers and mitigate reverse currents [63]. For example, in the asymmetric metal-contact photodiode device constructed by Han et al. (Fig. 4(a)) in 2022, the relatively high work function of Pd, approximately 5.12 eV, results in the formation of a significant Schottky barrier with n-type Bi_2O_2Se [64]. In contrast, Ti has a lower work function of approximately 4.26 eV, allowing the Ti electrode to establish Ohmic contact with Bi_2O_2Se (Fig. 4(b)). This configuration generates an internal asymmetric band distribution, enabling a self-driven optical response under zero bias conditions. The device demonstrates a broad spectral detection capability, ranging from 450 to 1400 nm, and exhibits a high switching ratio exceeding 10^3. The electrical rectification of the device is illustrated in Fig. 4(c). Correspondingly, the optoelectronic performance is shown in Fig. 4(d), which presents the current response under illumination across a range of incident optical power levels. In 2018, Dai et al. developed an Au/InSe/In asymmetric Schottky junction photodetector by depositing Au and In electrodes at opposite ends of the InSe material [65]. This device exhibited a spectral response range of 365–700 nm and demonstrated a rapid response time on the order of milliseconds. Notably, it achieved high response rates of 369 mA·W^{-1} at 365 nm and 244 mA·W^{-1} at 685 nm. Utilizing the barrier regulation effect, Tabata et al. constructed a Graphene/MoS_2 heterojunction gas sensor denoted as "GMH" in 2018 [66] (Fig. 4(e)). A Schottky barrier formed between graphene and MoS_2, allowing for the tunability of both bias and gate voltages. Figure 4(f) presents the I–V curves of the GMH sensor before and after the adsorption of NO_2 gas. The sensing mechanism primarily arises from the modulation of the barrier height induced by gas molecules.

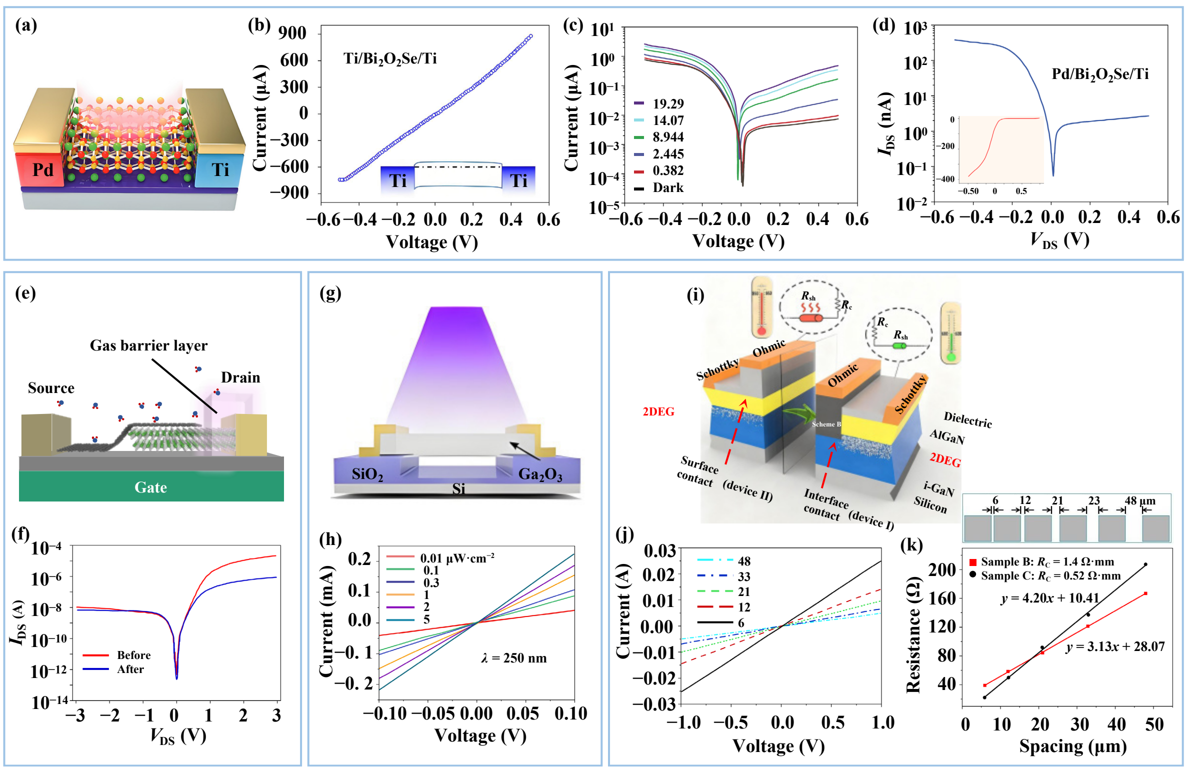


Figure 4 Applications of Schottky contact and Ohmic contact. (a) The schematic of Pd/Bi_2O_2Se/Ti photodetector under irradiation. The electrodes are in Schottky contact with Bi_2O_2Se. Reproduced with permission from Ref. [64], © Wiley-VCH GmbH 2022. (b) After replacing the Pd electrode in (a) with a Ti electrode, an Ohmic contact between the electrode and the 2D material is formed, which can be applied to photodetectors. (c) The logarithmic I–V curve of the Pd/Bi_2O_2Se/Ti photodiode. Inset: the diode behavior of the device. (d) I–V curves of the device as a photodetector under different laser power densities (500 nm). (e) Schematic of the GMH device with a gas barrier layer. The GMH device is a Schottky gas sensor, which can be viewed as an FET. Reproduced with permission from Ref. [66], © American Chemical Society 2018. (f) I_{DS}–V_{DS} curves for the GMH device before and after NO_2 exposure. (g) The schematic of the Ga_2O_3 photodetector. The electrodes are in Ohmic contact with Ga_2O_3. (h) Dependence of photocurrent on voltage under different illumination power intensity. Reproduced with permission from Ref. [69], © Li, X. X. et al. 2024. (i) The schematic of the AlGaN/GaN HEMT power device and an FET after annealing temperatures of 850 and 600 °C, respectively. Power devices operate in conditions of high current and voltage. The presence of a barrier at the contact interface leads to high R_C, causing additional power loss and impacting device reliability. Consequently, the use of Ohmic contact is essential to facilitate low-resistance carrier injection. Reproduced with permission from Ref. [70], © Elsevier Ltd. 2018. (j) I–V characteristics of scheme B in (e) annealed at 600 °C, which presented linear curves. (k) Measurement of R_C for scheme B annealed at 600 °C and scheme C using the transport length method test structure. The inset shows the transport length method patterns. Ohmic contact can be applied to characterization.

Unlike Schottky contact, which exhibits the "rectification effect", Ohmic contact is advantageous for enhancing carrier injection efficiency, minimizing resistance, and facilitating low-power transmission in applications such as power devices, characterization, and photodetectors [67, 68].

In 2024, the Ga_2O_3 photodetector constructed by Li et al. demonstrates that the electrode establishes an Ohmic contact with the Ga_2O_3 channel material (Fig. 4(g)) [69]. Under illumination at various power levels at 250 nm-wavelength, the device exhibits photocurrents of varying intensities that correlate positively, as illustrated in Fig. 4(h). This device successfully achieves both a high response rate and a rapid response time under ultra-weak light intensity. In 2019, Chen et al. addressed the challenge of reduced device mass resulting from high-temperature annealing in AlGaN/GaN high electron mobility transistor (HEMT) [70], as illustrated in Fig. 4(i), by removing the AlGaN barrier layer through plasma etching. When metals are directly in contact with GaN/AlGaN at an annealing temperature of 600 °C, a low R_C Ohmic contact is established, leading to an increase of 23% in saturation current. This finding underscores the beneficial impact of Ohmic contact on carrier transport in power devices (Fig. 4(j)). Furthermore, they measured R_C (6.29×10^{-5} Ω·cm^2) of the device using the transport length method (Fig. 4(k)). In electrical characterization, Ohmic contact is crucial; only when the electrode does not create an additional potential barrier can the carrier transport characteristics accurately reflect the intrinsic properties of 2D materials.

As demonstrated above, Schottky contact is appropriate for diodes, gas-sensitive devices, and optoelectronic devices that necessitate barrier control. In contrast, Ohmic contact is primarily utilized in low-resistance and low-loss power devices, photodetectors, and device characterization. An effective design of these two types of contacts must be grounded in the specific functions and requirements of the devices to fully leverage the capabilities of 2D materials.

3.4 Fermi-level pinning effect: Origins and mechanisms

The modulation of the SBH is governed by a far more complex set of parameters than the idealized W_m and material electron affinity, primarily due to extrinsic interface effects. In practice, the SBH is influenced by a multitude of factors. Empirical evidence consistently shows that the E_F in real devices often deviates from theoretical predictions and exhibits no systematic correlation with W_m. This discrepancy is attributed to FLP, a phenomenon driven by inherent defects in the 2D materials, interface states, and other perturbations (Figs. 5(a) and 5(b)). As illustrated in Fig. 5(a), FLP results in a fixed E_F that becomes insensitive to external modifications. The strength of this effect is quantified by the pinning factor, defined as [71]

$$S = \left| \frac{\mathrm{d}(q\Phi_B)}{\mathrm{d}W_m} \right| \tag{20}$$

where $q\Phi_B$ is the SBH, and S characterizes the efficacy of modulating the SBH via W_m. The values of S range from 0 to 1. A value of $S = 1$ corresponds to the ideal Schottky–Mott limit, where the barrier is fully tunable by the work function, while $S = 0$ indicates strong FLP, where the barrier becomes completely independent of the metal choice. Reported pinning factors for conventional semiconductors are approximately 0.3 for Si, 0.1 for GaAs, and 0.05 for Ge [72], reflecting varying degrees of FLP. In their study reported in 2025, Yu et al. integrated domain knowledge with machine learning to derive compact and physically interpretable descriptors for SBH. Their work introduced a physically grounded Schottky barrier factor (δ), which couples the interfacial work function difference (ΔW_F) with the electronegativity mismatch ($\Delta\chi$). This factor overcomes the limitations of the FLP model, accurately predicts the SBH of metal–2D semiconductor interfaces, and extends the applicability of the Schottky–Mott rule to atomic-scale 2D material systems [73].

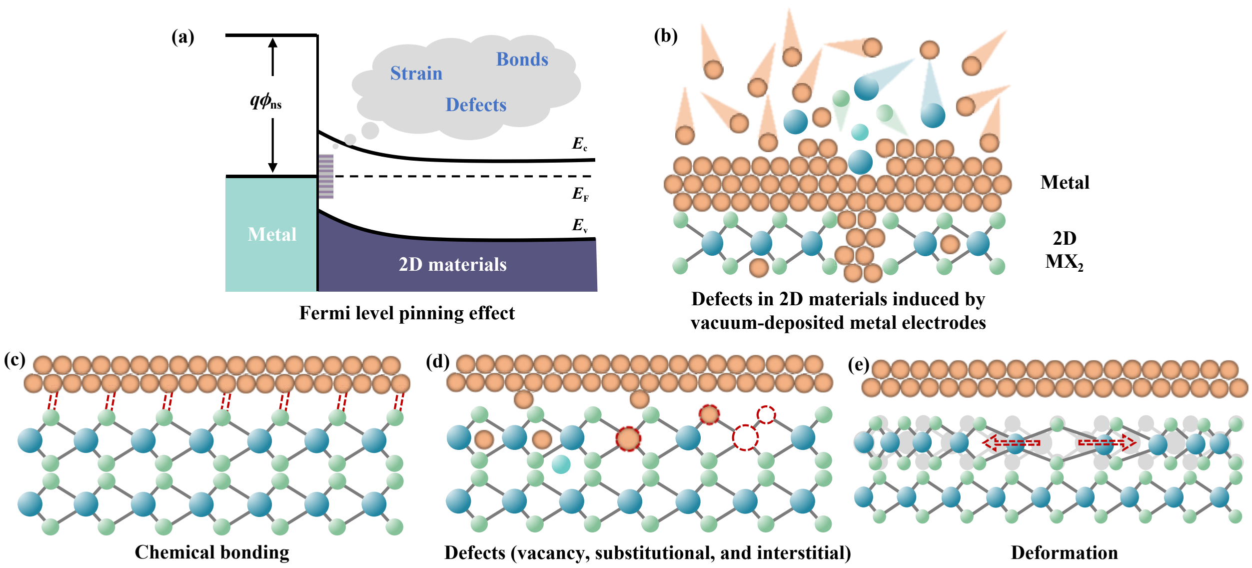


Figure 5 Origins of FLP at 2D material–metal contact interface. (a) Energy band diagram illustrating the FLP phenomenon. Interface states introduced within the bandgap due to various factors (e.g., lattice deformation, chemical bonding, and intrinsic defects) lead to the pinning of E_F. (b) The deposition of metal electrodes by physical vapor deposition method causes energetic metal particle bombardment, which disrupts the atomic lattice of the underlying 2D materials. All the mechanisms depicted in ((c)–(e)) contribute to the generation of interface states, which collectively result in the FLP effect as conceptualized in (a). (c) Reactive metals (e.g., Ti and Al) can form chemical bonds with 2D materials. (d) Various defect types, including vacancies, substitutional impurities, and interstitial atoms, are prevalent in 2D systems. (e) Metal contact can induce localized strain in 2D materials. The yellow balls represent metal atoms, and the green ball stick model represents two-dimensional materials. The dotted balls represent atomic vacancy defects. The dotted arrow indicates the direction of stress.

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The underlying causes of the FLP effect are multifaceted and can be analyzed from the following specific aspects.

3.4.1 Interfacial chemical reaction induceing FLP

Chemical interactions at 2D materials–metal contact interfaces can lead to the formation of new chemical bonds (Fig. 5(c)), which significantly alter the interface properties [74]. These reactions can disrupt the ideal Ohmic contact, modify the local electronic structure, and induce FLP [75].

Experimental evidence for such interactions is provided by the Ti-MoS_2 system. In 2019, Freedy et al. constructed Au/Ti/TiO_x/MoS_2, Au/Ti/MoS_2, and Au/TiO_x/MoS_2 (x denotes a non-fixed oxygen stoichiometry, which is generally $1 \leq x \leq 2$) devices for comparative analysis using X-ray photoelectron spectroscopy (XPS) combined with *in situ* Ti film deposition [76]. Under ultra-high vacuum conditions, the direct deposition of Ti film onto MoS_2 induced new chemical states, as evidenced by the appearance of metallic Mo (Mo^0) at 227.5 eV in the Mo^{3d} spectrum and Ti–S bonds in the S^{2p} spectrum. This confirms a substantial interfacial reaction during deposition. The resulting chemical bonds introduce gap states that lead to strong FLP. In contrast, when a TiO_x interlayer was introduced, the Mo–S bonds remained intact, and a significant Fermi level de-pinning effect was observed. This contrast underscores the pivotal role of direct chemical bonding in FLP.

Theoretically, first-principles calculations by Zhang et al. in 2022 provide further insight into the adsorption behavior of MoS_2 on different metal substrates [77]. Their work revealed that on a Ti substrate, MoS_2 undergoes chemical adsorption, which distorts its electronic structure and pins the E_F at approximately 0.54 eV below the conduction band minimum. In contrast, the adsorption on an Au substrate is primarily physical, inducing minimal disturbance to the electronic structure of MoS_2. This theoretical study corroborates the experimental findings, demonstrating that interfacial chemical bonding is a direct cause of FLP, and suggests that its mitigation can be achieved by selecting metals that favor the non-reactive and physical adsorption.

3.4.2 Defects of 2D materials induceing FLP

Intrinsic defects in 2D materials, including vacancies, substitutional impurities, and interstitial atoms (Fig. 5(d)), serve as a significant origin of FLP. The synthesis, transfer, and post-processing stages of 2D materials inevitably introduce such defects, which disrupt the perfect crystalline order. These defects create localized electronic states within the bandgap, which act as charge trapping centers and ultimately lead to FLP. Furthermore, the deposition of metal electrodes, a standard step in device fabrication, can exacerbate this issue. The deposition process often induces additional lattice damage (Fig. 5(b)), thereby introducing more defect states at the interface [78]. This synergy between intrinsic and process-induced defects strongly pins E_F and consequently elevates R_C, posing a fundamental challenge for achieving high-performance electronic devices.

In 2017, Bampoulis et al. systematically investigated the influence of defects on charge carrier transport in MoS_2 [79]. Using conductive atomic force microscopy (C-AFM), they quantified the density of subsurface metal-like defects at approximately 10^{11} cm^{-2}. These defects were found to induce a negative ionization of the outermost sulfur complex, which subsequently dominated the charge transport mechanism across the MoS_2/metal contact interface. This defect-mediated transport led to a significant FLP, fixing E_F at approximately 0.25 eV below the conduction band minimum. The predominant defect types identified were sulfur vacancies, molybdenum vacancies, and Mo-substitutional antisite defects. The strength of FLP was quantitatively assessed using the pinning factor (S). Measurements revealed a pinning factor of 0.3 in the pristine regions of MoS_2, which decreased sharply to 0.1 in the defect-rich regions. This pronounced FLP effect induced by defects was directly linked to a substantial reduction in the SBH. Specifically, the SBH in the defect regions was observed to be approximately 30%–50% lower than that in the pristine regions.

In 2022, Sun et al. further investigated the FLP effect in germanium sulfide (GeS) by measuring its SBH using C-AFM with probes of distinct work functions, namely Pt, n-Si, and p-diamond [80]. Despite the significant variation in probe work functions, the measured SBH remained nearly constant, with values of 0.41 ± 0.03, 0.40 ± 0.03, and 0.36 ± 0.03 eV, respectively. This clear deviation from the ideal Schottky–Mott rule provides direct experimental evidence for a strong FLP effect in GeS. The authors attributed this pronounced pinning primarily to the presence of charged defects and impurities within the material.

Utilizing a high-throughput computational screening framework, Ha and Giustino identified monolayer WS_2 as a promising ultra-high-mobility semiconductor in 2024 [81]. Their analysis revealed that intrinsic defects in 2D TMD materials, including sulfur vacancies, tungsten vacancies, W/S antisite defects, and substitutional oxygen defects, generate localized acceptor states near the valence band maximum. The presence of these defect states was shown to induce strong FLP, which consequently degraded the carrier mobility from its theoretical upper limit of 1342 $cm^2 \cdot V^{-1} \cdot s^{-1}$ to a calculated value of 509 $cm^2 \cdot V^{-1} \cdot s^{-1}$. This significant reduction underscores how defect-mediated FLP impedes efficient charge transport. Fundamentally, these surface defect states act as electron trapping centers, which not only cause FLP but also deteriorate the quality of the 2D material–metal contact interface, ultimately compromising device performance. Therefore, minimizing the density of such defects is a critical pathway for mitigating the pinning strength and achieving low-resistance Ohmic contacts.

3.4.3 Strain and deformation induceing FLP

External strain and deformation can effectively modulate the energy band structure of 2D materials, providing a versatile means to tailor their electronic and optical properties (Fig. 5(e)). The extreme thinness of these materials makes them exceptionally sensitive to mechanical stress, which can induce significant distortions in the atomic lattice. These structural changes subsequently modify the electronic band structure, leading to shifts in band alignment at heterointerfaces. Specifically, the energy positions of the conduction band minimum (CBM) and valence band maximum (VBM) can be redistributed, thereby altering key material parameters.

Such strain can be introduced during various fabrication and processing steps, including growth, transfer, annealing, and metal contact deposition. For instance, in chemical vapor deposition (CVD), residual strain often arises at the contact interface between the 2D material and the substrate due to a mismatch in thermal expansion coefficients or disparities in lattice constants. The resulting strain can substantially influence the E_F and related electronic properties, an effect that must be carefully considered in device design and analysis.

In 2016, Song et al. applied strain to 2D $MoTe_2$ films using the tip of an AFM, which induced a transformation of the 2H phase into 1T′ phase and significantly enhanced electrical conductivity [82]. This study elucidates the substantial regulatory effect of strain on the electrical properties of $MoTe_2$. In 2018, Zhang et al. examined the strain distribution in the 2D WSe_2–MoS_2 transverse heterojunction and its impact on the electronic structure [83]. The strain resulted in a notable upward shift of the VBM of MoS_2, leading to a transition in the band alignment from the original Type-II to Type-I. This transition represents a modification of the energy band structure induced by strain. In 2014, Desai et al. applied 2% uniaxial stretching to multiple layers of 2D WSe_2 (from 2 to 4 layers) and observed a pronounced increase in photoluminescence (PL) intensity [84]. The maximum amplification factor of PL in bilayer WSe_2 reached 35. This significant enhancement in PL was attributed to the transition from an indirect to a direct bandgap in bilayer WSe_2. Consequently, strain is likely to induce alterations in the band levels at the contact interface.

The strain-induced FLP effect in 2D materials can originate from multiple sources, such as thermal strain during metal deposition, tensile or compressive strain due to lattice mismatch with the substrate, or defect generation within the 2D material under mechanical stress. Therefore, in the development of future 2D material-based devices, controlling or mitigating unintended strain at contact interfaces represents a critical research direction, given its substantial influence on device performance and reliability.

4 Strategic pathways: Engineering ultralow-resistance Ohmic contacts

4.1 vdW electrode contact integration and deposition techniques for interface cleanliness

Achieving ultra-low R_C in devices based on 2D semiconductors remains a significant challenge, largely due to the inherent limitations of conventional metal deposition techniques. Methods such as thermal evaporation and sputtering often cause atomic-scale damage, introduce charge traps, and induce unfavorable chemical reactions at the metal–semiconductor contact interface. To overcome these issues, transferred metal electrode techniques have emerged as a highly promising alternative [19, 22, 47, 85–92]. By physically transferring pre-patterned metal electrodes onto 2D materials, this approach avoids the direct exposure of the material to energetic deposition processes, thereby minimizing contact interface damage and defect generation. Furthermore, the resulting vdW contact between the metal and the semiconductor mitigates FLP effects commonly associated with conventional metal deposition. This enables more tunable and favorable electronic contact, contributing to improved device performance and lower R_C values.

In 2018, Liu et al. [87] made a significant advancement in vdW metal-semiconductor contacts through polydimethylsiloxane (PDMS) stamp-assisted transfer (Fig. 6(a)). Their findings revealed

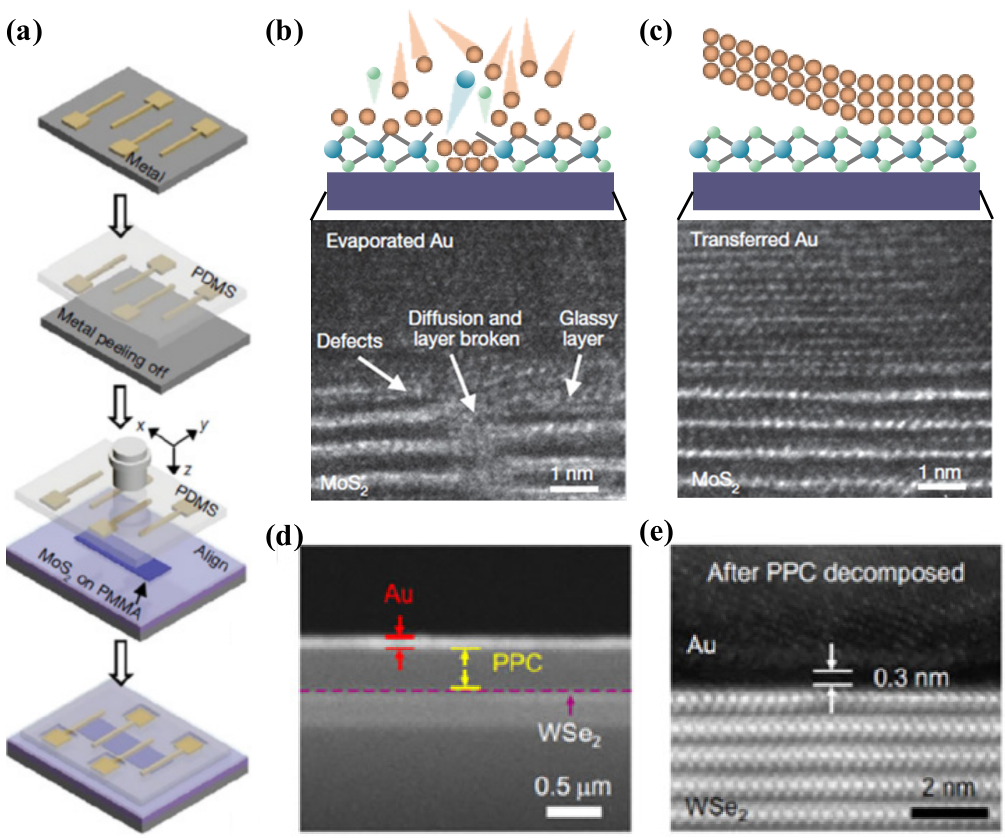

Figure 6 A brief process of transferring metal electrodes onto 2D materials. (a) Schematic diagram of integrated transfer of vdW forces at metal–semiconductor junctions. Reproduced with permission from Ref. [87], © Macmillan Publishers Ltd., part of Springer Nature 2018. (b) Cross-sectional schematic and transmission electron microscopy (TEM) image of the transferred Au electrode on top of MoS_2. (c) Cross-sectional schematic and TEM image of conventional electron-beam-deposited Au electrodes on top of MoS_2. (d) Cross-sectional scanning electron microscopy (SEM) image of WSe_2/PPC/Au tri-layer structure. Reproduced with permission from Ref. [90], © Kong, L. G. et al. 2023. (e) Cross-sectional high-resolution TEM (HRTEM) image of the WSe_2/Au vdW interface after the PPC layer decomposition.

that this contact interface exhibits nearly ideal vdW contact with minimal interface states, significantly suppressing the FLP effect (Figs. 6(b) and 6(c)). Utilizing this technique, the SBH was effectively tuned by selecting metals with different work functions, approaching the Schottky–Mott limit. Furthermore, the use of high-work-function platinum (Pt) as the contact electrode facilitated the fabrication of a p-type MoS_2 FET, a feat that direct deposition processes could not achieve. Building on this, Yang et al. [88] in 2023 reported a highly reproducible vdW integration process for wafer-scale 2D electronics. They designed a quartz/PDMS semirigid stamp and adapted a standard photolithography mask aligner to provide uniform mechanical force and a bubble-free and wrinkle-free interface during pickup/release, enabling large-area, uniform, and damage-free integration of contacts on monolayer MoS_2. This advancement demonstrates that vdW metal contacts are not only suitable for device-level applications but also scalable for semiconductor manufacturing.

During electrode transfer and vdW contact formation, polymers play a crucial role as support media. However, residual polymers can lead to interface contamination, which degrades contact performance. These residual materials introduce charge trap sites, unintended doping effects, and scattering centers, ultimately increasing R_C and compromising device stability and reliability. To mitigate this issue, Nakatani et al. [47] in 2024 developed a functional tape with adhesive force that is tunable by ultraviolet (UV) light, enabling solvent-free dry transfer of 2D materials. The UV-tunable tape achieves a high transfer yield (> 99%) and can transfer large-area monolayer graphene and other 2D materials (including TMDs and hexagonal boron nitride (hBN)) onto a variety of target substrates. In 2024, Choi et al. [92] demonstrated a residue-free transfer approach using polypropylene carbonate (PPC) as the supporting medium for monolayer TMDs. By incorporating atomically clean PPC-transferred monolayer MoS_2 with semimetal bismuth contacts on h-BN substrates, they achieved an ultralow Ohmic R_C (~ 78 Ω·μm, approaching the quantum limit) and record-high on/off current ratios (~ 10^{11} at 15 K) with negligible PPC residue coverage (~ 0.08%) across centimeter-scale films. These results underscore the importance of residue-free transfer processes for minimizing interface contamination and enabling high-performance TMD FETs, and suggest pathways toward clean and scalable integration techniques for 2D device technologies.

Achieving large-area and defect-free vdW metal integration remains a significant challenge, primarily due to the necessity of maintaining mechanical and structural integrity during the transfer process. Transferring electrodes must establish uniform, crack-free, and wrinkle-free contacts with the 2D semiconductor surface while avoiding contamination that could impair device performance. Structural defects such as wrinkles, cracks, and residues introduce local strain and charge inhomogeneities, leading to variations in R_C and degraded transistor electrical characteristics. In 2024, Zhang et al. [85] developed an all-stacking transfer method based on the quasi-vdW epitaxial growth of metals on fluorophlogopite mica (F-mica), enabling the mechanical peeling and deterministic stacking of pre-patterned metal electrodes onto 2D materials to form high-quality vdW contacts. The wafer-scale applicability of the method was demonstrated by transferring arbitrarily patterned metal electrodes from F-mica with nearly 100% yield onto 2D semiconductors. In 2019, Jung et al. [89] demonstrated a transferred-via-contacts (TVC) fabrication platform in which metal electrodes are embedded within insulating hBN and then dry-transferred onto 2D semiconductors, avoiding direct metallization on the sensitive 2D channels. This approach preserves the pristine semiconductor surface, suppresses deposition-induced damage, and yields ultra-clean vdW metal-semiconductor interfaces, enabling high-quality 2D FETs.

Another promising strategy for achieving defect-free vdW metal-semiconductor contact interfaces involves incorporating buffer layers to physically decouple metals from 2D materials. In 2022, Kwon et al. [22] showed that depositing an ultrathin selenium (Se) buffer layer before metal deposition enables the formation of interaction- and defect-free vdW contacts between metals and 2D semiconductors, thereby addressing strong FLP seen in conventional metal–semiconductor junctions. Devices fabricated with such Se-mediated vdW metal contacts exhibit low R_C, high on/off ratios, and mobility improvements compared with direct metal contacts, along with stable electrical characteristics. Similarly, Kong et al. [90] in 2023 demonstrated a wafer-scale and universal strategy for forming vdW metal–semiconductor contacts by introducing PPC as a sacrificial buffer layer during metal deposition (Figs. 6(d) and 6(e)). In this process, PPC is deposited between the metal and 2D semiconductor, subsequently volatilizing upon heating to eliminate direct interaction between the metal and semiconductor. This approach enables high-quality deposition of various metals on both 2D transistors and conventional bulk semiconductors, resulting in vdW contacts with suppressed FLP. In 2025, Zhang et al. [93] proposed a selenium-mediated dry transfer strategy that enables clean and damage-free migration of wafer-scale two-dimensional semiconductors from growth substrates to target wafers (Fig. 7(a)). By introducing a weakly interacting selenium interlayer as a sacrificial release medium, this approach eliminates the chemical contamination and polymer residues inherent to conventional wet transfer processes while preserving wafer-scale mechanical integrity. Importantly, this fully dry process is fully compatible with standard semiconductor fabrication, providing a viable pathway for the scalable integration of 2D materials into advanced electronic platforms.

Beyond buffer layers, significant progress has been made in optimizing deposition conditions to minimize process damage during metal contact formation. In 2021, Kim et al. [94] demonstrated that evaporating indium (In) onto MoS_2 at a substrate temperature cooled to ~100 K by liquid nitrogen produces ultraclean vdW contacts with MoS_2, giving rise to Ohmic-like charge transport dominated by field emission over a wide temperature range (2.4–300 K). First-principles analysis reveals that the presence of strong in-gap states at the interface underlies the near-Ohmic behavior while mitigating Fermi-level pinning. Concurrently, vacuum conditions prove essential for achieving high-quality metal-semiconductor interfaces. For instance, Sun et al. [91] in 2024 demonstrated that ultrahigh-vacuum (UHV) deposition of Ni contacts (~ 3 × 10^{-11} mbar) on monolayer MoS_2 yields significantly lower R_C than comparable high-vacuum depositions (~ 3 × 10^{-6} mbar) by minimizing interfacial reaction and defect formation during metal deposition, as confirmed by surface analysis. Under UHV conditions, Ni/MoS_2 field-effect transistors achieve R_C values as low as ~ 500 Ω·μm, approximately five times lower than under high-vacuum deposition, correlating with stronger interfacial bonding features observed via XPS.

2D semiconductors offer a viable pathway for device scaling and mitigation of short-channel effects. However, many promising materials, including black phosphorus (BP) and germanium arsenide (GeAs), remain challenging to implement as monolayer transistors, owing to a combination of processing-induced instability and contact formation difficulties. Conventional contact fabrication processes, such as photolithography and metal evaporation, readily damage monolayer channels, while thickness-dependent bandgap widening tends to increase SBH and R_C. In 2023, Li et al. [95] introduced a vdW channel thinning strategy, in which the channel region is mechanically thinned layer-by-layer down to monolayer thickness while preserving multilayer contact regions, thereby minimizing structural damage and mitigating R_C (Fig. 7(b)). This approach enabled a systematic investigation of thickness-dependent transport properties within the same device architecture. The results revealed a pronounced degradation of BP mobility with decreasing thickness, from ~ 100 $cm^2 \cdot V^{-1} \cdot s^{-1}$ in multilayer devices to ~ 1 $cm^2 \cdot V^{-1} \cdot s^{-1}$ in monolayers, whereas GeAs exhibited comparatively weak thickness dependence. This methodology is broadly applicable to structurally unstable two-dimensional semiconductors, providing a platform for probing their intrinsic monolayer transport properties.

4.2 Optimization of the contact area

Contact engineering, as the critical bridge connecting 2D materials to 3D systems, has become central to exploring the electronic properties of 2D materials. Currently, interface activation layers and process innovations offer viable solutions for the uniform deposition of high-κ oxides (materials with a higher dielectric constant (κ) than silicon dioxide (SiO_2, $\kappa \approx 3.9$)) on 2D materials, encompassing surface chemical pretreatment and seed layer introduction techniques (Fig. 8(a)). For instance, Li et al. [96] in 2019 employed a perylene-3,4,9,10-tetracarboxylic dianhydride (PTCDA) monolayer molecular crystal as a seeding layer to enable the atomic layer deposition of ultrathin high-κ gate dielectrics on 2D materials (Fig. 8(b)). By using PTCDA to promote nucleation, HfO_2 films with equivalent oxide thickness down to ~ 1 nm and reduced roughness, interface state density, and leakage current were obtained on graphene, MoS_2, and WSe_2, yielding dielectrics with high breakdown fields and excellent uniformity suitable for low-power devices. The resulting transistor devices show enhanced performance, evidencing the effectiveness of the molecular seed layer in achieving high-quality 2D dielectric interfaces (Fig. 8(c)).

In 2D semiconductor devices, regulating metal–semiconductor contact characteristics through interfacial doping has become a core strategy for reducing R_C (Fig. 8(d)). However, conventional ion implantation techniques pose risks of atomic-level damage and significant mobility degradation, rendering them unsuitable for atomically thin material systems. Consequently, alternative approaches such as surface charge transfer doping, metal-induced doping, and defect engineering have been extensively investigated. These methods enhance carrier injection while effectively preserving the intrinsic electronic properties of 2D semiconductors. One highly efficient doping strategy involves utilising metal oxides to induce surface charge transfer at interfaces. For instance, McClellan et al. [97] in 2021 reported that low-temperature (< 200 °C) sub-stoichiometric AlO_x deposited on monolayer MoS_2 provides a stable n-type doping layer compatible with complementary metal–oxide–semiconductor (CMOS)-process integration, achieving carrier concentrations exceeding ~ 2 × 10^{13} cm^{-2} and R_C of approximately ~ 480 Ω·μm in field-effect transistors. Devices with this AlO_x-induced doping exhibit high current densities approaching ~ 700 $\mu A \cdot \mu m^{-1}$ (> 110 $MA \cdot cm^{-2}$)

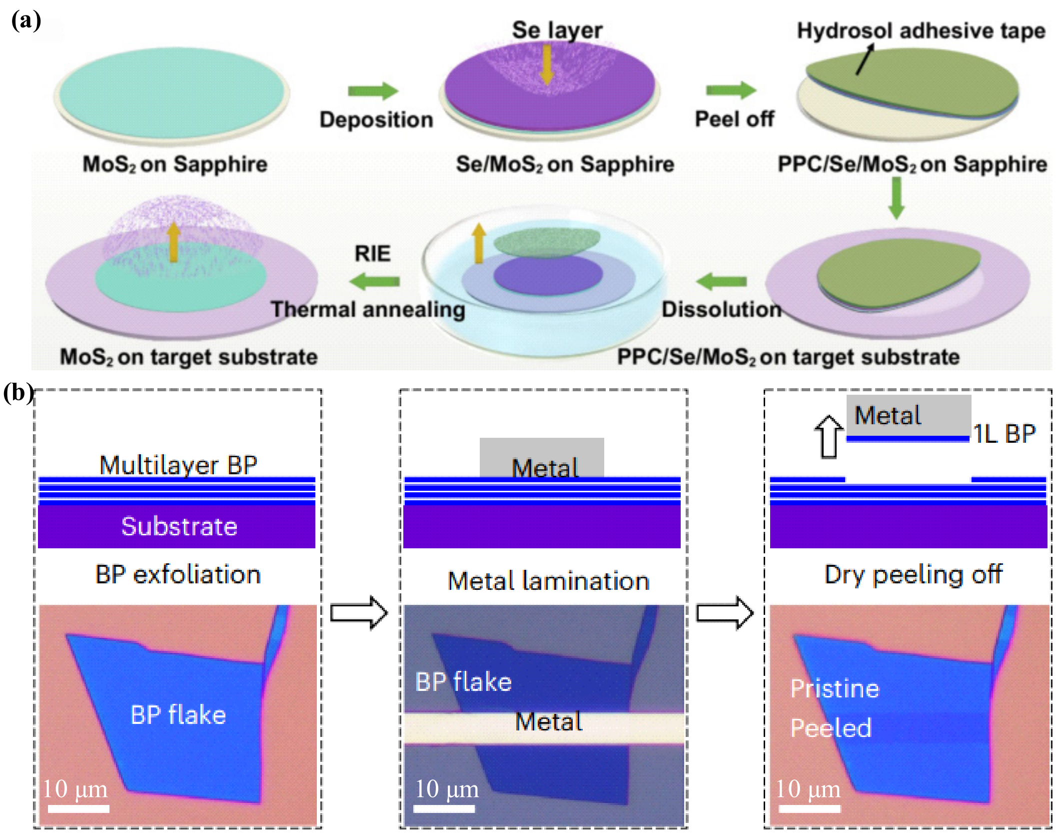

Figure 7 A brief process of transferring metal electrodes onto 2D materials. (a) The schematic of the Se-mediated transfer process for wafer-scale MoS_2.Reproduced with permission from Ref. [93], © Zhang, X. C. et al. 2025. (b) Fabrication processes for vdW peeling of BP. Reproduced with permission from Ref. [95],© Li, W. Y. et al. 2023.

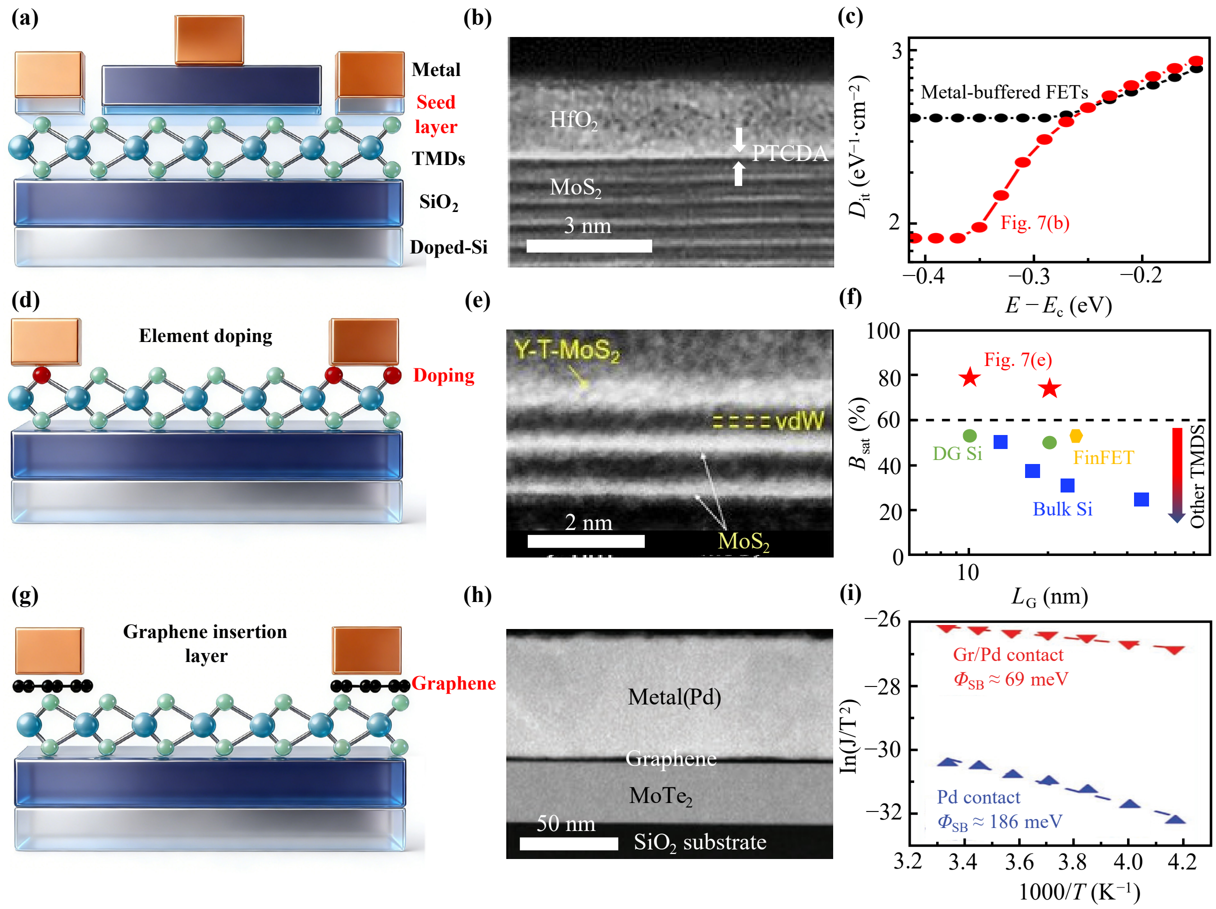

Figure 8 Optimise contact areas to enhance contact quality. (a) Introduction of a seeding layer for contact integration or improving contact quality. (b) Bright-field cross-sectional scanning TEM (STEM) image of ML PTCDA/HfO_2 on MoS_2. Reproduced with permission from Ref. [96], © Li, W. S. et al. 2019. (c) This distribution as a function of energy below the conduction band ($E - E_c$) from a typical MoS_2 FET with equivalent oxide thickness (EOT) = 2.1 nm. (d) Doping of the contact region or pretreatment of the interface. (e) Cross-sectional STEM images and electron energy loss spectroscopy (EELS) maps of Y-doping-induced phase-transition in trilayer MoS_2. Reproduced with permission from Ref. [107], © Jiang, J. F. et al. 2024. (f) Benchmarking the room-temperature ballistic ratios of MoS_2 FETs with those of short-channel FETs. (g) vdW integration process. (h) Dark-field STEM images of $MoTe_2$/Gr/Pd interface via graphene-enhanced vdWs integration (GEVI). Reproduced with permission from Ref. [101], ©Wiley-VCH GmbH 2023. (i) SBH of $MoTe_2$/Pd and $MoTe_2$/Gr/Pd.

while maintaining high on/off current ratios (> 10^6) and low off-currents, demonstrating exceptional performance metrics for low-power and high-current two-dimensional electron applications. Similarly, Lee et al. [98] in 2023 investigated how oxygen (O_2) plasma treatment followed by an aging process modulates metal–semiconductor interface properties in WSe_2 FETs. After plasma treatment and subsequent vacuum aging, the pinning factor (S) for holes decreases significantly. The study further shows that the enhanced p-type behavior and modified tunneling characteristics differ with contact metals (Pd vs. In). Fa et al. [99] reported that reverse sputtering-induced structural modification in the contact regions of MoS_2 FETs can effectively reduce R_C by inducing conductive 1T-MoS_2 phase at the metal–MoS_2 interface. Under optimized reverse sputtering conditions, the R_C was reduced to less than half compared with untreated contacts, translating into enhanced on-state currents and overall improved transistor performance.

CVD-grown graphene electrodes support large-scale CMOS-compatible fabrication. For instance, the diffusion-limited CVD method developed by the Yeh's group [100] enables site-selective growth of WS_2/WSe_2 on pre-patterned graphene substrates. The graphene-enhanced vdW integration technique proposed by the Qi's group [101] achieves nanometre resolution and nearly 100% device success rate through physical transfer of monolayer graphene/3D metal heterojunctions (Fig. 8(h)). Fitting the curves with a thermionic emission model yielded SBH of approximately 186 and 69 meV for $MoTe_2$/Pd and $MoTe_2$/Gr/Pd, respectively (Fig. 8(i)), indicating that graphene reduces the electronic Schottky barrier between n-type $MoTe_2$ and Pd contacts. However, this technique requires addressing issues such as small-scale electrode alignment precision, high-temperature process stability, and multi-step integration defects.

Semimetallic materials (e.g., Sc, Sb, and Sn) as contact electrodes effectively suppress MIGS and reduce the SBH (Fig. 9(a)). In 2021, Shen et al. [21] discovered that orbital resonance and near-zero-state density between Bi metal and 2D MoS_2 reduced the R_C of Bi-MoS_2-FETs to 123 Ω · μm at a carrier concentration of 1.5×10^{13} cm^{-2}. In 2023, Li et al. [102] further confirmed Sb metal's highly matched band structure with 2D MoS_2 (Fig. 9(b)), enhancing interface coupling via vdW forces to achieve an R_C as low as 42 Ω · μm with markedly improved thermal stability (performance remained stable after 400 °C annealing) (Fig. 9(c)). Sn metal-based Ohmic contacts also exhibited high on-current density of 480 μA · μm^{-1}, highlighting the potential of semimetals in next-generation 2D electronic

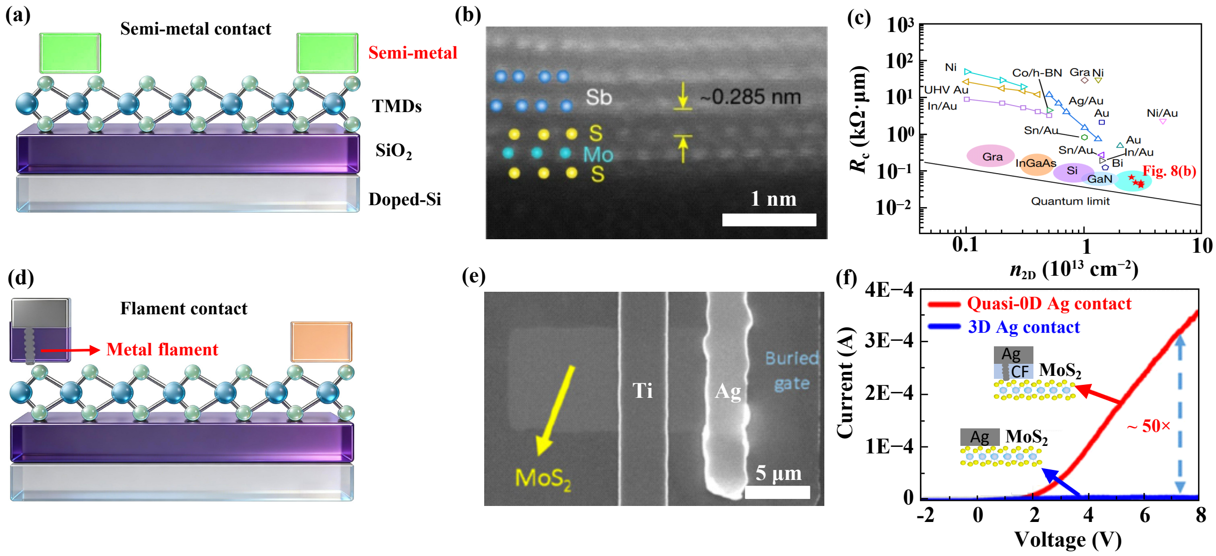

Figure 9 Developing new materials and contact methods to improve contact quality. (a) Development of novel materials such as semi-metal contact. (b) Zoom-in atomic-resolution image of the Sb (0112)–MoS_2 contact. Reproduced with permission from Ref. [102], © Li, W. S. et al. 2023. (c) R_C as a function of n_{2D} for monolayer MoS_2 and other semiconductors in the literature. The black solid line represents the quantum limit for R_C. (d) Flament contact. (e) The SEM image of a single devicele. Reproduced with permission from Ref. [104], © American Chemical Society 2019. (f) The on-current comparison between the traditional 3D contact and quasi-0D contact.

devices. In 2025, Du et al. [30] from Nanjing University achieved epitaxial growth of crystalline antimony contacts on molybdenum disulfide via molecular beam epitaxy, realising a R_C of 98 Ω·μm at a contact length of 18 nm. Using this contact, a scaled FET with a contact gate pitch of 40 nm was fabricated. The drive currents for single-layer, double-layer, and triple-layer MoS_2 channel devices reached 0.85, 0.95, and 1.08 mA·μm^{-1}, respectively. Statistical analysis of the transistor array confirmed the repeatability and stability of the crystalline antimony contact.

An innovative filamentary contact approach has emerged as an effective pathway to achieve subthreshold swing (SS) below 60 mV·dec^{-1} and high on-current (Fig. 9(d)). In 2018, Tian et al. successfully achieved graphene-based filamentary transistors with sub-10 mV·dec^{-1} SS and high on-current [103]. Building upon this, Wang et al. in 2019 proposed a dual-mode MoS_2 filamentary transistor concept (Fig. 9(e)), which has been successfully fabricated at the wafer scale [104]. Mode I achieves an exceptionally low SS of 2.26 mV·dec^{-1} by switching the filament's on/off state, while mode II leverages the filamentary structure as a quasi-zero-dimensional (0D) contact, attaining a record-breaking on/off current ratio of 2.6×10^9. Under identical measurement conditions, the on-current of quasi-zero-dimensional Ag–C contact transistors increased nearly fiftyfold (Fig. 9(f)), demonstrating the superior contact properties of quasi-zero-dimensional structures.

Edge contact technology employs O_2/CHF_3 plasma etching to deposit metal leads at the edges of hBN-graphene-hBN stacks, enabling efficient carrier injection and reduced resistance (Fig. 10(a)). Yang's team [105] employed high-work-function metals (e.g., Pd and Au) to construct MoS_2 one-dimensional edge contacts, enabling precise polarity control of n-type/p-type transistors. In 2022, Xiao et al. employed a clean terminal-bonding approach, yielding size-independent electrodes and an ultra-low R_C of 2.5 kΩ · μm (Fig. 10(b)) [106]. The output characteristics of MoS_2 FETs with top-contact and edge-contact configurations were measured as a function of back-gate voltage at room temperature. The top-contact device exhibits pronounced nonlinearity in its output characteristics, consistent with a Schottky contact effect. In contrast, the edge-contact FET shows nearly linear behavior at high gate voltages (50 V), indicative of Ohmic contact between the metal and the MoS_2 edge (Fig. 10(c)).

The vdW contacts between 2D semiconductors and metals have historically lagged behind the covalently bonded contacts used in the semiconductor industry, owing to their weak band coupling and limited interfacial bonding strength. In 2025, Gao et al. [74] from the University of Science and Technology Beijing introduced an atomic layer bonding (ALB) contact that enables strong band hybridization and high interfacial cohesion (Fig. 10(d)). This was achieved by forming a coherent metallic bonding interface between the exposed transition-metal atomic layer of transition metal dichalcogenides and the metal electrode (Fig. 10(e)). As a result, the ALB contact exhibits ultra-low R_C and exceptional thermomechanical stability, approaching the performance metrics of conventional covalently bonded contacts and representing one of the best-performing contact schemes reported to date. For monolayer MoS_2/Au junctions, an R_C of ~ 70 Ω·μm was achieved, together with thermomechanical stability up to 400 °C. After high-temperature annealing, the devices delivered a maximum on-current of 1.1 mA·μm^{-1}, highlighting the strong potential of ALB contacts for scalable and industrially relevant 2D device integration (Fig. 10(f)).

4.3 The scope and applicability of the contact-engineering strategies

The strategies discussed above demonstrate significant potential for achieving ultralow-resistance contacts in 2D material devices. However, translating these laboratory advances into practical and scalable technologies requires careful consideration of manufacturing constraints, operational reliability, and integration with existing semiconductor infrastructure.

4.3.1 Scalability of vdW integration

The most successful strategies for ultralow-resistance contacts (e.g.,

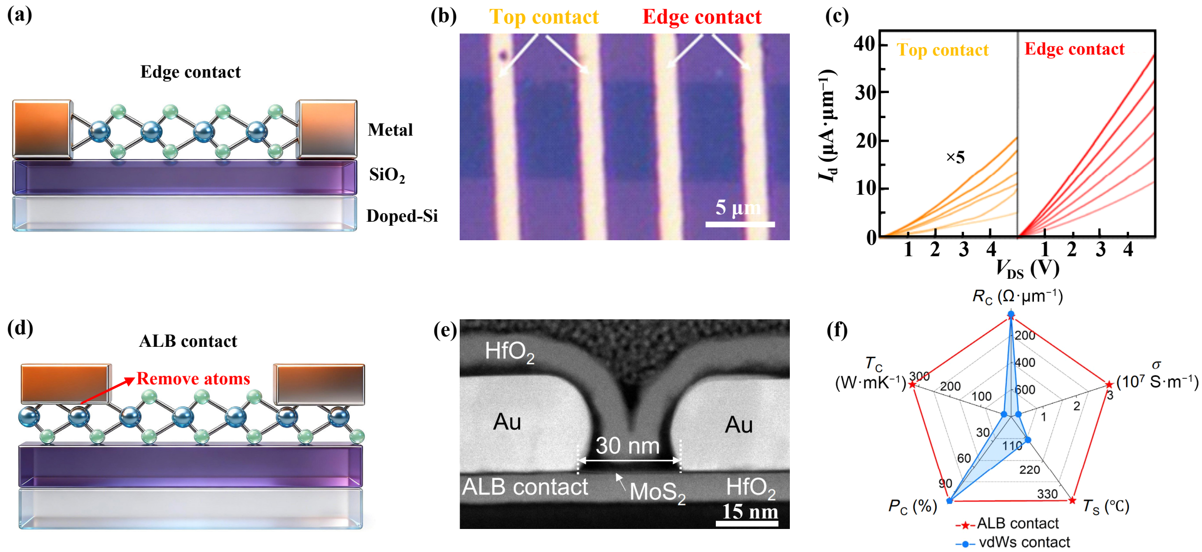

Figure 10 Developing new materials and contact methods to improve contact quality. (a) Edge contact. (b) Optical image of top-contacted MoS_2 FET and edge contacted MoS_2 FET on the same MoS_2 strip. Reproduced with permission from Ref. [106], © Tsinghua University Press and Springer-Verlag GmbH Germany, part of Springer Nature 2021. (c) Output characteristics of the top-contacted MoS_2 FET and edge contacted MoS_2 FET. (d) ALB contact. (e) Cross-sectional TEM image of a 30 nm short channel MoS_2 FET. Reproduced with permission from Ref. [74], © Gao, L. et al. 2025. (f) Radar plot of ALB contact versus Sb vdW contact, benchmarked against industrial-grade contact performance. P_C, process compatibility; σ, electrical conductivity (S·m^{-1}); T_C, thermal conductivity (W·mK^{-1}); T_S, thermomechanical stability (°C).

edge contacts) are often incompatible with mainstream Si-CMOS fabrication flows. A primary obstacle to industrialization is developing high-throughput and high-yield patterning and integration techniques that reconcile 2D material contact engineering with existing semiconductor production lines. While vdW electrode integration offers pristine interfaces free from deposition-induced damage, current transfer techniques (mechanical exfoliation and deterministic placement) remain fundamentally limited in throughput. For example, the manual nature of dry transfer processes yields placement accuracies of ~ 1 μm, insufficient for sub-10 nm node alignment requirements in advanced logic. For contact area optimization, edge-contact geometries require precise lithographic definition of sub-100 nm features atop atomically thin channels, demanding step-edge roughness below 1 nm to prevent contact discontinuity-specifications challenging for current industrial patterning tools when applied to fragile monolayers.

4.3.2 *Stability and reliability concerns*

The long-term stability of the metal–2D material interface under electrical stress, thermal stress, or environmental exposure is a critical issue. Interfacial diffusion, oxidation, or chemical reactions can lead to degradation of R_C over time, affecting device lifetime. For strategies based on interface dipole engineering or defect engineering, the long-term stability of their effects requires systematic evaluation. For example, encapsulation strategies (e.g., hBN capping layers) mitigate degradation but complicate subsequent processing steps and electrical access. And the FLP mechanisms (interfacial reactions, defects, and strain) evolve dynamically under electrical stress.

4.3.3 *Performance uniformity and cost*

While pursuing extreme R_C, it is essential to balance other metrics such as performance uniformity across the wafer, device on/off ratio, and subthreshold swing. Furthermore, many strategies involve precious metals (e.g., Pd and Pt) or complex equipment and process steps, making cost-effectiveness an unavoidable consideration in practical applications. For instance, ALD of interfacial oxides offers angstrom-level precision but requires vacuum processing that increases production costs. Future work should focus on developing robust and reproducible processes that can be integrated with roll-to-roll or large-area deposition techniques.

5 Challenges and perspectives

5.1 Critical unresolved issues in contact engineering

Despite significant progress, contact engineering remains a central challenge for the practical adoption of 2D electronics. The intrinsic environmental sensitivity of 2D materials (where their electronic and interfacial properties are strongly influenced by dielectrics, adsorbates, and adjacent layers) poses a fundamental barrier to the stable and reproducible realization of well-controlled Schottky or Ohmic contacts, often leading to deviations of device performance from theoretical predictions. Several critical issues still require systematic resolution. Firstly, achieving stable and low-resistance Ohmic contacts in scalable manufacturing remains a major bottleneck for commercialization. Although strategies such as vdW integration and edge contacts show promise in laboratories, their compatibility with conventional silicon-based processes and their reproducibility at the full-wafer scale have not been adequately verified. Secondly, the physical origins of FLP and universal methods for its modulation still lack a clear theoretical framework, leaving interface design largely dependent on empirical trial-and-error. Furthermore, there is a lack of systematic understanding regarding the enhanced effects of quantum confinement, tunneling behavior, and MIGS at extreme scaling limits, such as the sub-1 nm node. Finally, for the contact properties of diverse 2D materials (including semiconductors, semimetals, and magnetic materials), no unified theoretical model yet exists to guide the development of universal contact strategies, which limits the diversified development of heterogeneously integrated 2D devices.

To address these challenges systematically, a shift toward a holistic and co-optimized research strategy is essential, advancing across three interconnected fronts: At the fundamental level, contact design must transition from empirical optimization to theoretically informed prediction by integrating *operando* characterization techniques (which enable real-time analysis under operating conditions) with unified multi-scale theoretical models capable of accurately describing charge injection across material combinations, thereby building a precise knowledge framework for interface control. At the material innovation level, moving beyond conventional metal electrodes to explore next-generation electrode and interlayer materials (such as tailored alloys, 2D conductors (e.g., graphene and MXenes), and functional layers (e.g., ferroelectrics)) is crucial for enabling dynamically tunable Schottky barriers or ultraclean vdW interfaces. At the integration level, prioritizing scalable and damage-free integration techniques (including wafer-compatible area-selective atomic deposition, clean vdW integration of pre-patterned electrodes, and advanced direct patterning methods) is vital to transition the technology from laboratory demonstrations to industrial manufacturing. Ultimately, through interdisciplinary collaboration, a clear path can be paved toward performance breakthroughs and large-scale application of 2D electronic devices.

5.2 Application-specific contact engineering for 2D materials: From low resistance to functional customization

Application-specific interface engineering is emerging as a crucial direction in contact research for 2D materials. Moving forward, generic contact solutions will be insufficient to meet the extreme performance requirements of diverse devices, necessitating customized design and optimization tailored to specific application scenarios. For instance, in ultra-scaled logic transistors, the core challenge lies in achieving record-low contact resistivity, which requires the development of atomically precise interfaces that simultaneously ensure ultralow Schottky barriers and highly efficient tunneling injection. For flexible and wearable electronics, interfaces must exhibit excellent mechanical resilience and strain stability, maintaining reliable electrical contacts under repeated bending, driving the design of flexible contacts based on low-dimensional materials or adaptive structures. In quantum devices, such as spin qubits or topological circuits, the primary requirement shifts toward preserving the coherent quantum properties of carriers, minimizing decoherence caused by interfacial scattering, magnetic disturbances, or charge noise. Therefore, future contact engineering must transcend the singular paradigm of “low resistance” and evolve toward multifunctional and customizable solutions that are deeply co-optimized with end-use applications, thereby unlocking the full potential of 2D material devices across various fields.

5.3 Towards standardized fabrication and metrology

Establishing standardized fabrication processes and metrology is a crucial prerequisite for advancing 2D material contact technology from the laboratory to industrialization. Currently, the evaluation of contact performance (e.g., contact resistance and Schottky barrier height) is highly dependent on specific device geometries, measurement conditions, and extraction methodologies, leading to poor comparability of data across different studies. Therefore, there is an urgent need for collaborative efforts between industry and academia to develop a set of standard testing protocols and benchmark device structures to enable reliable and comparable characterization of interface properties.

On the fabrication front, it is necessary to develop integration processes compatible with mainstream semiconductor production lines that can maximally preserve the intrinsic properties of 2D materials, such as low-temperature, damage-free metal deposition, and patterning techniques. Simultaneously, establishing standards for *in situ*, high-spatial-resolution characterization of interfacial atomic structure, chemical states, and band alignment is paramount for building accurate process-performance correlations. Ultimately, by promoting standardization in fabrication and metrology, a solid and reliable foundation can be provided for material screening, process optimization, and device modeling, thereby accelerating the maturation and application of 2D electronics technology.

5.4 Roadmap for next-generation 2D electronic and optoelectronic devices

In the roadmap for next-generation 2D electronic and optoelectronic devices, the concept of “the interface is the device” has emerged as a core design paradigm. The 2D material itself can be viewed as a functional “special interface”, where its atomic thickness merges surface and bulk properties. Simultaneously, the contact interface between the 2D material and the metal electrode constitutes another decisive “special interface”. This dual interfacial characteristic fundamentally reshapes the physical mechanisms and functional potential of devices. Future device design and functional development must, therefore, prioritize the precise engineering of 2D material–metal contacts as a primary strategic focus. This necessitates moving beyond traditional Ohmic contact optimization toward constructing intelligent, dynamic, and multifunctional contact systems, such as utilizing ferroelectric interlayers for non-volatile Schottky barrier modulation or employing phase-change materials to create optically/electrically programmable contact logic. At the application level, breakthroughs in this interfacial engineering will directly accelerate the practical adoption of 2D materials in cutting-edge fields, including ultra-low-power transistors, high-performance photodetection and modulation-integrated systems, neuromorphic computing, and quantum sensing. Thus, establishing a clear roadmap to systematically advance research across the full spectrum (from fundamental theory and material innovation to process integration) is essential for ultimately realizing a new generation of information devices centered on 2D interfaces.

5.5 Conclusions

The emergence of 2D materials has opened new frontiers for post-Moore’s Law electronics and optoelectronics, yet their atomic thinness introduces a fundamental contact challenge: the ubiquitous formation of a Schottky barrier at the metal–2D interface, leading to high R_C. This review systematically examines the dual nature of this central issue: The Schottky barrier acts both as a bottleneck for conventional transistor performance and as an essential functional element in devices such as photodetectors. We first elucidate the underlying physical mechanisms governing interface behavior, including FLP, charge transfer, interfacial dipole formation, and Schottky barrier modulation, highlighting the limitations of the classical Schottky–Mott rule in 2D systems. We then distinguish two strategic engineering pathways: innovative approaches toward ultralow-resistance Ohmic contacts (such as vdW integration, interfacial doping, and edge contacts) and methods for functional Schottky contact tailoring through barrier-height tuning. Prevalent experimental methods for characterizing R_C and SBH are introduced and evaluated. This discussion aims to deepen the understanding of contact physics in 2D systems and provide actionable insights for device design and fabrication.

Despite remarkable progress, critical challenges remain in 2D contact engineering. Fundamental issues such as material environmental sensitivity, universal control of FLP, and interfacial uniformity in scalable manufacturing require urgent solutions. Future advances demand coordinated efforts across three dimensions: at the fundamental level, developing theoretical frameworks capable of accurately predicting interface behavior; in materials innovation, exploring novel contact materials including 2D conductors and functional interlayers; and in integration technology, creating damage-free fabrication methods compatible with existing semiconductor processes. Importantly, within the new paradigm of "the interface is the device", the 2D material–metal contact is no longer merely an auxiliary connection but has become the core functional component of the device. Through cross-scale and multidisciplinary collaboration and a shift from empirical optimization to rational design, we can fully exploit the unique advantages of 2D materials and establish a solid interfacial foundation for next-generation electronic devices. Ultimately, breakthroughs in 2D contact engineering will not only extend transistor performance scaling but also unlock new opportunities in neuromorphic computing, quantum sensing, and multifunctional integrated systems.

Data availability

Not applicable.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (Nos. 92577101, 52102044, 52372046, and 12322406), the National Key Research and Development Program of China (No. 2022YFA1403503), the Guangzhou Science and Technology Program (No. 2025A04J5461), and the Guangdong Provincial Basic and Applied Basic Research Fund (No. 2023A1515012743).

Declaration of competing interest

All the contributing authors report no conflict of interests in this works.

Author contribution statement

X. Z. X., X. Z., and J. L. conceived the article and supervised the project. Y. P. G., Y. H. M, and C. C. conducted literature research, prepared charts and figures, and drafted the manuscript. L. L. L. contributed to the discussion and manuscript. X. Z. X. , X. Z., and J. L. also contributed to the manuscript. All the authors have approved the final manuscript.

Use of AI statement

None.

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