

High-performance 2D semiconductor floating gate transistors incorporating an ultrathin oxygen layer

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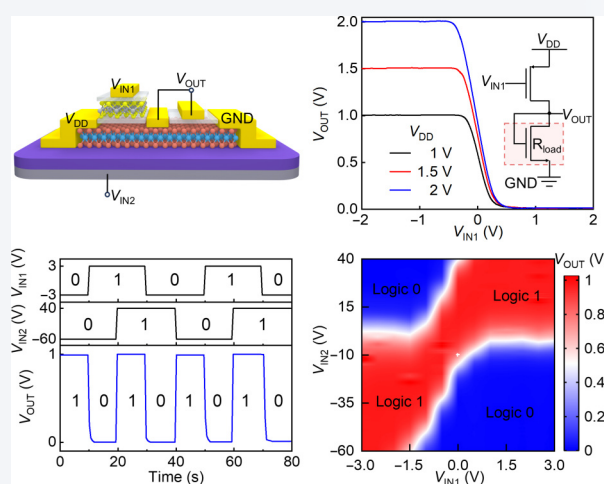
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ABSTRACT: Depositing high-quality tunneling layers for two-dimensional (2D) floating gate transistors remains challenging, as it requires precise process control and parameter optimization. Herein, we fabricated a floating gate structure incorporating a high-quality hafnium oxide (HfO_x) tunneling layer achieved via ozone-induced oxidation of HfS₂ flakes. This process forms a nano-confined elemental oxygen layer at the tunneling layer/channel interface, which effectively suppresses leakage current. As a result, the WSe₂ floating gate transistor exhibits exceptional memory performance, including a high programming/erasing ratio, a long retention time (10⁵ s), multibit storage capacity, and reliable low temperature operation. Leveraging its programmable characteristics and robust performance, we demonstrated logic-in-memory operations with functional NOT, XNOR, and XOR gates. This rationally designed floating gate structure offers a promising approach for high-performance memory devices and logic-in-memory systems.

KEYWORDS: floating gate transistor, logic gates, native HfO_x oxides, van der Waals heterostructures

1 Introduction

Floating gate memory is widely adopted owing to its high data storage capacity and low manufacturing costs [1, 2]. However, integrating an ultrathin tunneling layer into floating gate transistors creates an inevitable trade-off between operating voltage and retention time. A high-quality tunneling layer on a two-dimensional (2D) channel is crucial for ensuring operational



stability and retention performance, as it effectively suppresses leakage current [3–6]. Due to the inert, dangling bond free surface of 2D materials, conventional deposition techniques like atomic layer deposition (ALD) require bonding media (pre-prepared grains) as nucleation sites on 2D crystal surfaces to facilitate chemical bond formation [7–10]. Additionally, oxide dielectrics such as hafnium oxide (HfO_x) are typically amorphous and form degraded dielectric/channel interfaces with high defect densities [11–15]. These defects induce defect-assisted tunneling of storage charges in floating gate structures, undermining device reliability [16–18]. Concurrent electron transitions between defects and tunnel injection toward the floating gate further raise reliability concerns. Although 2D hexagonal boron nitride is commonly used as a gate insulator in transistors, it is unsuitable as a tunneling layer

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due to excessive tunnel currents and inherent fabrication challenges [19–22]. Notably, conduction-electron density in high- κ insulating films can be modulated during electron trapping and detrapping [23, 24]. Thus, depositing a high-quality tunneling layer in floating gate transistors while preserving adjacent 2D channel performance remains a significant challenge.

Our previous work showed that native HfO_x oxides formed via ozone treatment offer a promising strategy for high-performance, low-power electronic devices as gate dielectrics [25]. Building on this, we explored direct transformation of HfS_2 flakes into $\text{HfO}_x/\text{HfS}_2/\text{HfO}_x$ floating gate stacks via ozone treatment. We achieved controlled partial oxidation of top and bottom surfaces of HfS_2 flakes, and then integrated the resulting stacks with WSe_2 to fabricate a floating gate transistor. During oxidation, excess oxygen accumulated at the interface, forming a nano-confined elemental oxygen layer that effectively suppressed leakage current and prolonged charge retention. The fabricated WSe_2 floating gate transistor exhibited a high programming/erasing ratio, long storage retention (10^5 s), multi-bit storage capability, and reliable low temperature performance. This process eliminates the need for invasive dielectric deposition techniques, such as sputtering or atomic layer deposition. Furthermore, configurable logic-in-memory functionality was achieved with multi-gate structures, where programming operations were controlled by the electrostatic potential of the floating gate stack. Benefiting from this design, robust XNOR and XOR output logic sequences were realized. Overall, the demonstrated nonvolatile memory devices and high-performance multi-level operations hold substantial potential for advancing logic-in-memory applications.

2 Results and discussion

Figures 1(a) and 1(b) present the structure and optical image of the

WSe_2 floating gate transistor. The fabrication process was as follows: A WSe_2 flake with a thickness of 3–5 layers was mechanically exfoliated using Scotch tape and transferred onto a p^+ Si substrate with a 300 nm SiO_2 layer. Cr/Au (10 nm/30 nm) contacts were patterned via electron-beam lithography, followed by metal deposition and lift-off to form source/drain electrodes. HfS_2 flakes (approximately 15 nm thick) were then transferred onto the device, overlapping the WSe_2 channel. Ozone treatment was performed: Supersaturated oxygen atoms accumulated at the $\text{HfS}_2/\text{WSe}_2$ interface, driving partial oxidation of HfS_2 flake from both surfaces. The evolution of the $\text{WSe}_2/\text{HfS}_2$ interface during oxidation is illustrated in Fig. S1 in the Electronic Supplementary Material (ESM). After 40 min, the HfS_2 flake converted into an $\text{HfO}_x/\text{HfS}_2/\text{HfO}_x$ floating gate stack. Supersaturated oxygen also widened the intrinsic van der Waals gap at the $\text{HfS}_2/\text{WSe}_2$ interface, forming a nano-confined elemental oxygen layer. Finally, the top-gate electrode was fabricated to complete the structure. Figure 1(c) displays Raman spectra of different regions in the $\text{HfO}_x/\text{HfS}_2/\text{HfO}_x/\text{WSe}_2$ stack. WSe_2 spectral profiles are consistent between the HfO_x -covered and exposed regions on the SiO_2/p^+ Si substrate, confirming negligible impact of ozone oxidation on WSe_2 channel properties. Figure 1(d) shows electron energy loss spectra line scans, visualizing oxygen distribution. The shaded region (O K-edge partial density of states) reveals elemental oxygen accumulation at the $\text{HfO}_x/\text{WSe}_2$ interface [26, 27]. To analyze the composition of the nano-confined elemental oxygen layer, depth-resolved XPS measurements were performed, revealing that the oxygen layer is predominantly composed of O–O-bonded species (Fig. S2 in the ESM). The corresponding cross-sectional scanning transmission electron microscopy image (Fig. 1(e)) clearly shows layered structure of WSe_2 channel, HfS_2 floating gate, and HfO_x layer with distinct boundaries. Furthermore, the XPS results in Fig. S3 in the ESM corroborate these findings, confirming the structural

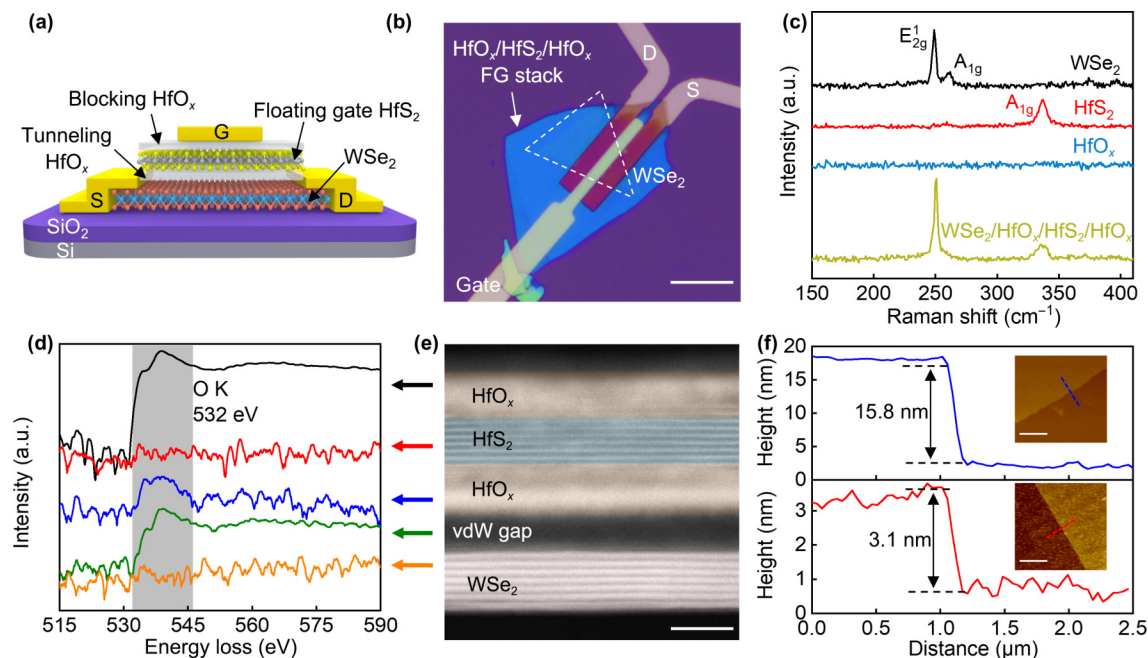


Figure 1 (a) 3D schematic of the device, including a WSe_2 channel, an HfS_2 floating gate, and bilateral HfO_x layers. These HfO_x layers serve as both the tunneling layer and control-gate oxide dielectric. (b) Optical image of the WSe_2 floating gate transistor. Scale bar: 10 μm . (c) Raman spectra collected from different regions in the device. (d) Electron energy loss spectra of O K-core level edges, summed from different layers of the device stack. (e) False-color scanning transmission electron microscopy image of the WSe_2 floating gate transistor. Scale bar: 5 nm. (f) Height profiles of the $\text{HfO}_x/\text{HfS}_2/\text{HfO}_x$ stack and WSe_2 , along the blue dashed line and red dashed line, respectively. The inset shows the topography image measured by AFM. Scale bar: 2 μm .

integrity of the WSe₂ layer. Figure S4 in the ESM compares the dielectric constants of HfO_x obtained by HfS₂ oxidation and HfO₂ grown by conventional ALD, which are 20.9 and 17.6, respectively. Using an atomic force microscope (AFM), as illustrated in Fig. 1(f), the thickness of each material was measured: The HfO_x/HfS₂/HfO_x stack was approximately 15.8 nm thick, while the WSe₂ layer measured around 3.1 nm.

Figures 2(a) and 2(b) present transfer curves of the device under varied sweeping ranges of back-gate voltage (V_{BG}) and top-gate voltage (V_{TG}), with a fixed drain-source bias (V_{DS}) of 1 V. The observed counterclockwise hysteresis stems from the charge trapping mechanism, which generates memory windows (ΔV) defined by threshold voltage shift between forward and reverse sweeps [28]. As illustrated in Fig. 2(c), ΔV gradually increases with larger $V_{G, MAX}$ values. This phenomenon arises from enhanced amounts of charge trapped in or detrapped from the HfS₂ floating gate, signifying excellent memory window tunability. Specifically, top-gate and back-gate devices can achieve maximum ΔV values of 2.6 and 51 V, respectively. The number of stored charges in the HfS₂ floating gate can be estimated using the formula $(\Delta V \times C_G)/e$ [29]. Here, e is the electron charge (1.6×10^{-19} C), and C_G is dielectric capacitance between the HfS₂ floating gate layer and control gate. The calculated stored electron density in the HfS₂ floating gate exceeds 3.7×10^{12} cm⁻², and this high charge density enables convenient detection in practical applications. Figures 2(d) and 2(e) illustrate energy band diagrams of the HfS₂/HfO_x/WSe₂ heterostructure under positive and negative gate voltages. When a positive gate voltage is applied, electrons tunnel through the HfO_x tunneling layer from the WSe₂ channel into the HfS₂ floating gate. After gate voltage removal, electrons remain trapped in the floating gate due to the high energy barrier of the tunneling dielectric. These trapped electrons then act as an effective negative local gate potential for the channel. Since WSe₂ exhibits hole-dominant

conductivity, the device switches to the on state. Conversely, a negative gate voltage induces electrons detrapping from the HfS₂ floating gate into the WSe₂ channel, leading the device to the off state under zero gate bias. Figure 2(f) illustrates retention capability of the WSe₂ floating gate transistors. After programming operations ($V_{BG} = 70$ V or $V_{TG} = 3$ V) and erasing operations ($V_{BG} = -70$ V or $V_{TG} = -3$ V), a drain-source bias of $V_{DS} = 1$ V was applied to monitor channel current, while the gate electrodes were kept in a floating state to evaluate the non-volatility of the stored charges. Over a 10⁵ s monitoring period, the current ratio between programmed and erased states remained stable at 10³, demonstrating excellent retention performance. This robust retention performance originates from the elemental oxygen layer in the floating gate structure. This layer effectively suppresses mutual coupling between gate-stored charges and carriers in the WSe₂ channel under both high and low resistance states. Furthermore, the elemental oxygen layer acts as a barrier to inhibit defect-assisted tunneling between channel electrons and gate-stored charges. Thus, it provides immunity against storage failures otherwise induced by an ultrathin tunneling layer in floating gate devices. We fabricated a control WSe₂ floating-gate transistor without an elemental oxygen layer, in which both the tunneling and blocking layers were composed of HfO₂ grown by ALD. Figure S5 in the ESM presents a direct performance comparison between the control device and our proposed device incorporating a nano-confined elemental oxygen layer. The results clearly demonstrate that the WSe₂ floating-gate transistor with the nano-confined elemental oxygen layer exhibits significant enhancements in storage capability and a reduction in leakage current.

Figures 3(a) and 3(b) illustrate resistance switching characteristics of a WSe₂ floating gate transistor under varied gate voltage pulse conditions. Before each programming operation, the device was reset to the erased state via a negative gate voltage. As

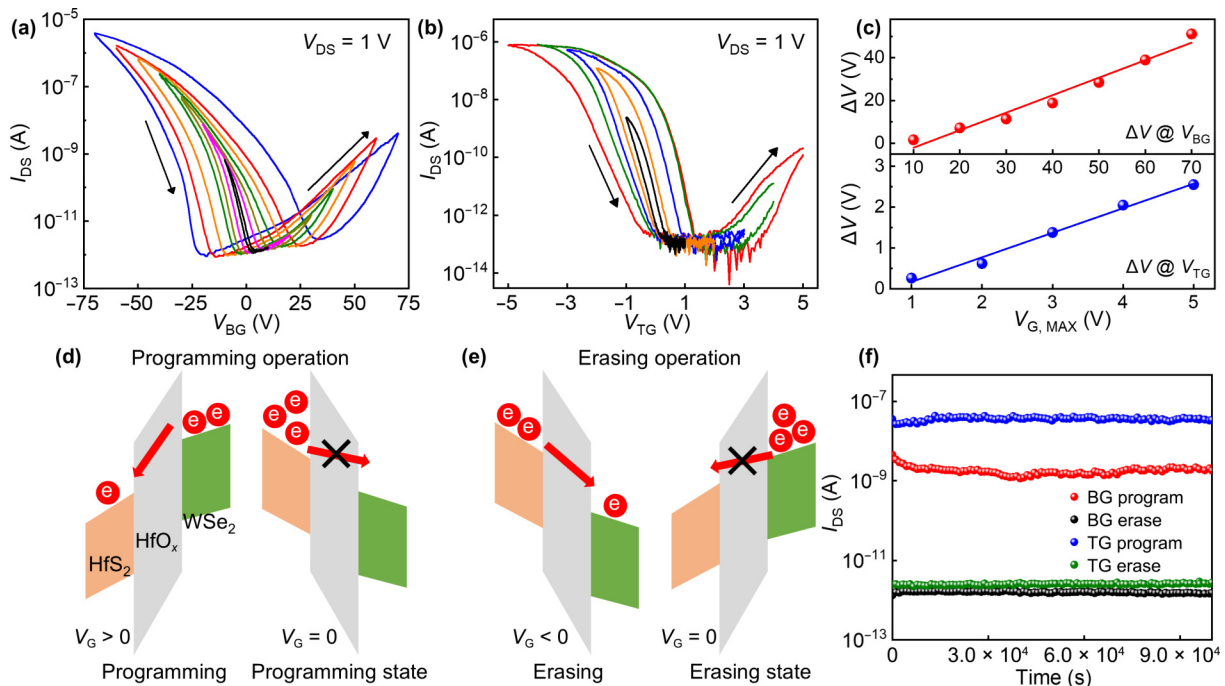


Figure 2 (a) Back-gate and (b) top-gate transfer characteristics of WSe₂ floating gate transistors. (c) Extracted memory window as a function of maximum applied voltage ($V_{G, MAX}$). Schematic energy-band diagrams of the WSe₂ floating gate transistor during (d) programming and (e) erasing operations. The specific energy band values were extracted from corresponding Refs. [30, 31]. (f) Retention characteristics of the WSe₂ floating gate transistor after applying back-gate pulses of ± 70 V and top-gate pulses of ± 3 V (pulse duration: 1 s). The gate was maintained in a floating state during the retention monitoring.

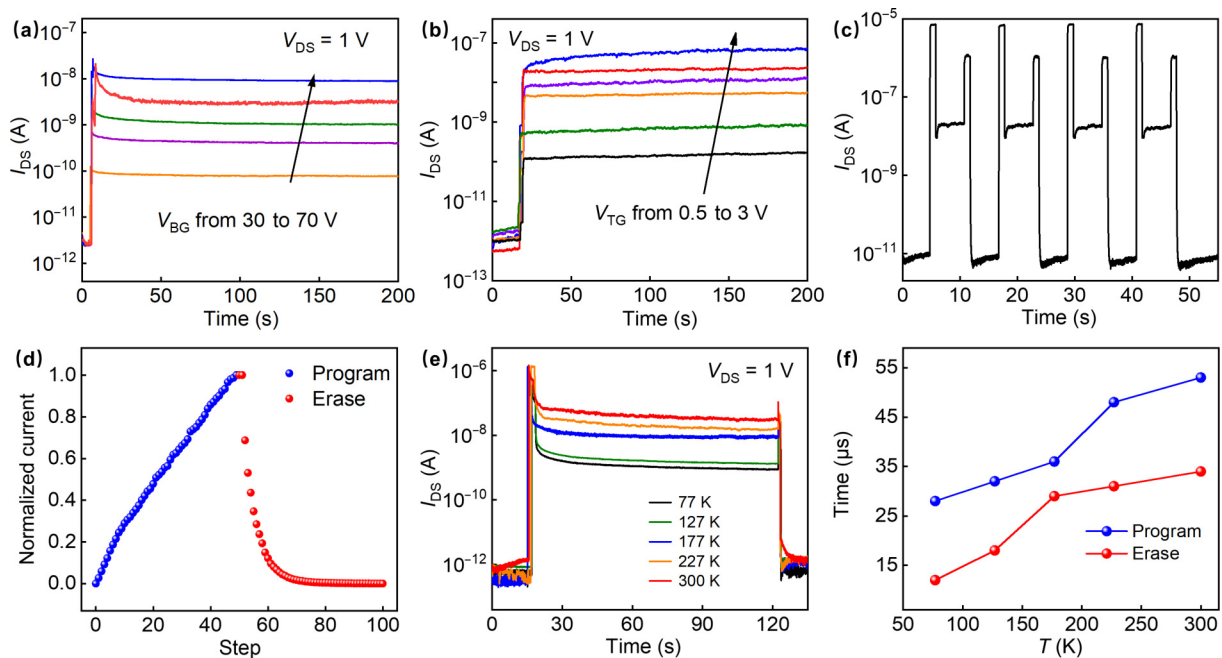


Figure 3 (a) and (b) Multilevel memory operation processes: (a) using back-gate pulses (pulse duration: 1 s) with voltages incrementally increased from 30 to 70 V. (b) Using top-gate pulses (pulse duration: 1 s) with voltages incrementally increased from 0.5 to 3 V. (c) Endurance characteristics of the WSe₂ floating gate transistor. Programming and erasing operations were performed under cyclic V_{TG} of ± 3 V (pulse duration: 1 s), while the reading current was measured at a V_{DS} of 1 V. (d) I_{DS} –time curve with pulses ($V_{TG} = \pm 0.5$ V, pulse duration: 0.01 s) applied at 5 s intervals, demonstrating multi-level memory capability. (e) Programming and erasing processes of WSe₂ floating gate transistors under different temperature conditions. (f) Temperature-dependent operation speed of the device.

gate voltage pulse amplitude increases, channel current rises gradually and programming/erasing ratio increases from 10^2 to 10^4 . The device exhibits stable, distinguishable states under different gate pulse conditions. To evaluate reliability for memory applications, the device underwent multiple resistance switching cycles induced by successive V_{TG} pulses. As illustrated in Fig. 3(c), the transistor demonstrates highly reproducible switching between the low-resistance (LRS) and high-resistance states (HRS). Throughout the extended endurance test of 2000 cycles, the memory window remained remarkably stable and clearly distinguishable, highlighting the robust performance and practical potential of this floating gate structure (Fig. S6 in the ESM). For multi-bit memory, Fig. 3(d) presents normalized current as a function of pulse number. The device was first erased to the lowest conductance state with a large negative top-gate voltage (-3 V). Programming and erasing voltages were set to a V_{TG} of 0.5 and -0.5 V to trap and release electrons in the floating gate, respectively. Electron injection into the floating gate shifts the threshold voltage toward a more positive value, resulting in a higher read current and confirming feasibility of multi-level storage. To identify dominant transport mechanism, transfer characteristics were measured across various temperatures. As presented in Fig. 3(e), low-resistance state current increases with temperature, which is attributed to temperature-dependent Fowler–Nordheim tunneling in the floating gate stack. The electron injected current follows the model described by the following equation [32]

$$I = WLA \left(\frac{V_G - V_{FG}}{t_{ox}} \right)^2 e^{-\frac{B_{fox}}{V_G - V_{FG}}} \quad (1)$$

Here, t_{ox} is tunneling oxide layer thickness, W and L are channel width and length, V_{FG} is voltage across the floating gate, A and B are temperature-dependent fitting parameters. At higher temperatures,

more carriers accumulate in the channel, which enhances tunneling probability and promotes electron injection into the floating gate, ultimately resulting in a higher low-resistance state current. Even at 77 K, the device maintains an on/off ratio exceeding 10^3 , confirming Fowler–Nordheim tunneling as the dominant mechanism. Programming/erasing speed was measured with an oscilloscope at different temperatures (Fig. 3(f)). At 77 K, the transistor achieves a 28 μ s programming speed and a 12 μ s erasing speed. A slight variation in speed with temperature corresponds to a weak thermionic emission process.

The top-gate and back-gate enable multi-gate operation, as illustrated in Fig. 4(a). Using this configuration, transistor-based logic gates, including NOT, XNOR, and XOR gates, were designed to verify functionality. In digital electronics, encoded information uses two distinct voltage ranges. With V_{IN1} as input, a PMOS inverter (NOT gate) was constructed: the WSe₂ floating gate transistor acts as switching transistor, while a second transistor operating in saturation mode serves as load. For this load transistor, HfO_x oxide from an ozone-treated HfS₂ flake was used as gate dielectric. Figure 4(b) exhibits voltage transfer characteristics of the inverter under different supply voltages (V_{DD}), with V_{OUT} and V_{IN1} as output and input voltages, respectively. The insets show the circuit diagram. Figure 4(c) presents a maximum voltage gain of 3.5, which is critical for effective signal regeneration in digital circuits. The static power consumption of the inverter is shown in Fig. S7 in the ESM. Specifically, the static power consumption remains below 4 nW at $V_{DD} = 2$ V, and further decreases to approximately 1 nW when $V_{DD} = 1$ V. Figure 4(d) presents the circuit diagram and corresponding truth table of the XNOR gate, with the top and back gates as two inputs and load transistor as a pull-down resistor. Figure 4(e) demonstrates the XNOR logic function: Upper panel shows input signals for V_{IN1} and V_{IN2} , with high and low input voltages representing logic “1” and logic “0”, respectively. When

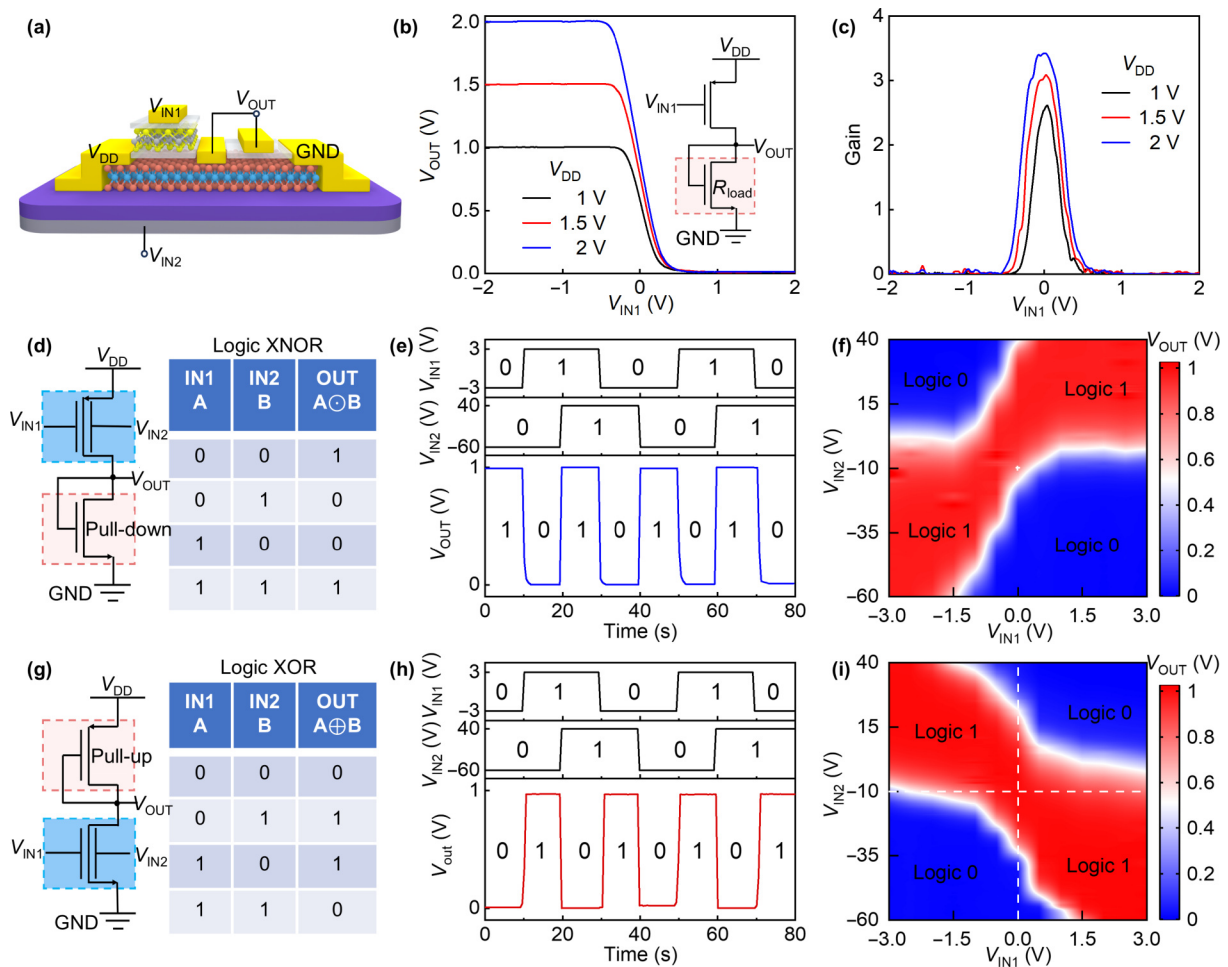


Figure 4 (a) Schematic of the fabricated logic device. (b) Output voltage as a function of input voltage. The inset shows the inverter circuit diagram. (c) Voltage gain of the inverter. (d) Circuit diagram and truth table of the XNOR logic gate. (e) Output voltage of the XNOR logic gate under four typical input states (power supply: $V_{DD} = 1$ V). (f) Operational performance of the XNOR logic gate with different V_{IN1} and V_{IN2} values. (g) Circuit diagram and truth table of the XOR logic gate. (h) Output voltage of the XOR logic gate under four typical input states (power supply: $V_{DD} = 1$ V). (i) Operational performance of the XOR logic gate with different V_{IN1} and V_{IN2} values.

both V_{IN1} and V_{IN2} are negative (or both positive), the input signals correspond to logic low level “0” (or logic high level “1”). In this case, the WSe_2 floating gate transistor operates in p-type (or n-type) conduction with a resistance much lower than that of the pull-down resistor, making V_{OUT} close to 1. When V_{IN1} is negative (or positive) and V_{IN2} is positive (or negative), top and back gate electric fields cancel, preventing majority carrier accumulation. The transistor turns off with a resistance far higher than that of pull-down resistor, resulting in a low V_{OUT} of “0”. Figure 4(f) illustrates XNOR logic operation, where red and blue represent the on and off states of the transistor, respectively. Similarly, XOR logic was verified using load transistor as a pull-up resistor. Figure 4(h) demonstrates the XOR logic function, and Fig. 4(i) presents the operating characteristics of the XOR logic circuit.

3 Conclusions

In summary, we developed a floating gate transistor fabrication process via HfS_2 flake oxidation. This process removes the need for invasive sputtering or atomic layer deposition during dielectric deposition. We demonstrated that the $\text{HfS}_2/\text{WSe}_2$ structure enables simultaneous oxidation of HfS_2 into $\text{HfO}_x/\text{HfS}_2/\text{HfO}_x$ from both upper and lower surfaces. This forms a composite structure

comprising a tunneling layer, a floating gate, and a top-gate dielectric layer. This design simplifies the floating gate transistor fabrication workflow and forms a nano-confined elemental oxygen layer. This layer effectively suppresses defect-assist leakage current. The fabricated WSe_2 floating gate transistor exhibits a programmable memory function and excellent low-temperature memory characteristics. We also constructed NOT, XNOR, and XOR logic gates and realized computing-in-memory functionality. Our floating gate transistor fabrication strategy can integrate 2D materials with amorphous oxide dielectrics, providing a promising approach for the development of high-performance electronic devices.

4 Experimental acknowledgements

4.1 Device fabrication and electrical characterization

Initially, WSe_2 flakes were positioned onto a highly doped Si wafer coated with a 300-nm-thick SiO_2 layer by mechanical exfoliation. A bilayer consisting of methyl methacrylate and poly (methyl methacrylate) served as the photoresist, and the pattern for the source/drain contact electrodes was established using electron beam lithography (EBL). Following development, thermal evaporation

was employed to deposit Cr/Au electrodes (10/30 nm), which were subsequently subjected to a lift-off process. Subsequently, an HfS_2 flake was positioned above the WSe_2 channel using a physical transfer technique. Ozone treatment was then applied to oxidize the HfS_2 , converting it to HfO_x . This process occurred within a chamber pre-filled with oxygen gas under atmospheric conditions, where ultraviolet light from a UV lamp was used to generate ozone. A 300 W ultraviolet lamp was used as the UV source, and the UV light intensity was 50 mW/cm^2 . The thermal irradiation led to a mild temperature of 40°C on the substrate. Lastly, the top-gate electrode area was defined by EBL, and the Cr/Au electrode (10/30 nm) was deposited using thermal evaporation, followed by a lift-off procedure. The electrical performance was evaluated using a Lake Shore TTPX probe station operating in a vacuum environment. The temperature conditions for these measurements ranged from 77 to 377 K. The gathered data were then recorded by an Agilent B1500A semiconductor parameter analyzer. Additionally, the response times were specifically captured using a KEYSIGHT CX3324A device current waveform analyzer. Raman spectra were determined using a WiTec Alpha300R system. A continuous-wave laser with a wavelength of 532 nm was employed as the excitation source. The thicknesses of WSe_2 and HfS_2 layers were determined by a Bruker Dimension Icon atomic force microscope.

4.2 Cross-sectional transmission electron microscopy (TEM) sample preparation and characterization

For the preparation of cross-sectional TEM samples, a multibeam scanning electron microscopy-focused-ion-beam system (model JIB 4501 by JEOL) was used. This system operated with Ga ions at an acceleration voltage of 30 kV. To further characterize the samples, TEM was conducted using a JEOL JEM-2100F TEM/scanning TEM instrument, which was operated at 200 kV. This TEM setup incorporated an Oxford INCA energy-dispersive spectroscopy (EDS) detector for elemental analysis and an electron energy loss spectroscopy (EELS) spectrometer for elemental mapping. To minimize potential electron-beam-induced artifacts, data were collected using a low-dose acquisition mode with optimized dwell times, ensuring the structural integrity of the oxide layers.

Electronic Supplementary Material: Supplementary material (TEM images, XPS spectra, dielectric properties, electrical performance comparison, endurance performance and static power consumption) is available in the online version of this article at <https://doi.org/10.26599/NR.2026.94908578>.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

W. C. N.: Data curation, writing – original draft. P. C. Z.: Formal analysis, validation. Z. D. X.: Simulation, validation. T. B.: Investigation. L. T.: Data curation. S. Z.: Investigation. B. J.: Conceptualization, validation. X. Z.: Resources. X. T. H.: Methodology. X. M. Z.: Supervision. X. P. D.: Funding acquisition, project administration. L. L.: Funding acquisition, conceptualization. X. Q. L.: Funding acquisition, methodology, experimental design. All the authors have approved the final manuscript.

Use of AI statement

None.

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