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Orientation-engineered halide perovskite single-crystal cathodes for efficient field emission in nano vacuum channel transistors

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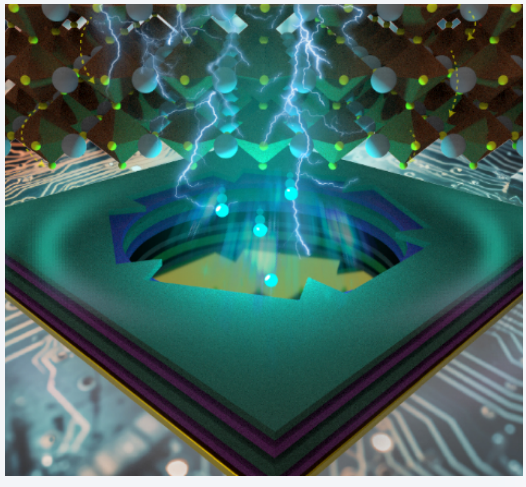
ABSTRACT: Nano vacuum channel transistors (NVCTs) are increasingly recognized as a promising class of devices for high-frequency, radiation-hardened, and beyond-complementary metal-oxide-semiconductor (CMOS) electronics, yet their progress has been constrained by the low emission current, high turn-on voltage, and limited manufacturability. Here, we reported the first integration of halide perovskite single crystals ($MAPbBr_3$, MA stands for methylammonium) as the electron emitter in NVCTs, achieving performance levels incomparable to those using other cathode materials. Remarkably, even with a large vacuum channel length of ~ 230 nm, the devices delivered drain currents up to 1.26 mA and operated at a remarkably low turn-on voltage of 8 V in air, highlighting their exceptional emission capability. The perovskite-assisted NVCTs exhibited a robust gate modulation with negligible leakage and pronounced photo-responsivity, enabling potential electrical–optical joint control. Importantly, the devices were fabricated on display glass substrates using thin-film transistor-liquid crystal display (TFT-LCD) manufacturing processes, offering a pathway toward low-cost, scalable, and integrable nano-vacuum electronics. This work established perovskite single crystals as a new material platform for manufacturable, multifunctional vacuum electronics with relevance to the next-generation information and communication technologies.



KEYWORDS: perovskite, nano vacuum channel transistor (NVCT), electron emission, ion migration, vacuum electronics

1 Introduction

The relentless demand for higher information throughput and device operating frequencies, driven by big data, artificial intelligence (AI), and ubiquitous Internet of Things (IoT) connectivity, has exposed intrinsic limits in conventional solid-state electronics [1–5]. As device dimensions approach the nanoscale, further scaling incurs escalating fabrication costs and heat dissipation issues; meanwhile, short-channel effects and carrier-velocity saturation fundamentally cap the speed and power performance of semiconductor transistors (e.g., the electron saturation velocity of Si is ~ 10^7 cm/s) [6, 7]. These constraints motivate alternative device concepts for high-frequency, high-power, and harsh-environment operation.

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Nano vacuum channel transistors (NVCTs) have emerged as a promising class of devices that integrate the scattering-free transport properties of vacuum with the precision of semiconductor processes [8–11]. In the vacuum, electrons propagate free of lattice scattering, phonon interactions, and defect trapping, enabling quasi-ballistic transport with minimal signal distortion and ultrafast switching. These intrinsic features endow NVCTs with high-frequency capability, radiation immunity, and thermal stability, making them promising candidates for high-power radio frequency (RF) power amplifiers, millimeter-/terahertz-wave transmit front-ends, and other extreme-environment electronics [12–14].

Nevertheless, despite significant advances in device physics and fabrication methods, practical NVCTs remain constrained by three major bottlenecks: insufficient emission current, high turn-on voltages, and limited manufacturability/scalability [15, 16]. Reported devices typically delivered only nA–μA level on-currents in air, required sub-mean-free-path channel lengths (< 100 nm) for stable operation [17–19], and relied on fabrication flows that were difficult to scale to large-area manufacturing. These limitations have

been hindering the transition of NVCTs from laboratory demonstrations to deployable systems.

These challenges ultimately stem from the emitter, which governs the supply of electrons into the vacuum channel. The turn-on voltage, on-state current, and gate controllability of NVCTs are all dictated by emitting efficiency, making their design critical to the ultimate device performance. To address this, researchers have explored three major types of emitters. Jones et al. [20] designed Spindt-type metallic tip arrays that achieved high current densities via strong field enhancement, though fabrication required complex vacuum deposition and was highly sensitive to tip uniformity. Xu et al. [21] demonstrated a graphene-based NVCT with a ~ 90 nm vacuum channel fabricated by standard electron-beam lithography (EBL). The device achieved an on/off current ratio of ~ 10^2 with working voltages below 20 V and leakage currents under 0.5 nA, highlighting graphene as a viable emitter in NVCTs. But these devices suffered from poor long-term stability and large-area reproducibility. Han et al. [22] advanced this field by proposing a surround-gate architecture combined with sacrificial layer defined vacuum channels, showing that the gate not only switched the device but also significantly improved emission control and array current. However, their devices relied on vacuum encapsulation, exhibited limited current levels at relatively high voltages, and involved costly, complex processing, leaving critical bottlenecks unsolved.

Taken together, these studies revealed a persistent trade-off: While metallic emitters can provide strong currents, carbon nanostructures lower operating voltages, and wide-bandgap semiconductors improve stability, none of them could simultaneously achieve high performance and scalable, low-cost fabrication. Halide perovskites have recently emerged as a versatile class of semiconductors that combine high carrier mobility, low exciton binding energies, and intrinsically defect-tolerant lattices [23–25]. Their low formation energy enables facile solution processing, while their tunable band structures and abundant surface states make them excellent candidates for optoelectronic applications, including solar cells [26–29], light-emitting devices (LEDs) [30, 31], and photoelectric sensing devices [32–34]. These attributes suggest that halide perovskites may also serve as efficient electron emitters: Their high carrier densities and adjustable surface electronic structures could facilitate electron injection into vacuum under relatively low electric fields [35, 36]. Yet, despite extensive exploration in photovoltaics and light emission, their potential as cathode materials in vacuum electronics has remained largely unexplored.

In this work, we leveraged these unique advantages by integrating $MAPbBr_3$ (MA stands for methylammonium) perovskite single-crystal (SC) into a hollow-edge NVCT architecture. Fabricated entirely on glass substrates using scalable fabrication processes in semiconductor display industry, our devices demonstrated milliampere emission currents at a low turn-on voltage of ~ 8 V in air, even with a relatively wide ~ 230 nm vacuum channel. Compared with conventional NVCTs, the perovskite-assisted devices exhibited enhanced gate modulation without noticeable gate leakage, as emission predominantly arose from the perovskite surface rather than parasitic edge tips. Moreover, they showed pronounced photo-responsivity, indicating the feasibility of electronic–optoelectronic joint control. By transforming the emitter role from a purely geometric field enhancement element to a materials-driven electron source, this study provided a low-cost and scalable pathway toward multifunctional nano vacuum electronics.

2 Experimental

2.1 Fabrication of nano vacuum channel transistors

As shown in Fig. S1 in the Electronic Supplementary Material (ESM), 4-inch glass substrates were sequentially cleaned in acetone, ethanol, and deionized water by ultrasonic agitation for 15 min each, followed by nitrogen blow-drying. A 40 nm Au film was then deposited on the cleaned substrates by magnetron sputtering and patterned into bottom electrodes using photolithography and wet etching. Subsequently, a 40 nm Si_3N_4 insulating layer was deposited on the bottom electrodes by plasma-enhanced chemical vapor deposition (PECVD). On top of this layer, a 100 nm Ag film was sputtered and patterned by photolithography and wet etching to form the gate electrodes. Another 40 nm Si_3N_4 dielectric layer was deposited by PECVD to isolate the gate. 40 nm Al layer was then sputtered on the top surface and patterned through photolithography and wet etching to form the top electrodes. Finally, reactive ion etching (RIE) was employed to remove the excess Si_3N_4, completing the fabrication of the NVCTs.

2.2 Synthesis of $MAPbBr_3$ single crystals

For the precursor solution, $PbBr_2$ (Aladdin, 99%) and MABr (Aladdin, 99.9%) were dissolved in N,N-dimethylformamide (DMF) at a concentration of 1.2 M, with a molar ratio of 1:1.5. After complete dissolution of the solids, the solution was filtered through a polytetrafluoroethylene (PTFE) syringe filter with a pore size of 25 μm. For the growth of (100)-oriented single crystals, 5 mL of the filtered solution was transferred into a glass vial, and a seed crystal was introduced. The vial was kept at 50 °C for 2 days, yielding single crystals with an average size of ~ 3 mm. For the growth of (110)-oriented single crystals, $PbBr_2$ and MABr were dissolved in DMF at a total concentration of 1.2 M, with an adjusted molar ratio of 1.2:1. Approximately 2 mL of the precursor solution was dropped onto the surface of a polydimethylsiloxane (PDMS) film and placed in a nitrogen-filled glovebox. The sample was maintained at 30 °C for about 7 days, resulting in the formation of hexagonal single crystals with (110) orientation.

2.3 Integration of perovskite SCs with NVCT devices

For device assembly, $MAPbBr_3$ single crystals were mounted onto the emitter region of the NVCTs. In all cases, a smooth and flat facet (either an as-grown facet or a freshly cleaved facet) was oriented downward to fully cover the pore-array emitter region, ensuring that the apertures were covered by a planar crystal surface. For (100)-oriented crystals, the as-grown surfaces typically exhibited a higher density of surface defects; therefore, the crystals were cleaved along their natural cleavage planes to expose flatter, defect-minimized facets prior to placement.

To fix the SC on the emitter region, a thermo-compression procedure was employed (Fig. S3 in the ESM). A thin PDMS layer was placed on top of the perovskite crystal only as a compliant buffer during pressing, while thicker PDMS spacers were arranged around the periphery to keep the pressing load level and prevent tilting. A glass slide was then placed on top, followed by a ~ 2 kg weight to provide a gentle and constant load. The assembly was heated at 60 °C for 60 min under this load and then cooled to room

temperature. After the thermo-compression step, the weight, glass slide, and PDMS pieces were carefully removed while still warm, and the device was subsequently cooled to room temperature, with the perovskite crystal remaining on the emitter region. Notably, PDMS was used only on the top side during pressing and was not present at the perovskite/electrode interface. For (110)-oriented crystals grown directly on PDMS films, the bottom facets were relatively flat; thus, a smooth facet could be directly oriented toward the pore-array emitter region and fixed using the same thermo-compression procedure.

3 Results and discussion

Figure 1(a) presents an optical image of the perovskite-integrated NVCT array, where individual $MAPbBr_3$ SCs can be clearly observed on top of the NVCT emitters. Through a hot-pressing process, the perovskite single crystal is tightly bonded to the underlying device. Figure 1(b) illustrates the device architecture, consisting of a vertically stacked structure of perovskite SC/Al/Si_3N_4/Al/Si_3N_4/Au/Ti (from top to bottom). When a large bias (source–drain voltage (V_{sd})) is applied between the top source electrode and the bottom drain electrode, electrons are emitted from the cathode region (perovskite and Al) by overcoming the surface potential barrier. These electrons travel along the electric field lines through the vacuum channel and are collected by the bottom drain, forming the drain current (I_d). The magnitude of I_d directly reflects the emission capability of the device.

Figure 1(c) shows a microscopic image of the NVCT arrays, which are composed of multiple single-pore NVCT units. Even after multiple rounds of photolithography and pattern transfer, the arrays maintain excellent uniformity and reproducibility, underscoring the compatibility of the fabrication process with large-area integration. Figure 1(d) depicts a single NVCT unit, where the emission aperture has a diameter of ~ 15 μm. Such relatively large apertures are deliberately adopted to relax lithographic resolution requirements, thereby enabling fabrication using cost-effective, large-area processes commonly employed in the display industry.

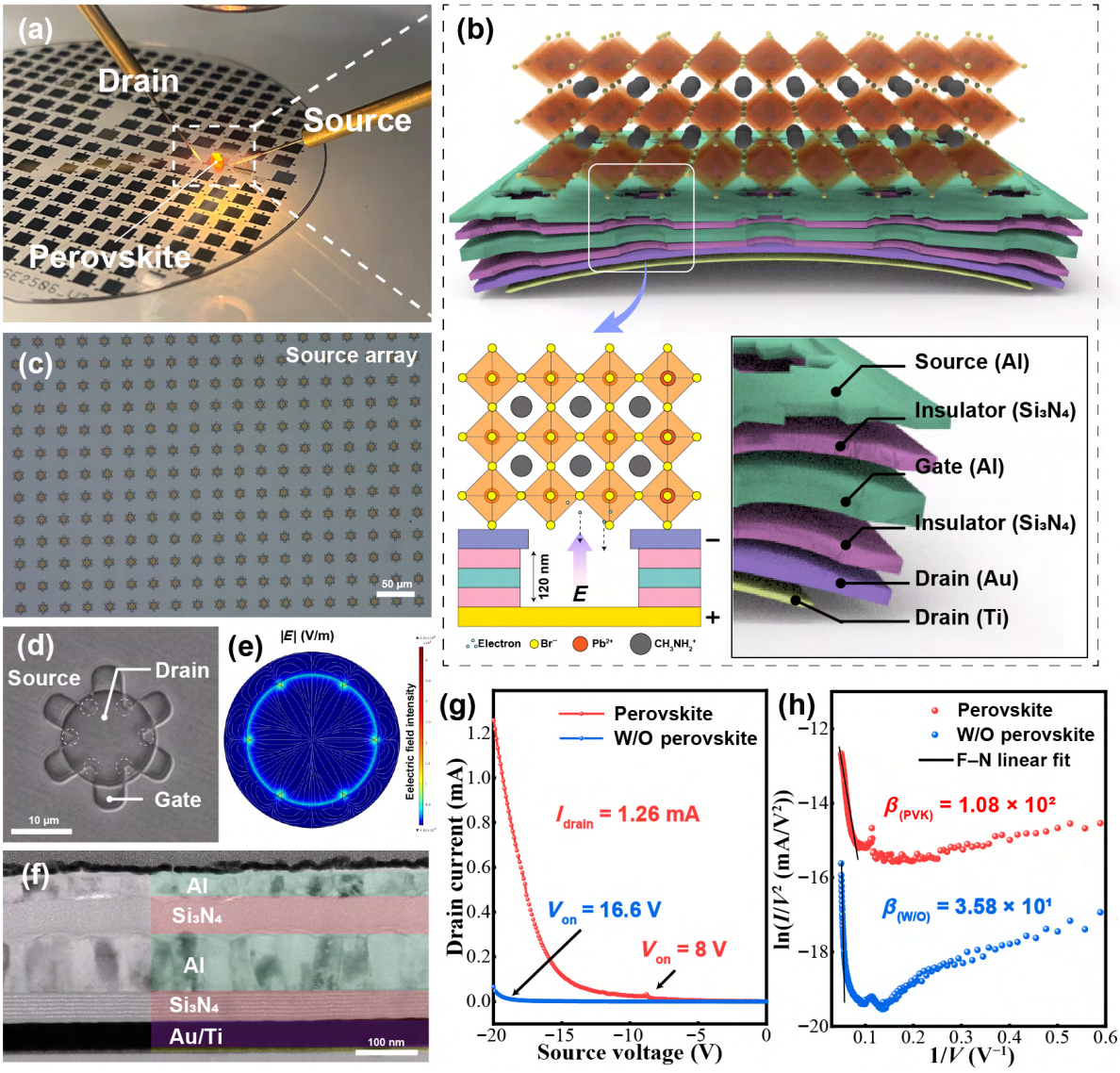

Figure 1 Device structure and electrical performance of NVCTs. (a) Photograph of the NVCT array. (b) Schematic illustration of the device architecture. (c) Optical micrograph of the NVCT array. (d) Micrograph of a single NVCT unit. (e) Simulated electric-field distribution. (f) Cross-sectional image of the device. (g) I_d–V_{sd} characteristics comparing bare and perovskite-integrated devices. (h) Corresponding Fowler–Nordheim plots.

This approach stands in contrast to many previously reported NVCTs that require high-cost, low-throughput techniques, such as focused ion beam (FIB) or EBL. By designing a mask with three rectangular features arranged at 60 °C relative to one another, subsequent photolithography and wet etching produce a hexapod-like emitter with six sharp tips. This geometry concentrates the local electric field at the tips, significantly enhancing electron emission. The simulated electric field distribution (shown in Fig. 1(e), the simulations were performed using COMSOL Multiphysics 6.3), confirms strong field localization around the tips, verifying the efficacy of this low-cost, uniform emitter design compared to conventional Spindt-type tip arrays. Figure 1(f) shows the cross-sectional transmission electron microscope (TEM) image of the device, where each functional layer can be clearly distinguished. Elemental mapping by energy dispersive spectroscopy (EDS) further confirms the material composition of each layer (shown in Fig. S4 in the ESM). The vacuum channel length, measured from the bottom to the top electrode, exceeds 230 nm (shown in Fig. S5 in the ESM).

To avoid the influence of other factors, all device measurements were carried out under dark conditions. Figure 1(g) presents the I_d–V_{sd} characteristics of the array devices. With increasing source voltage, the drain current rises correspondingly. Compared to the control devices without perovskite, the perovskite assisted NVCTs exhibit a markedly reduced turn-on voltage (V_{on} = 8 V) and significantly higher emission current, reaching 1.26 mA at V_{sd} = −20 V. At relatively weak external fields, conduction electrons near the material surface are confined by the potential barrier defined by the work function, which prevents them from escaping into vacuum. As the applied electric field increases, the surface potential barrier becomes progressively thinner and lower, thereby enhancing the tunneling probability of electrons from the conduction band into vacuum states and giving rise to a measurable field-emission current, in accordance with the Fowler–Nordheim (F–N) tunneling model [37]. Derived from the F–N equation (the full derivation can refer to F–N equation derivation section in the ESM), the field-emission characteristics can be expressed in the linearized form

$$\ln\frac{I}{V^2} = \ln A - \frac{B}{V} \tag{1}$$

where A and B are fitting parameters derived from the linearized F–N equation

$$A = \frac{A_F a \beta^2}{\phi d^2} \tag{2}$$

$$B = \frac{B_F \phi^{\frac{3}{2}} d}{\beta} \tag{3}$$

where A_F = 1.54 × 10^{-6} A·eV/V^2 and B_F = 6.83 × 10^9 V/(eV^2·m) are constants, α is the effective emission area, β is the field enhancement factor, Φ is the work function, and d is the anode–cathode spacing [37]. The work function of Al is typically 4.1 eV [9], while the effective electron affinity of $MAPbBr_3$ SCs is 3.3 eV as reported in previous studies [38]. From the F–N fitting of the array devices, as shown in Fig. 1(h), the extracted field enhancement factor of the perovskite-assisted NVCT reaches 1.08 × 10^2, in contrast to only 35.8 for the metal-only device. This more than two-fold increase in β directly reflects the ability of the $MAPbBr_3$ single crystals to concentrate the local electric field at the emitter surface. As a consequence, even with comparable device geometries, the perovskite-modified cathodes exhibit a much lower apparent turn-on electric field and deliver substantially higher emission currents. In addition, the device exhibits an on/off ratio of 1.93 × 10^3, substantially exceeding that of the control device (2.73 × 10^2). These results provide quantitative evidence that the incorporation of halide perovskites can effectively boost electron emission efficiency in NVCT architectures.

Figure S6 in the ESM compares the core-level X-ray photoelectron spectroscopy (XPS) depth-profile of $MAPbBr_3$ SCs, showing a clear shift of all peaks toward higher binding energies from the surface to the bulk, indicating a difference in band structure between the surface and interior states. The Pb 4f peaks remain overall stable in position, but evolve from only two Pb^{2+} components at the surface to four distinct peaks in the bulk, reflecting the more diverse coordination environment of Pb inside the crystal. A more detailed comparison is given in Fig. 2(a), where the spectra after 30 and 60 s of etching are plotted. The N 1s peak becomes markedly stronger after 60 s, demonstrating that the surface contains fewer methylammonium cations while the bulk is relatively richer. In contrast, the Br 3d peak intensity decreases at 60 s, indicating that Br^- anions are enriched at the surface but depleted in the bulk. Taken together, these results provide direct evidence that the surface of $MAPbBr_3$ differs significantly from the bulk in both ionic composition and chemical states, with MA^+ deficiency and Br^- enrichment driving surface-state modifications, which are highly relevant to ion migration and its impact on band structure modulation.

In addition, the survey spectra show that the C 1s signal decreases markedly after sputtering, indicating effective removal of adventitious surface contamination and supporting that the subsequent core-level evolution reflects intrinsic near-surface versus bulk differences. The Pb 4f spectra remain dominated by Pb^{2+} related features across different depths, and no dominant anomalous new peaks are observed, suggesting that the perovskite framework is largely preserved within the probed depth range and reducing ambiguity associated with severe decomposition or parasitic products. Meanwhile, the Br 3d doublet retains an overall similar line shape and binding-energy position, implying no pronounced change in the Br chemical state; upon magnified comparison, a discernible depth-dependent intensity evolution is observed, further supporting a non-uniform Br distribution between the surface and the interior. Figure 2(a) is an enlarged view extracted from Fig. S6 in the ESM to more clearly illustrate the difference between 30 and 60 s etching conditions.

Figure 2(b) compares cross-sectional Kelvin probe force microscopy (KPFM) mappings of $MAPbBr_3$ single crystals before and after electrical poling under −40 V for 30 min. After poling, the regions close to the cathode exhibit significantly lower surface potential, as indicated by the darker contrast, consistent with the migration of Br^- anions toward the positively biased electrode. Figure 2(c) schematically illustrates the corresponding band alignment changes: The redistribution of ionic species generates localized surface charges, leading to downward band bending near the cathode and reducing the effective barrier height for electron emission [39]. Figure 2(d) further depicts the microscopic mechanism, where Br^- ions migrate preferentially along the octahedral edges within the perovskite lattice, producing dipolar fields that modulate the vacuum barrier. As summarized in

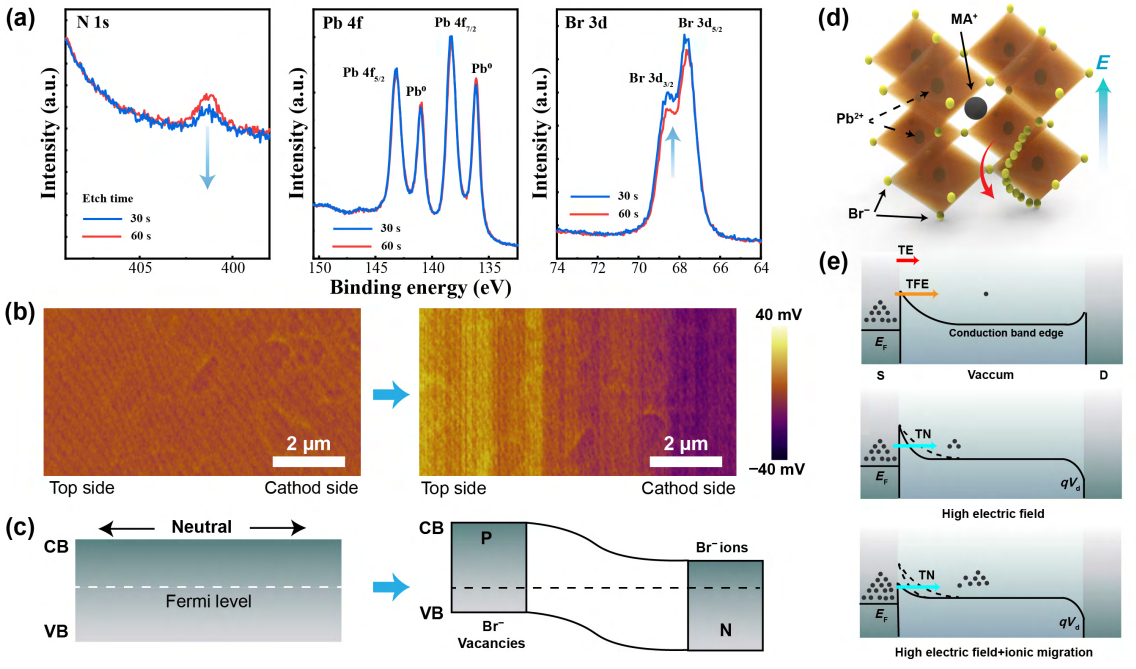

Figure 2 (a) XPS spectra, (b) cross-sectional KPFM of the single crystal before and after biasing, (c) schematic illustration of band bending, (d) schematic of ion migration in perovskite, and (e) the mechanism of enhanced electron emission.

Fig. 2(e), this ion-driven surface reconstruction narrows and lowers the tunneling barrier, thereby transforming the carrier injection mechanism from negligible thermionic/thermionic-field emission (TE/TFE) to efficient F–N tunneling, ultimately facilitating strong vacuum emission.

To further establish the correlation between perovskite-assisted emission and surface states, single-pore NVCTs were employed as substrates to ensure that the $MAPbBr_3$ crystals fully covered the emission aperture (Fig. 3(a)). The measurement wiring is illustrated in Fig. S3(b) in the ESM. The source-measure unit was connected to the patterned metal electrodes/pads to apply bias and establish the electric field. For clarity, the vacuum channel corresponds to the circular apertures located underneath the perovskite crystal. $MAPbBr_3$ served as the electron-emitting material, electrons were extracted from the emitter region under the applied field, emitted into vacuum, and finally collected by the bottom electrode. In addition, Fig. S3(c) in the ESM provides an optical image of the fabricated device (left) and a scanning electron microscope (SEM) image of the device edge region, with an inset schematic for clarity. As shown, the cathode region is not suspended; instead, an approximately 50 nm thick Si layer remains underneath as a supporting and insulating layer. Owing to the layer-by-layer fabrication process, a distinct topographical step is visible at the gate edge. This step is uniformly covered by Si, ensuring continuous insulation and preventing electrical leakage. SCs with (110) and (100) orientations were integrated, and their X-ray diffraction (XRD) patterns (Figs. 3(b) and 3(c)) show sharp reflections without secondary peaks, confirming high crystalline quality.

The I_d–V_{sd} characteristics of bare NVCTs, (110)-oriented and (100)-oriented devices are compared in Figs. 3(d)–3(f). Relative to the bare device, the turn-on voltage is reduced from 13.3 to 8.2 V (110) and 8.1 V (100), while the emission current (I_d) is enhanced from 0.27 to 2.18 and 2.66 μA, respectively. The corresponding F–N fits (Figs. 3(g)–3(i)) yield field enhancement factors of 2.79 × 10^2, 3.04 × 10^2, and 3.87 × 10^2, with the (100) devices exhibiting the largest β. This indicates that the (100) surface is more susceptible to forming favorable surface dipoles and band bending under bias, thereby lowering the effective emission barrier; in addition, its edge morphology facilitates stronger geometric field concentration. Together, these factors account for the substantially higher tunneling emission current observed in the (100) devices.

Figures 4(a) and 4(b) present simulated cross-sectional electric-field distributions and field-line orientations for NVCTs without and with perovskite, respectively (the simulations were performed using COMSOL Multiphysics 6.3). The three-dimensional geometries used in the simulations are shown in Fig. S9 in the ESM. For the perovskite-free configuration, the top cavity above the cathode is defined as vacuum, whereas in the perovskite-integrated configuration it is filled with $MAPbBr_3$. The electrostatic field distribution is obtained using the electrostatics interface, where the cathode, gate, and anode electrodes are assigned fixed potentials corresponding to the experimental biasing conditions. Based on the calculated field, electron trajectories are computed via the charged particle tracing interface. The electron emission from the cathode surface is modeled using the F–N formulation implemented through a field-dependent release feature. The walls at the designated collection surfaces (e.g., the anode and side boundaries) are defined with the freeze wall condition, meaning that electrons are absorbed upon impact without reflection or secondary emission. This treatment avoids artificial back-scattering and ensures that the simulated current only originates from the emission process. Material permittivity, geometric dimensions, and bias conditions follow the experimentally fabricated NVCT structure to enable direct comparison between simulation and measurement.

Under a gate bias, the field lines in the bare device exhibit pronounced bending near the gate, indicating a higher probability of electron interception by the gate electrode. In contrast, the perovskite-assisted device shows a broader and more uniform field distribution, with field lines in the central channel region oriented nearly vertically downward, suggesting that electron emission is less

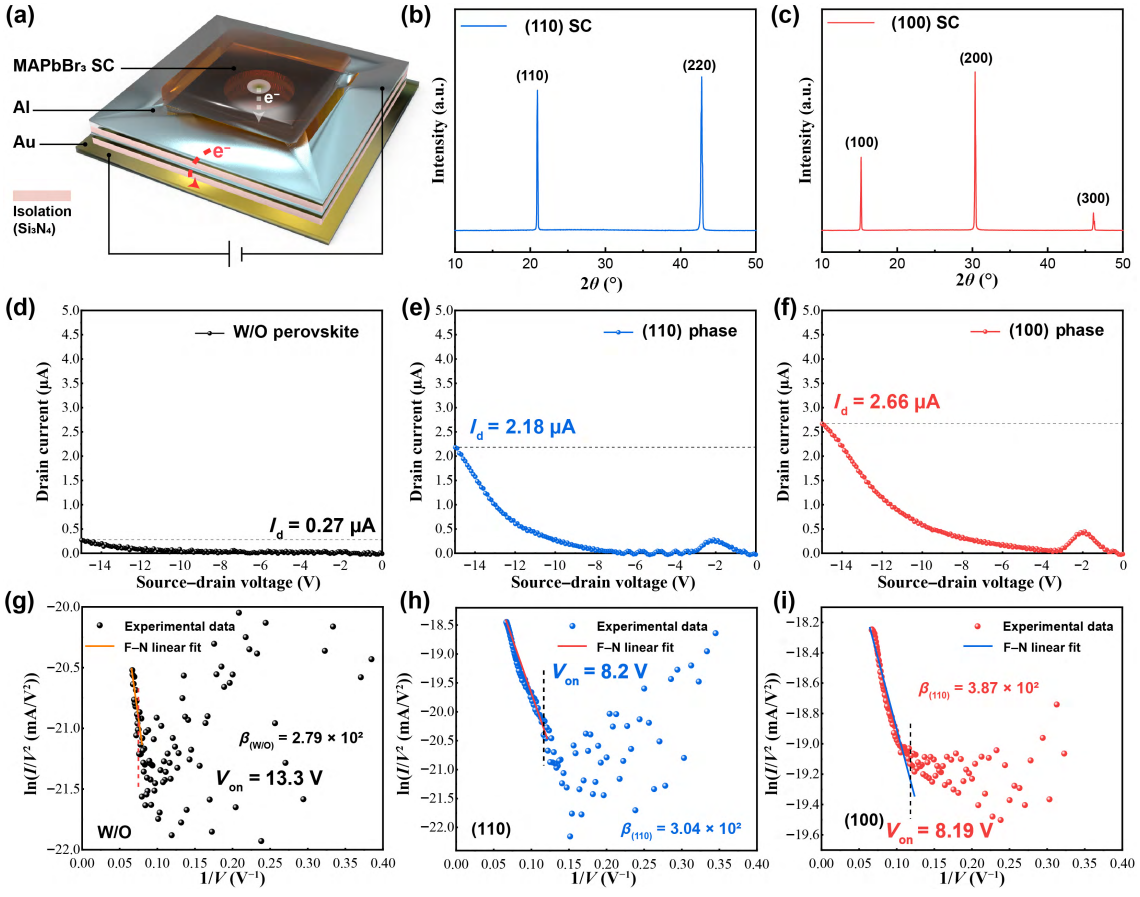

Figure 3 Comparison of single-pore NVCTs with $MAPbBr_3$ single crystals of different orientations. (a) Structure diagram of single-pore device; ((b) and (c)) XRD patterns; ((d)–(f)) curves of bare, (110), and (100) devices; and ((g)–(i)) F–N fitting curves.

influenced by the gate. Figures 4(c) and 4(d) show the transfer characteristics (I_d–V_g, V_g refers to the gate voltage) of the two devices. The gate modulation ratio of the bare NVCT is only ~ 52, whereas the perovskite-based device reaches 1.68×10^3. Moreover, the gate current of the bare NVCT rises rapidly with increasing gate bias, while that of the perovskite device remains relatively small (Figs. 4(e) and 4(f)). This difference arises because in perovskite-assisted devices, emission primarily originates from the perovskite surface at the aperture center, where the electron trajectories are directed more vertically toward the drain, reducing the likelihood of gate interception. The underlying mechanism is schematically illustrated in Fig. 4(g). In perovskite-based devices, electrons are predominantly emitted vertically from the aperture center. Owing to the intrinsically large emission current and abundant electron supply, the gate field exerts a pronounced influence on the beam trajectory. Under positive gate bias, the field induces beam divergence, reducing the number of electrons reaching the anode. In contrast, negative gate bias plays the role of focusing the electron beam and enhancing anode collection. As a result, the device delivers large drain currents while exhibiting strong gate controllability and maintaining negligible gate leakage.

We further assessed the operational stability of the perovskite-based devices. As shown in Fig. 5(a), after eight repeated test cycles under identical conditions, the emission current and corresponding I_d–V_{sd} characteristics remained essentially unchanged, indicating excellent cycling stability. Figure 5(b) presents the I_d–time (T) response under different gate biases at V_{sd} = 15 V. Over a continuous 60 s test, the drain current exhibited negligible decay across all gate voltages, confirming robust temporal stability. Considering halide perovskites as efficient optoelectronic semiconductors, we investigated their photo response.

As shown in Fig. 5(c), the device current increased markedly under illumination with an optical power density of 100 mW/cm² compared with the dark state. Moreover, during I_d–t measurements with different illumination intensities, the device current was clearly modulated by the incident light power (Fig. 5(d)). These results demonstrate that the device current can be regulated not only electrically through the gate voltage but also optically through illumination, pointing to the potential of perovskite-assisted NVCTs for multifunctional and logic-reconfigurable vacuum electronics.

We further evaluated the reproducibility and stability of the devices (shown as Fig. S10 in the ESM). Specifically, the current–voltage (I–V) characteristics of multiple NVCT devices integrated with perovskite SCs and those of bare NVCT devices were compared, as shown in Figs. S10(a) and S10(b) in the ESM. Statistical analysis of the emission current and turn-on voltage for both groups was conducted. As summarized in Fig. S10(c) in the ESM, most perovskite-based devices exhibit emission currents in the range of 2–5 μA with turn-on voltages of approximately 6 V, which are significantly improved compared to the bare devices. Figure S10(d) in the ESM presents the I–T characteristics measured under a constant bias (V_{sd} = 10 V). After continuous operation for 30 min, the performance of the device can still be maintained at approximately 85% of its initial value. This slight degradation is attributed to device heating induced by prolonged field emission,

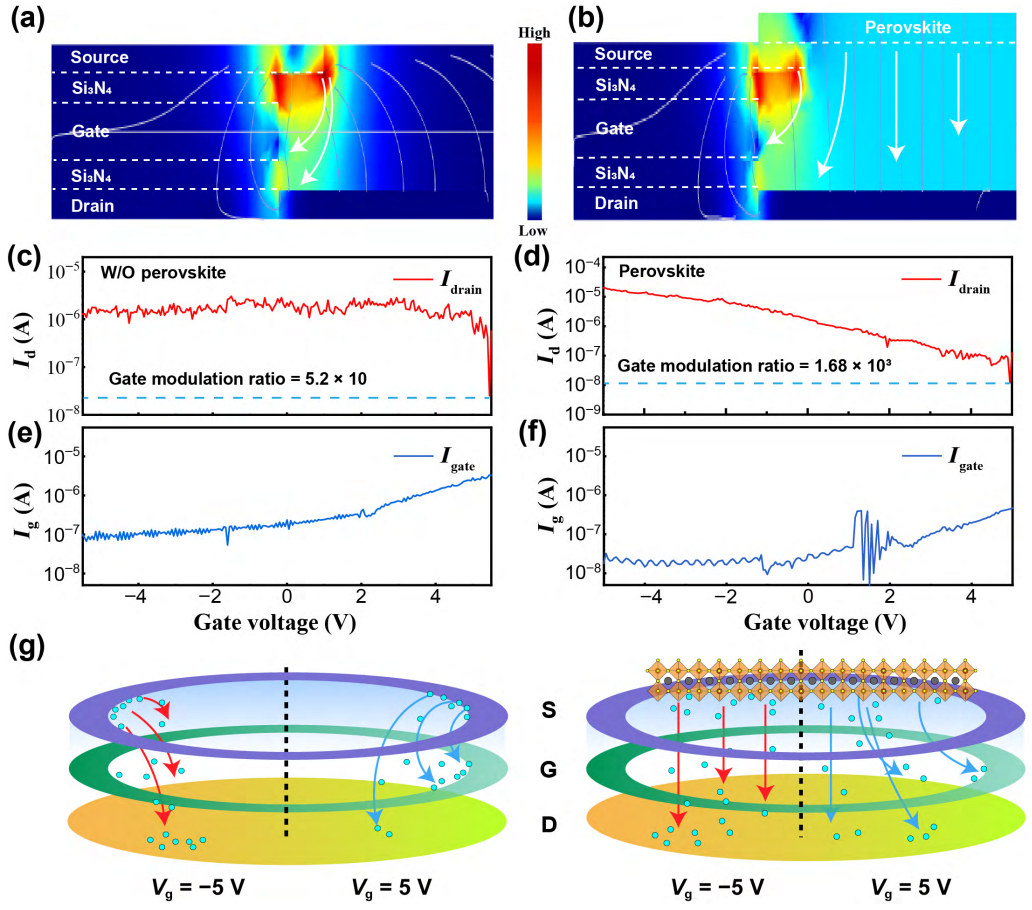

Figure 4 (a) Simulated cross-sectional electric-field distribution of the bare-metal device, (b) simulated cross-sectional electric-field distribution of the perovskite-assisted device; ((c) and (e)) I_d–V_g and I_g–V_g characteristics of the device without perovskite; ((d) and (f)) I_d–V_g and I_g–V_g characteristics of the device with perovskite; and (g) schematic illustration of the gate-control mechanism.

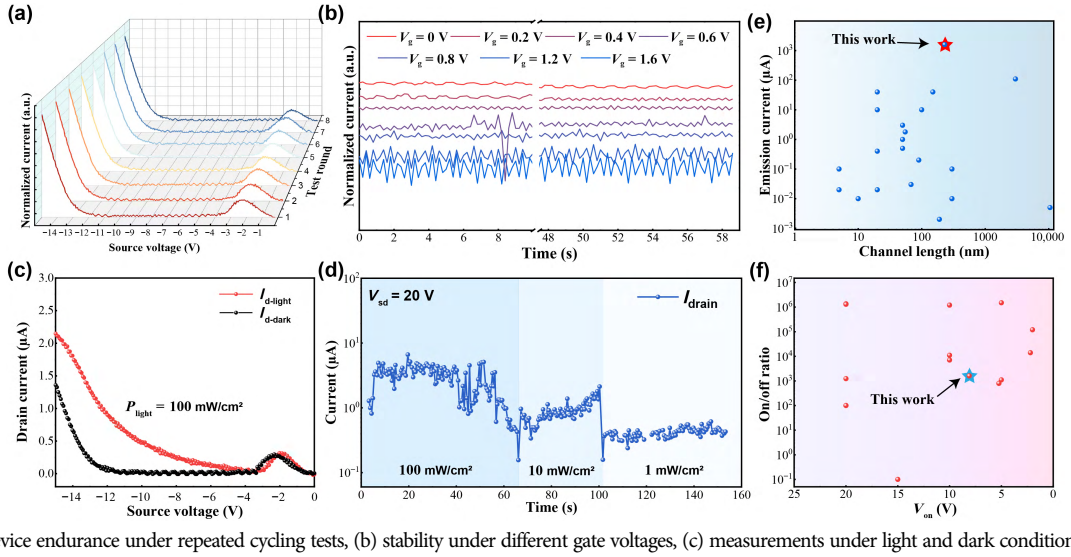

Figure 5 (a) Device endurance under repeated cycling tests, (b) stability under different gate voltages, (c) measurements under light and dark conditions, (d) I_d–t curves at various illumination intensities, and ((e) and (f)) performance comparison with previously reported devices.

which may affect the emission behavior. Figure 5(e) compares the emission currents of devices with different channel lengths reported from literature, clearly showing that our perovskite NVCT delivers a much higher emission current, even at relatively longer channel lengths. As further illustrated in Fig. 5(f), the device also exhibits a low turn-on voltage and a favorable on/off ratio. Detailed performance parameters are summarized in Table 1. NVCT device geometries are highly diverse, and performance differences reported across the literature are often jointly influenced by local field enhancement, device dimensions, and measurement conditions. Therefore, Table 1 is intended primarily to compare representative metrics of electron-emission capability; cross-geometry

Table 1 Comparison of device performance from recent reports

Device structure	Cathode material	Channel length (nm)	Turn-on voltage (V)	Emission current	On/off ratio	References
Planar back-gate	SOI-Si	— (< 20)	< 20	40 μA	10^6	[12]
Planar back-gate	Graphene	~ 90	< 20	~ 200 nA	10^2	[19]
Planar side-gate	Au	— (< 20)	< 20	~ 400 nA	10^3	[40]
Planar back-gate	Au	< 5	< 5	~ 100 nA	10^3	[11]
Layered geometry	Si	68	10	30 nA	—	[41]
Lateral geometry	Si	190	2	1–4 nA	—	[42]
Lateral device	Diamond	10,500	15	5 nA	0.1	[43]
In-plane collection	Metal	< 10 V	< 10	10 nA	> 10^4	[44]
Lateral geometry	SiC	20	5	22.3 nA	—	[45]
Planar transistor	Si	150	2	—	10^5	[46]
Gate-all-around nanowire	Si	50	5	500 nA	10^3	[8]
Gate-all-around	N-Si	3000	< 2.2	> 110 μA	10^4	[47]
Vertical transistor	Graphene	300	< 5	100 nA	10^6	[48]
Vertical transistor	SiC	— (< 20)	< 20	~ 10 μA	10^2	[22]
Planar nanodiode	GaN	30	0.24	0.5μA	—	[49]
Vacuum tunneling transistor	Au	50	10	3 μA	10^4	[10]
Vertical transistor	Mo	55	0.24	10 μA	10^3	[50]
Planar side-gate	Au	7000	10	100 nA	—	[51]
Vertical transistor	Perovskite	230	8.1	1.26 mA	10^3	This work

comparisons are provided for reference only and should not be interpreted as indicating structural superiority. Although this work focuses primarily on facet-dependent emission and gate electrostatic control, the halide perovskite cathode intrinsically provides an additional photo-responsive degree of freedom. Under optical excitation, photogenerated carriers, surface-state filling, and light-induced ionic redistribution jointly reduce the effective emission barrier of the perovskite surface. As a result, the emission current can be modulated simultaneously by gate voltage and light illumination, enabling a conceptual dual-input logic scheme.

4 Conclusions

In conclusion, we have demonstrated the first use of halide perovskite single crystals as efficient electron emitters in nano vacuum channel transistors. Owing to ion-migration-induced surface state modulation, which lowers the emission barrier, the devices achieved milliampere-level currents and low turn-on voltages under ambient conditions, even with wide vacuum channels. The NVCTs showed robust gate control, low leakage, cycling stability, and strong photo response, all realized through low-cost, scalable fabrication processes on glass substrates. This work established halide perovskites as a promising platform for multifunctional vacuum electronics and pointed to a disruptive pathway toward next-generation nano vacuum technologies for high-frequency communication, extreme-environment operation, and optoelectronic integration.

Electronic Supplementary Material: Supplementary material (including the derivation and validation of the Fowler–Nordheim formalism, device cross-sectional schematics, full XPS survey spectra, and the screening with preliminary characterization of electrode materials) is available in the online version of this article at https://doi.org/10.26599/NR.2026.94908436.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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None.

Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

X. Y. P.: Conceptualization, methodology, investigation, data curation, writing – original draft. Y. C. L.: Investigation, validation, formal analysis. X. D. G.: Visualization, resources, writing – review & editing. C. Z.: Software, simulation, data curation. F. J.: Supervision, project administration, funding acquisition. Y. Z. L.: Conceptualization, supervision, writing – review & editing, funding acquisition. All authors have read and approved the final manuscript.

Use of AI statement

None.

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