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High-performance carbon nanotube thin-film transistors via atomic layer etching-assisted, resist-contamination-free fabrication

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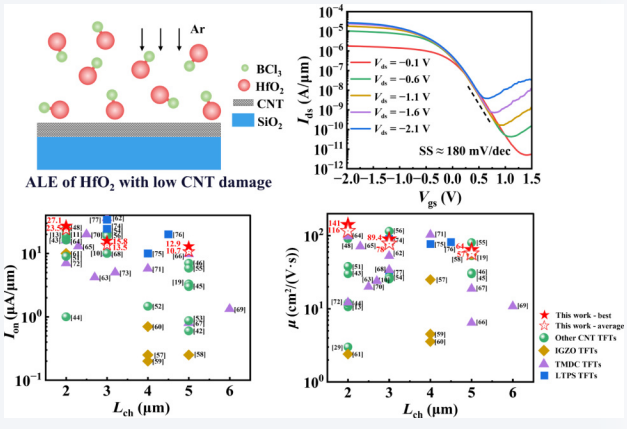
ABSTRACT: Carbon nanotubes (CNTs) offer exceptional electronic properties, making them promising candidates for high-performance thin-film transistor (TFT) applications. However, conventional fabrication exposes CNT surfaces to resists, leaving persistent residues that degrade dielectric and contact interfaces, resulting in reduced on-state current, lower mobility, poor subthreshold swing, and device nonuniformity. Existing approaches, including ultraviolet-ozone treatment, wet etching, or sacrificial layers, partially mitigate contamination but cannot fully eliminate residues and often limit device scaling. Here, we introduce a fabrication process for top-gate CNT TFTs that achieves resist-contamination-free interfaces using atomic layer etching (ALE) technology. A Y_2O_3 sacrificial layer defines the active region, enabling high-quality atomic layer deposition of the gate dielectric. Selective ALE precisely etches the dielectric above source/drain regions, with Ar plasma power tuned to minimize damage to underlying CNTs, yielding excellent metal contacts. CNT TFTs fabricated with this approach demonstrate a maximum on-state current of 27.1 μA/μm and peak mobility of 141 cm²/(V·s) at a channel length of 2 μm, and also exhibit excellent performance uniformity, low contact resistance, and low interface trap density. These devices surpass other CNT, low-temperature polycrystalline silicon (LTPS), indium-gallium-zinc-oxide (IGZO), and transition metal dichalcogenide (TMDC) TFTs in performance, scalability, and process simplicity. This work provides a scalable pathway towards high-performance CNT TFTs and also suggests potential for miniaturized transistors, as ALE's vertical, highly directional etch preserves lateral dimensions.



KEYWORDS: carbon nanotubes, thin-film transistors, atomic layer etching, sacrificial layer, resist-contamination-free

1 Introduction

Carbon nanotubes (CNTs), owing to their unique one-dimensional tubular structure, exhibit outstanding electronic properties, including high carrier mobility, excellent gate control efficiency, large current-carrying capability, and low intrinsic capacitance [1–4]. Thin-film transistors (TFTs) using CNT network films as the channel are compatible with large-area fabrication and both rigid and flexible substrates, making them promising candidates for various applications [5, 6]. Prototype demonstrations, including CNT-TFT-driven organic light-emitting diodes (OLEDs) [7, 8], mini- and micro-LEDs (μLEDs) [9–11], flexible and printed circuits [12–15], and sensors [16–18], have already been realized. Despite

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these advances, key performance metrics such as on-state current (I_{on}) and mobility (μ) still lag behind or only marginally surpass those of commercially-available low-temperature polycrystalline silicon (LTPS) or metal oxide (e.g., indium-gallium-zinc-oxide (IGZO)) TFTs, limiting their practical adoption.

The performance of CNT transistors is primarily governed by the quality of the dielectric and contact interfaces [3, 4, 19, 20]. In conventional fabrication, resist is typically used to protect CNTs within the active region. Plasma etching is then applied to remove CNTs outside this area, followed by resist stripping and cleaning. Source/drain (S/D) contacts are subsequently defined by spin-coating resist across the wafer, patterning by exposure and development, and performing metal evaporation and lift-off. During these two critical processes, the CNT film, covering both channel and contact regions, comes into contact with resist at least twice. Because of strong interactions between CNTs and resist materials, common solvents such as acetone or N-methyl-2-pyrrolidone (NMP) cannot fully remove resist residues, leaving persistent contamination on CNT surfaces [21, 22]. Resist residues in the channel region introduce a high interface trap density (D_{it}) and additional scattering centers, which interface with atomic layer deposition (ALD) of the gate dielectric and degrade device performance. These effects manifest as increased subthreshold swing (SS), pronounced hysteresis, reduced on/off ratio (I_{on}/I_{off}), and lowered mobility. In severe cases, the dielectric leakage or complete device failure can occur. Resist residues in the contact region form a non-conductive interfacial layer between the CNTs and metal electrodes, increasing the tunneling barrier and contact resistance (R_c) [23]. Moreover, oxidative functional groups within resist residues can oxidize low-work-function metals used for n-type CNT transistors, leading to the device degradation or failure [3, 24]. Collectively, the resist contamination in both channel and contact regions introduces non-uniformities in CNT films, resulting in significant device-to-device, die-to-die, and wafer-to-wafer variability, a major obstacle to large-scale integration. Several strategies have been explored to mitigate these issues. Huang et al. employed a ultraviolet–ozone (UVO) treatment to reduce resist residues, resulting in moderate improvements in I_{on} and μ while preserving CNT morphology [25]. Performance enhancements were nevertheless limited to ~ 15%, likely because the channels still contacted resist during fabrication. Tian et al. utilized wet-etched Y_2O_3/Al or Al_2O_3/Al gate stacks and Cu or Co contacts to form CNT TFTs [26]. Due to the inherent lateral etch associated with wet processing, relatively large gate-to-contact spacing was required, leaving CNTs in these regions exposed to resist during lithography. In addition, challenges in achieving good wettability between Cu/Co and CNTs made it difficult to form high-quality contacts. Zhang et al. introduced a germanium (Ge) sacrificial layer to shield CNTs from resist exposure, enabling reduced R_c after selective Ge wet-etching [27]. However, CNTs still experienced the resist contact during active-area definition, and overall performance remained comparable to leading lift-off-based CNT transistors [4, 28]. Li et al. employed an Al protective layer and wet etching to realize resist-free contacts, and reported modest improvements in SS and mobility [29]. In summary, no existing fabrication approach has fully eliminated resist contamination across both channel and contact regions while maintaining compatibility with device scaling, representing a key bottleneck to achieving high-performance CNT transistor technologies.

This work presents a fabrication process for CNT TFTs based on atomic layer etching (ALE) that completely eliminates resist-induced contaminations to CNTs. The process employs a Y_2O_3 sacrificial layer to define the CNT active region, providing a pristine interface for ALD of the gate dielectric. Concurrently, ALE is used to selectively remove the gate dielectric layer above the S/D regions. By precisely tuning the Ar plasma energy, the process minimizes damage to the underlying CNTs and enables the formation of high-quality metal–CNT contacts. CNT TFTs fabricated using this approach demonstrate a maximum I_{on} of 27.1 μA/μm and a peak μ of 141 $cm^2/(V·s)$ at a channel length (L_{ch}) of 2 μm, along with excellent performance uniformity, low D_{it}, and low R_c. These devices outperform previously reported CNT, LTPS, IGZO, and transition metal dichalcogenide (TMDC) TFTs with comparable device dimensions. This work provides a scalable route toward high-performance CNT TFTs and also offers key insights for CNT transistor scaling at advanced technology nodes.

2 Results and discussion

2.1 ALE-assisted, resist-contamination-free fabrication of CNT TFTs

Figure 1(a) illustrates the ALE-assisted fabrication process for CNT TFTs, which completely avoids the resist contamination of the CNTs. A CNT network film is first deposited on a substrate with alignment markers. An yttrium (Y) layer is then deposited and fully oxidized to Y_2O_3, serving as a sacrificial layer that defines the active region. Standard photolithography is performed on the Y_2O_3, where the protected area corresponds to the intended active region. The unprotected Y_2O_3 is selectively removed in diluted hydrochloric acid (HCl), followed by oxygen (O_2) plasma etching to eliminate exposed CNTs outside the active area. After resist stripping, the remaining Y_2O_3 above the active region is removed by diluted HCl, yielding exceptionally clean CNTs (Figs. 1(d) and 1(g)). The Y_2O_3 sacrificial layer not only prevents CNT–resist contact but also partially removes polymer wrappers introduced during semiconducting CNT sorting, producing pristine CNT surfaces that are crucial for subsequent dielectric deposition [22, 30]. The lateral undercut of Y_2O_3 inherent to HCl wet etching is acceptable because the active region includes both the channel and contacts with relatively large dimensions. For future device scaling, dry-etching approaches such as ion beam etching (IBE) or reactive ion etching (RIE) could be used to minimize lateral loss. Subsequently, the gate dielectric layer is deposited by ALD. Because CNTs have never been exposed to resist, their clean surfaces enable uniform and high-quality dielectric growth with low D_{it}. A high-temperature post-deposition anneal (PDA) can be further applied to optimize interface quality, because no metal contacts are yet present. Next, the gate electrode is formed by standard photolithography, electron-beam evaporation (EBE), and lift-off. A subsequent lithography step defines the S/D regions, after which ALE is employed to selectively remove the exposed dielectric with minimal damage to the underlying CNTs. Finally, S/D metals are deposited by EBE and patterned by lift-off to form contacts. Compared with conventional S/D patterning where CNTs directly contact resist, this approach yields a much cleaner CNT–metal interface and substantially reduce R_c. In addition, because ALE is inherently vertical and does not induce lateral etch, it minimizes ungated access regions between the gate and S/D, supporting the device scaling. Overall, the process prevents CNTs from contacting resist at any stage and ensures high-

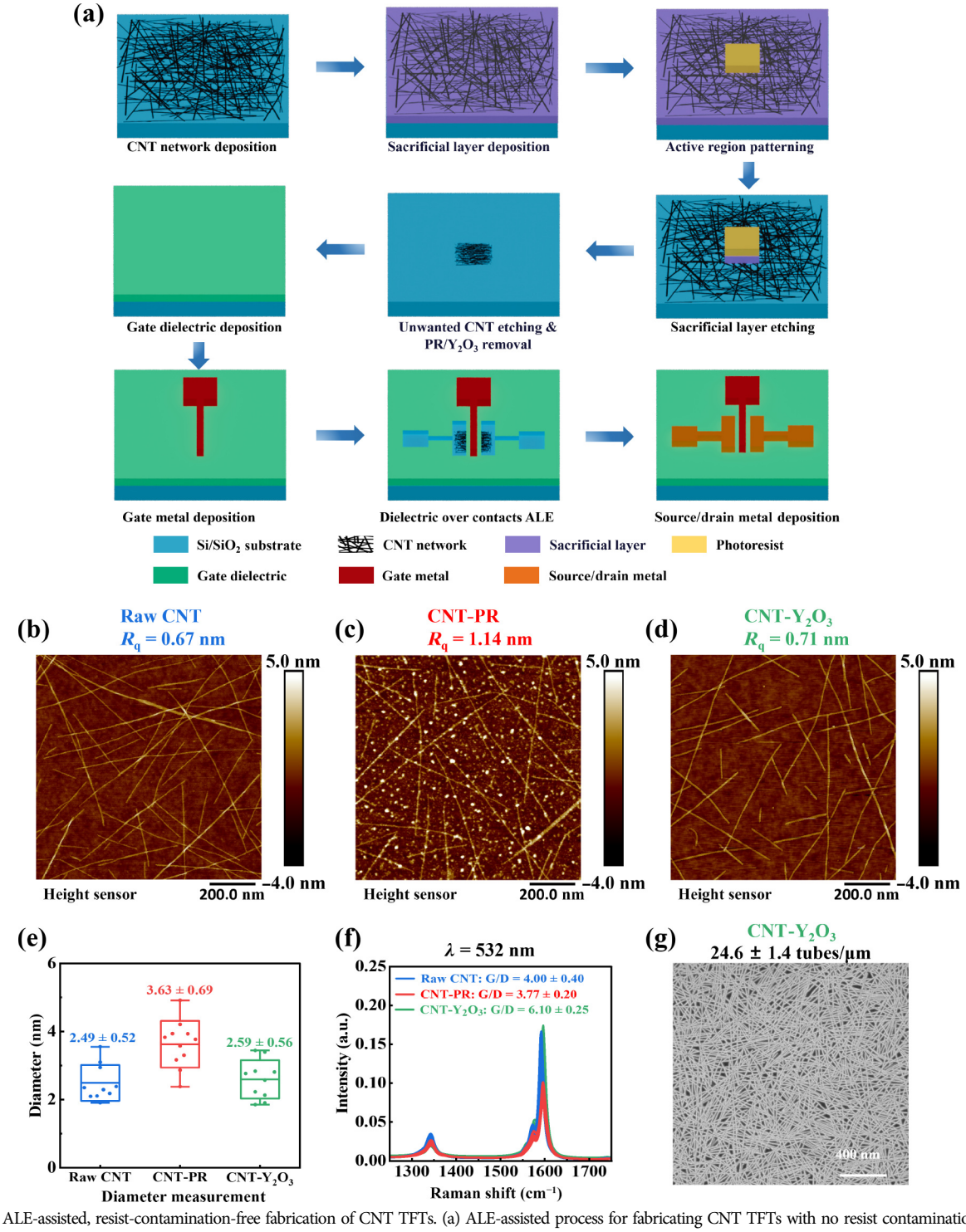

Figure 1 ALE-assisted, resist-contamination-free fabrication of CNT TFTs. (a) ALE-assisted process for fabricating CNT TFTs with no resist contamination to CNTs. Representative AFM images of (b) the "raw CNT", (c) "CNT-PR", and (d) "CNT-Y_2O_3". (e) Statistics of diameters corresponding to CNTs in (b)–(d). (f) Raman spectra of CNTs in (b)–(d) measured using 532 nm laser. The intensities are normalized to Si peak at 520 cm^{-1}. (g) Representative SEM image of CNT network film after active region definition using the Y_2O_3 sacrificial layer process.

quality CNT–dielectric and CNT–metal interfaces while remaining compatible with further scaling of CNT transistors.

Figure 1(b)–1(d) show representative atomic force microscopy (AFM) images of the as-deposited and annealed CNT network film ("raw CNT"), "raw CNT" after photolithograph process ("CNT-PR"), and "raw CNT" after Y_2O_3 coating and removal ("CNT-Y_2O_3"), respectively. CNT network films with a density of ~ 10 tubes/μm were used for the AFM characterizations to accurately measure their diameters. The corresponding CNT diameter statistics are summarized in Fig. 1(e). The "raw CNT" sample exhibits an average diameter of 2.49 ± 0.52 nm and a root-mean-square roughness (R_q) of 0.67 nm. In contrast, CNTs in the "CNT-PR" sample exhibit pronounced thickening due to resist residues, with the average diameter increasing to 3.63 ± 0.69 nm

and R_q to 1.14 nm. Meanwhile, CNTs in the "CNT-Y_2O_3" sample retain sharp AFM features, with an average diameter of 2.59 ± 0.56 nm and R_q of 0.71 nm, both statistically indistinguishable from those of the "raw CNT" sample. Figure 1(f) displays the Raman spectra of the corresponding CNT network films, with enlarged spectral details shown in Fig. S1 in the Electronic Supplementary Material (ESM). The "CNT-PR" sample shows a noticeable decrease in the G-peak to D-peak ratio (G/D ratio), indicating the degradation of the sp^2 electronic structure of CNTs. In contrast, the "CNT-Y_2O_3" sample exhibits an increase in G/D ratio, consistent with reports that Y_2O_3 can partially remove polymer wrappers and improve CNT quality [22, 30]. Figure 1(g) shows a representative scanning electron microscopy (SEM) image of CNT network films with a density of ~ 24 tubes/μm after active region definition using the Y_2O_3 sacrificial layer process, revealing uniformly distributed CNTs with sharp surface morphology. These results confirm that employing Y_2O_3 sacrificial layer effectively preserves CNT structure and uniformity while improving the surface cleanliness.

2.2 Low-damage ALE for CNTs

ALE is an emerging high-precision etching technique in the semiconductor industry. Its ability to achieve atomic-scale precision is particularly important for integrated circuit (IC) fabrication at advanced technology nodes. Compared with conventional dry-etching techniques such as IBE or RIE, ALE proceeds through self-limiting cyclic reactions that remove material in a layer-by-layer manner, offering superior process controllability and etching selectivity [31–33]. Figure 2(a) illustrates the ALE process used to selectively remove the hafnium oxide (HfO_2) gate dielectric above the S/D regions of CNT TFTs. In the first step, the reactive precursor boron trichloride (BCl_3) is introduced and chemisorbs on the HfO_2 surface, converting the top atomic layers into a chlorinated layer that can be subsequently removed. After an Ar purge removes unreacted BCl_3, Ar plasma with carefully tuned ion energy is applied to physically desorb ("bombard") the modified surface layer. Due to the highly directional ion bombardment, lateral etching is strongly suppressed, resulting in vertical sidewall profiles desirable for device scaling. Furthermore, precise ion energy control ensures that only the reacted surface layer is removed, minimizing disturbance to the underlying HfO_2 lattice. Finally, Ar purge removes etch byproducts and completes a single ALE cycle. By repeating these steps, HfO_2 can be etched with atomic-scale precision, and the total number of cycles can be adjusted according to the target thickness. Figure S2 in the ESM shows the etch rates of HfO_2 under various substrate bias voltages, corresponding to different ion energies. The process exhibits the self-limiting characteristics of ALE, with a constant thickness of HfO_2 removed per cycle at a given bias voltage. Moreover, the etch rate increases with increasing bias voltage, which is attributed to enhanced physical ion bombardment from the Ar plasma. Importantly, for the final ALE cycles near the CNT interface, precise tuning of Ar plasma energy is required to fully remove HfO_2 while minimizing

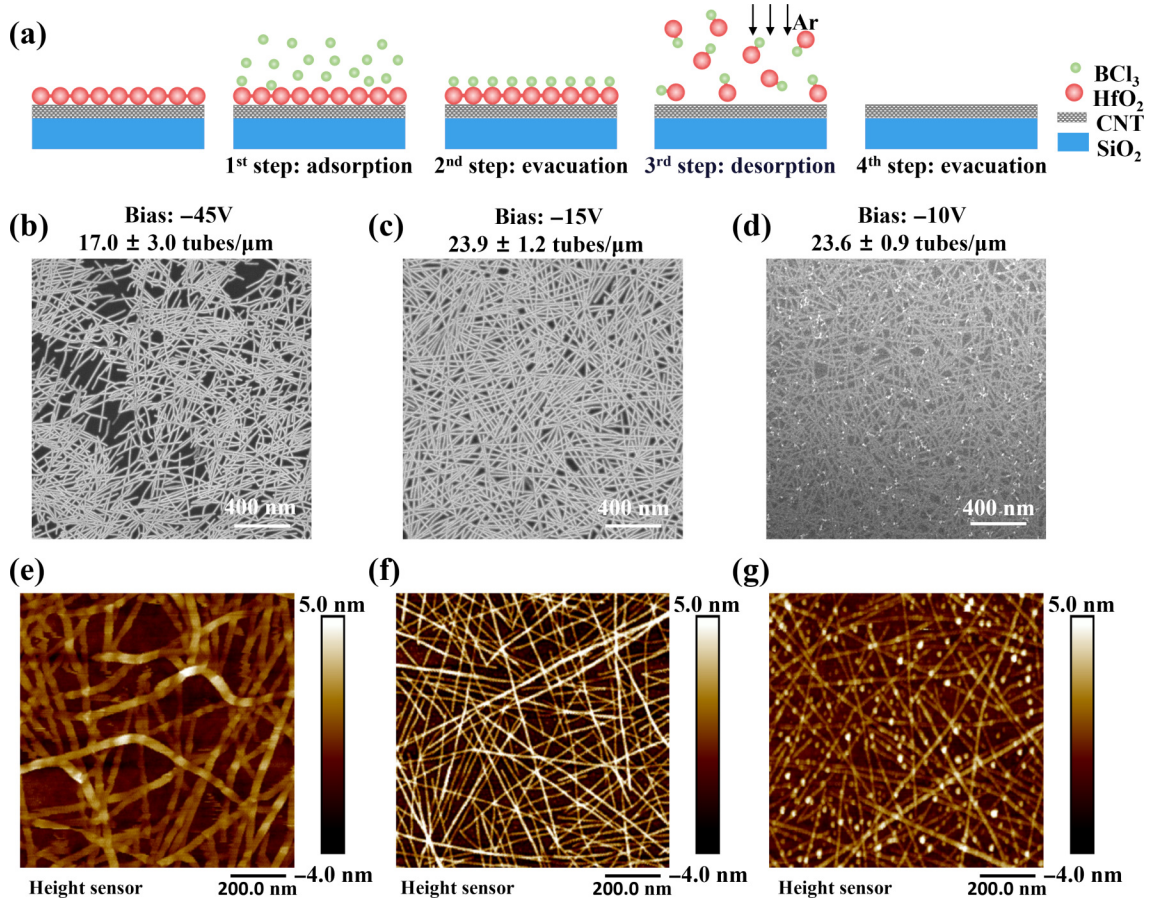

Figure 2 Low-damage ALE for CNTs. (a) Schematic illustration of layer-by-layer ALE removal of the HfO_2 dielectric above the CNT S/D regions. SEM images of CNT network films after identical ALE cycles performed under (b) high (–45 V), (c) medium (–15 V), and (d) low (–10 V) substrate bias voltages. ((e)–(g)) Corresponding AFM images of the samples in (b)–(d).

damage to the CNTs, a key challenge when processing low-dimensional materials that consist of only a few atomic layers (e.g., MoS_2) or even a single atomic layer (e.g., CNTs) [34–36].

Key ALE parameters include the BCl_3 reaction time and gas flow, the Ar plasma bombardment energy and duration, and the total number of etching cycles. Among these, Ar plasma energy is the most critical for fully removing the HfO_2 dielectric while minimizing CNT damage, and is precisely controlled by the substrate bias voltage. Figures 2(b)–2(d) and 2(e)–2(g) show the SEM and AFM images of CNT network films subject to identical ALE cycles under high (−45 V), medium (−15 V), and low (−10 V) substrate bias voltages. Under high bias voltage (−45 V), the CNT network suffers severe damage, with the density reduced from ~ 24 to 17.0 tubes/μm and pronounced non-uniformity. Under low bias voltage (−10 V), the CNT density and uniformity are preserved, but residual HfO_2 particles remain on the surface. At medium bias voltage (−15 V), no visible HfO_2 residue is observed, and the CNT density and uniformity are well maintained. The complete removal of HfO_2 is further confirmed by chemical analysis of the cross-section of a contact structure using transmission electron microscopy (TEM) combined with energy dispersive X-ray spectroscopy (EDS), as shown in Fig. S3 in the ESM. No Hf signal is detected, confirming the complete removal of HfO_2 within the detection limits of EDS (~ 100 ppm). We further evaluated plasma-induced damage to CNTs by directly subjecting the CNTs (without any HfO_2 overlayer) to two cycles of ALE under substrate bias voltages ranging from −10 to −15 V. Raman spectra (Fig. S4 in the ESM) show that the G/D ratio remains a similar level for substrate bias voltages between −10 and −12 V, and decreases slightly for bias voltages of −13 to −15 V, suggesting only a marginal increase in CNT damage at higher bias voltages. Overall, the degree of damage remains comparable across the investigated bias range. Considering the need for complete removal of HfO_2 to achieve good electrical contacts, a substrate bias voltage of −15 V was selected as the optimal condition. These results indicate that the medium-energy Ar plasma enables complete HfO_2 removal while suppressing CNT structural damage. Although lowering plasma energy mitigates the CNT damage, it slows the HfO_2 etch rate and may even destabilize the plasma. Therefore, a combined strategy of high-energy pre-etch followed by medium-energy fine etch is adopted: Most of the HfO_2 is rapidly removed using high-energy plasma, and the remaining dielectric near the CNT interface is cleared using medium-energy plasma. Because medium-energy plasmas still contain a fraction of high-energy species that can damage CNTs, the number of ALE over-etch cycles near the CNT interface must be carefully controlled to balance complete HfO_2 removal with the preservation of CNT structural integrity (Fig. S5 in the ESM for details).

2.3 Characterizations of CNT TFTs fabricated via ALE-assisted, resist-contamination-free processing

CNT TFTs with various L_{ch} were fabricated following the process flow in Fig. 1(a), with detailed procedures provided in Section 4. Figures 3(a) and 3(b) show optical microscope and SEM images of a representative device with a nominal L_{ch} of 2 μm. Due to lithographic and alignment limitations, the actual L_{ch} is ~ 1.8 μm, and ~ 200 nm of access regions are present between the gate and S/D electrodes on each side. Importantly, CNTs in the access regions also remain free of resist exposure. These non-active access regions can significantly affect the performance of CNT TFTs. The lengths of these regions can be reduced by integrating spacers, whose thickness corresponds to the access region length and can be

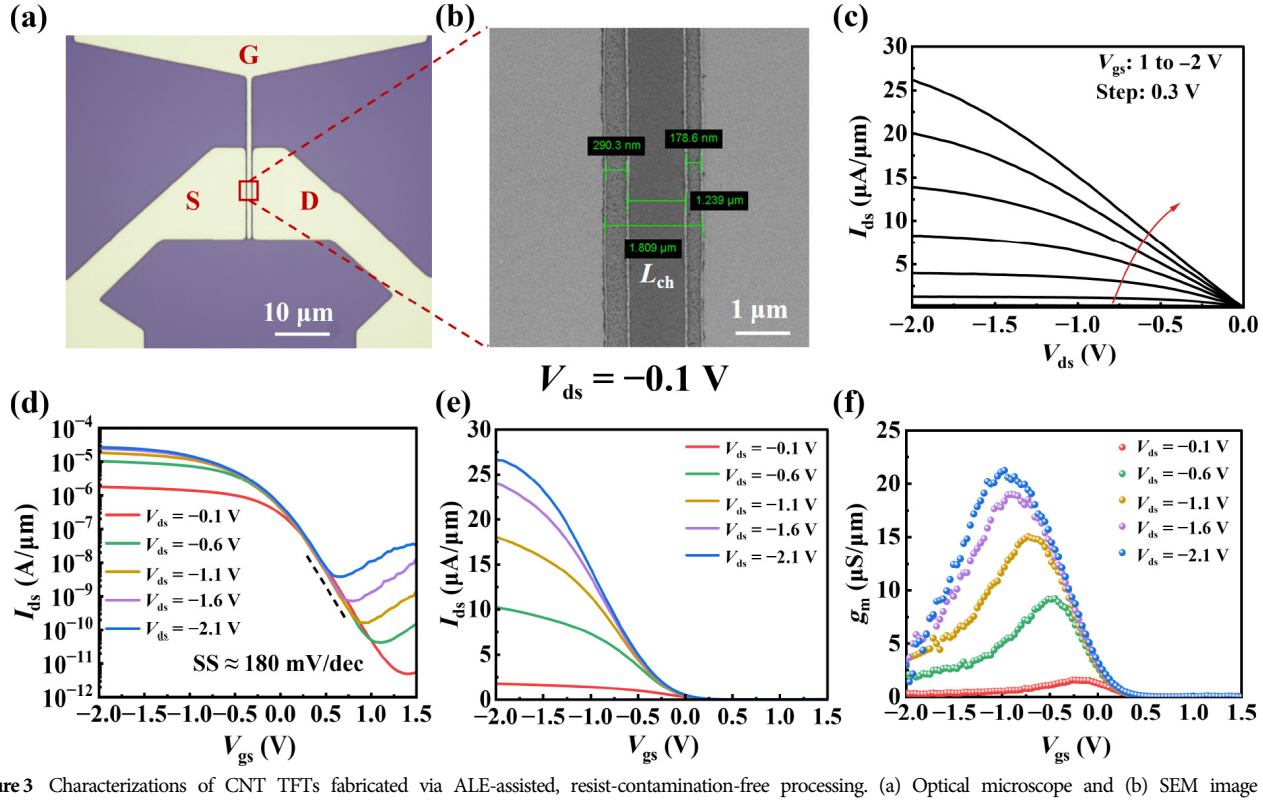

Figure 3 Characterizations of CNT TFTs fabricated via ALE-assisted, resist-contamination-free processing. (a) Optical microscope and (b) SEM image of a representative CNT TFT with a nominal L_{ch} of approximately 2 μm. Electrical characteristics of the device in (a) and (b): (c) output characteristics, (d) transfer characteristics in log and (e) linear scales, and (f) transconductance as a function of V_{gs}.

precisely controlled using plasma-enhanced chemical vapor deposition (PECVD), thereby alleviating the requirements for photolithographic alignment. Additionally, the incorporation of spacers enables the extension doping and self-aligned source and drain patterning, further enhancing the overall performance of CNT TFTs [37, 38]. Figures 3(c)–3(f) summarize the electrical characteristics of the device in Figs. 3(a) and 3(b), including output characteristics (Fig. 3(c)), transfer characteristics in log (Fig. 3(d)) and linear (Fig. 3(e)) scales, and transconductance (g_m) as a function of gate-to-source voltage (V_{gs}, Fig. 3(f)). The CNT TFT exhibits typical p-type behavior with ohmic contacts and clear current saturation. At a drain-to-source voltage (V_{ds}) of −2.1 V, it delivers ion of 26.7 μA/μm, g_m of 21.5 μS/μm, and I_{on}/I_{off} of 7×10^3. In addition, the device shows a low SS of 180 mV/dec, high μ of 115 $cm^2/(V{\cdot}s)$, low drain-induced barrier lowering (DIBL) of 0.24 V/V, and small hysteresis (Fig. S6 in the ESM). Parameter extraction methods are described in the ESM. Figure S6 in the ESM also presents the transfer and output characteristics of representative CNT TFTs with L_{ch} of 3 and 5 μm, which similarly exhibit excellent electrical performance. Overall, these results highlight the effectiveness of the ALE-assisted, resist-contamination-free process in enabling high performance CNT TFTs.

CNT TFTs fabricated using the ALE-assisted and resist-contamination-free process also exhibit excellent performance uniformity. Figures 4(a)–4(c) show the transfer characteristics of devices with L_{ch} of 2 (40 devices), 3 (18 devices), and 5 μm (24 devices) measured at V_{ds} of −0.1 and −2.1 V. Figures 4(d)–4(i) summarize statistics of key device parameters, including I_{on} (Fig. 4(d)), μ (Fig. 4(e)), I_{on}/I_{off} (Fig. 4(f)), threshold voltage (V_{th}, Fig. 4(g)), g_m (Fig. 4(h)), and hysteresis voltage (V_{hyst}, Fig. 4(i)). As shown in Fig. 4(d), under V_{ds} = −2.1 V, the peak I_{on} values for devices with L_{ch} of 2, 3, and 5 μm are 27.1, 15.8, and 12.9 μA/μm, with averages of 23.5, 13.5, and 10.7 μA/μm, respectively. This trend reflects the expected I_{on} enhancement with L_{ch} scaling. Mobility μ is extracted using peak transconductance method, where the gate capacitance per unit area (C_{ox}) is determined using two approaches. The first ($C_{calculated}$) calculates C_{ox} from the measured HfO_2 dielectric constant (via metal–insulator–metal (MIM) structure) together

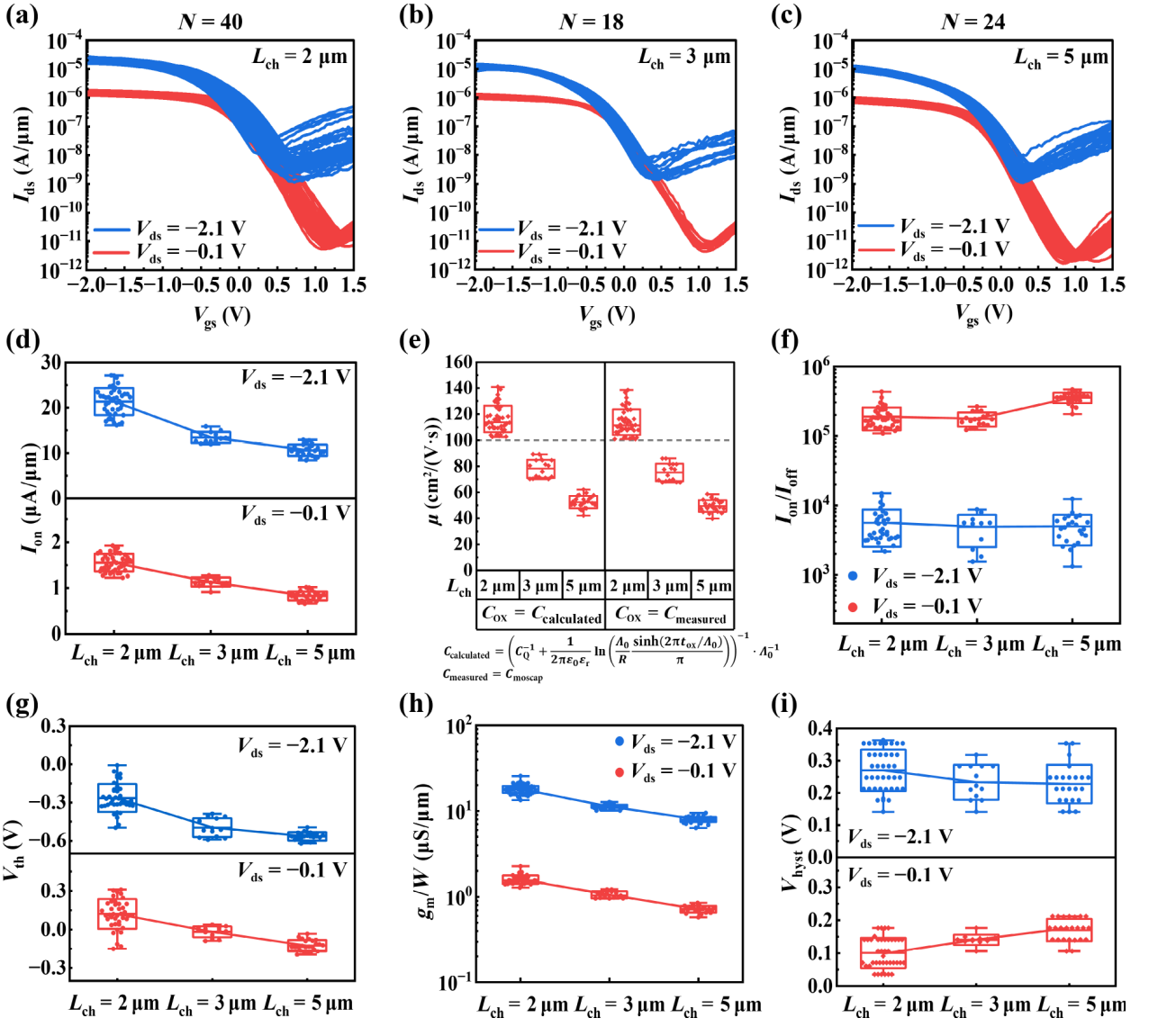

Figure 4 Uniformity of CNT TFTs fabricated via ALE-assisted, resist-contamination-free process. Transfer characteristics of the CNT TFTs with L_{ch} of (a) 2, (b) 3, and (c) 5 μm, measured at V_{ds} = −0.1 V and V_{ds} = −2.1 V. Statistics of key device parameters corresponding to (a)–(c): (d) I_{on}, (e) μ, (f) I_{on}/I_{off}, (g) V_{th}, (h) g_m, and (i) V_{hyst}.

with an average CNT diameter of ~ 1.5 nm, CNT density of ~ 24 tubes/μm, CNT quantum capacitance (C_Q) of 3.47 × 10^{-10} F, and dielectric thickness (t_{ox}) of 7 nm. The second ($C_{measured}$) uses the maximum capacitance in strong accumulation from *C*–*V* measurements of CNT metal-oxide-semiconductor capacitors (MOSCAPs), which includes contributions from both gate dielectric capacitance and CNT quantum capacitance. Detailed C_{ox} characterization results are provided in Fig. S7 in the ESM. As shown in Fig. 4(e), peak μ values for L_{ch} of 2, 3, and 5 μm are 141, 89.4, and 64 $cm^2/(V·s)$, with averages of 116, 78, and 57 $cm^2/(V·s)$, respectively. The excellent agreement between the two C_{ox} determinations confirms the reliability of the mobility extraction. The reduction of mobility with increasing L_{ch} can be mainly attributed to percolative transport through the CNT network. As L_{ch} increases from a value comparable to the nanotube length to larger values, more tube-to-tube junctions are introduced into the conduction path, leading to a decrease in device mobility. Figure 4(f) shows I_{on}/I_{off} exceeding 10^5 for all devices at V_{ds} = −0.1 V. Although I_{on}/I_{off} decreases at V_{ds} = −2.1 V due to DIBL, it remains greater than 10^3. As shown in Fig. 4(g), V_{th} shifts positively with reduced L_{ch}, consistent with V_{th} roll-off from enhanced lateral electric fields during device scaling. Figure 4(h) shows that peak g_m values for L_{ch} of 2, 3, and 5 μm are 25.6, 12.8, and 9.5 μS/μm, with averages of 18, 11.3, and 8 μS/μm, respectively. As shown in Fig. 4(i), V_{hyst} is less than 0.22 and 0.37 V for V_{ds} of −0.1 and −2.1 V, respectively, indicating a low density of interface traps and weak charge trapping effects [19, 39].

The excellent performance and uniformity of these CNT TFTs stem primarily from the ALE-assisted, resist-contamination-free process, which substantially improves both the gate dielectric and S/D contact interfaces. R_c, extracted using the transmission line method (TLM), is 8.5 ± 3.25 kΩ·μm (Fig. S8 in the ESM), among the lowest reported for CNT network TFTs (Table S1 in the ESM) [29, 40–48]. In addition, the top-gate structure avoids contact-gating effects [49, 50]. The minimum D_{it}, extracted from *C*–*V* measurements of CNT MOSCAPs using the conductance method, ranges from 1.1 × 10^{11} to 3.5 × 10^{11} eV/cm^2 (Fig. S9 in the ESM), also among the lowest values reported for CNT TFTs [19, 20]. Across devices with different L_{ch}, D_{it} remains below 1.5 × 10^{12} eV/cm^2 within the operating voltage range (V_{gs} = −2 to 1.5 V), contributing to the relatively low V_{hyst} and SS. To evaluate the long-term stability and reliability of our devices, bias stress testing was performed (Fig. S10 in the ESM). Under positive bias stress (PBS) at an electric field of 1.25 MV/cm for 1000 s, the V_{th} shift is approximately −0.2 V, whereas under negative bias stress (NBS) at the same field and duration, the V_{th} shift is about +0.05 V. The bias stress stability of the devices may be further improved through the optimization of the gate dielectric growth process and PDA conditions.

2.4 Performance benchmarking

Figure 5 benchmarks ALE-assisted, resist-contamination-free fabricated CNT TFTs against previously reported CNT TFTs [10, 11, 13, 19, 29, 42–46, 48, 51–56], IGZO TFTs [57–61], TMDC TFTs [62–73], and LTPS TFTs [74–77]. Details are provided in Table S2 in the ESM. As shown in Fig. 5(a), I_{on} of our CNT TFTs exceeds most reported CNT and TMDC TFTs, surpasses IGZO TFTs, and is only slightly lower than state-of-the-art LTPS TFTs. CNT and MoS_2 TFTs reported in Refs. [56, 62] show higher I_{on} at L_{ch} of 3 μm, but both use back-gate structures in which the contact-gating suppresses R_c and enhances I_{on} [49, 50]. However, neither includes device passivation, essential for stable operation in practical applications. Although LTPS TFTs achieve marginally higher I_{on}, their fabrication requires complex steps, including high-temperature laser crystallization and ion implantation, and further L_{ch} scaling is challenging. Our CNT TFTs also deliver excellent mobility across all L_{ch}, as shown in Fig. 5(b). Notably, when L_{ch} is reduced to 2 μm, both the maximum and average μ exceed 100 $cm^2/(V·s)$. At L_{ch} of 3 μm, the mobility surpasses that of commercial LTPS TFTs while offering advantages such as compatibility with flexible substrates, large-area processing, and simple fabrication. CNT TFTs in Refs. [55, 56] show slightly higher μ at similar L_{ch} but rely on back-gate structures without surface passivation. In summary, CNT TFTs fabricated through the ALE-assisted, resist-contamination-free process offer superior performance, scalability, and process simplicity relative to other TFT technologies. Importantly, the inherently vertical and highly directional etch profile of ALE preserves lateral dimensions, making the process naturally compatible with device miniaturization and further performance improvements at advanced technology nodes.

High-performance electronic systems generally require complementary integration of both p-type and n-type devices. Our resist-contamination-free process is also applicable to n-type CNT devices. However, their performance is currently inferior to that of p-type devices. The analysis indicates that oxidation of the low-work function scandium (Sc) at the contact interface is the primary cause (Fig. S11 in the ESM). Additionally, the ungated access regions exhibit minimal gate control, and CNTs in these regions tend to behave as p-type, forming p–n junctions near the contacts and limiting device performance. Future work will focus on

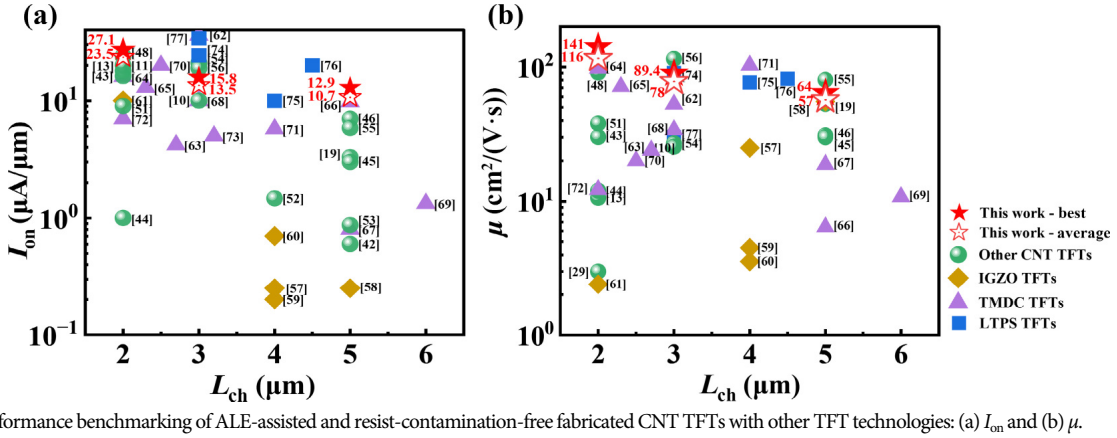

Figure 5 Performance benchmarking of ALE-assisted and resist-contamination-free fabricated CNT TFTs with other TFT technologies: (a) I_{on} and (b) μ.

mitigating Sc oxidation, reducing access region lengths, and n-doping CNTs in these regions using spacers to realize high-performance n-type CNT TFTs [37, 38].

3 Conclusions

In summary, we demonstrate high-performance CNT TFTs fabricated using an ALE-assisted, resist-contamination-free process. The approach uses a Y_2O_3 sacrificial layer to define the CNT active region and ALE to selectively remove HfO_2 above S/D electrodes with minimal damage to underlying CNTs, ensuring high-quality dielectric and contact interfaces. Top-gate CNT TFTs fabricated with this method achieve a maximum I_{on} of 27.1 μA/μm and peak μ of 141 $cm^2/(V{\cdot}s)$ at L_{ch} of 2 μm, along with excellent device uniformity, low R_c, and low D_{it}. These devices surpass other TFT technologies in performance, scalability, and process simplicity. Furthermore, the inherently vertical, highly directional ALE etch makes this process naturally compatible with miniaturized devices at advanced technology nodes, offering a pathway toward high-performance, scalable CNT electronics.

4 Methods

4.1 Preparation of high-purity semiconducting CNT solutions

High-purity semiconducting CNT solutions were prepared via polymer-wrapping extraction. Poly[9-(1-octylonyl)-9H-carbazole-2,7-diyl] (PCz) and raw arc-discharged CNTs were mixed at a 1:1 mass ratio and dispersed in toluene at 1 mg/mL, followed by tip sonication to achieve uniform dispersion. The mixture was then centrifuged twice, and the supernatant was collected for subsequent use.

4.2 ALE-assisted, resist-contamination-free fabrication of CNT TFTs

First, alignment marks (0.3/60 nm Ti/Pd) were formed on a Si/SiO_2 substrate using standard photolithography, EBE, and lift-off. The substrate was then immersed in a high-purity semiconducting CNT solution to deposit a CNT network film. Next, 3 nm of Y was deposited via EBE, and the substrate was heated at 250 °C for 30 min in air to fully oxidize Y into Y_2O_3. The active region was defined by photolithography, and the Y_2O_3 sacrificial layer outside the active region was wet-etched with diluted HCl (1:20) for 90 s. CNTs outside the active region were removed using oxygen plasma etching (100 W, 100 sccm, and 90 s). The photoresist was then stripped with NMP, followed by removal of the Y_2O_3 layer using the same HCl solution. Subsequently, 7 nm of HfO_2 was deposited as the gate dielectric via ALD at 90 °C. The gate electrode (0.3/60 nm Ti/Pd) was fabricated using standard photolithography, EBE, and lift-off. The gate dielectric over the S/D regions was exposed by photolithography and etched using ALE (BCl_3/Ar) to reveal the CNTs. Finally, S/D electrodes (0.3/60 nm Ti/Pd) were deposited via EBE and lift-off, completing the CNT TFT fabrication.

4.3 Characterizations

The electrical characteristics (I–V and C–V) of CNT TFTs, CNT MOSCAPs, and HfO_2 MIM structures were measured using a probe station (MPI TS2000SE) in combination with a semiconductor parameter analyzer (Keysight B1500A) and an impedance analyzer (Keysight E4990A). Morphology and structural characterizations were performed using SEM (Zeiss Gemini 360), AFM (Bruker Dimension Icon), and Raman spectroscopy (Horiba LabRAM Odyssey).

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Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the Electronic Supplementary Material. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

L. B. and Y. C. conceived the idea and supervised the project. T. L., S. K. W., and Z. L. Y. designed the ALE-assisted, resist-contamination-free process, fabricated CNT TFTs, and performed electrical characterizations. Z. L. Y. and Z. L. L. optimized the ALD process. C. C. Z., K. L. C., and L. G. helped electrical characterizations. C. W., Y. H. H., and B. Y. H. deposited CNT network films and performed morphology and structural characterizations. T. L., S. K. W., Z. L. Y., L. B., and Y. C. analyzed data. L. M. P., Y. W., J. H. K., and X. L. L. contributed to data analysis and fruitful discussions. T. L. and Y. C. prepared the initially manuscript. All the authors have approved the final manuscript.

Use of AI statement

None.

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