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Review Article

A review on monolithic 3D integration: From bulk semiconductors to low-dimensional materials

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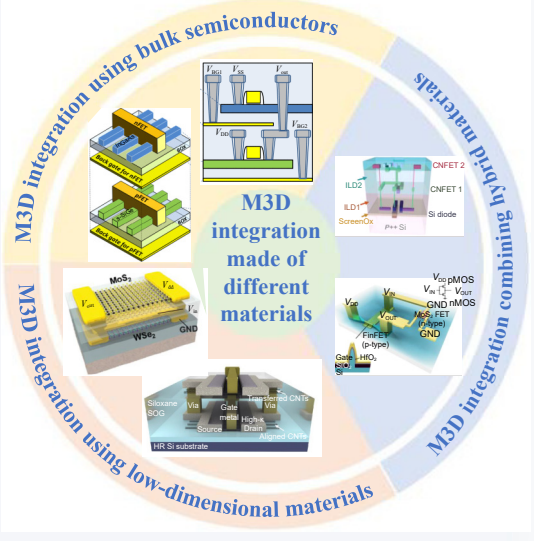
ABSTRACT: Monolithic three-dimensional (M3D) integration represents a transformative approach in semiconductor technology, enabling the vertical integration of diverse functionalities within a single chip. This review explores the evolution of M3D integration from traditional bulk semiconductors to low-dimensional materials like two-dimensioanl (2D) transition metal dichalcogenides (TMDCs) and carbon nanotubes (CNTs). Key applications include logic circuits, static random access memory (SRAM), resistive random access memory (RRAM), sensors, optoelectronics, and artificial intelligence (AI) processing. M3D integration enhances device performance by reducing footprint, improving power efficiency, and alleviating the von Neumann bottleneck. The integration of 2D materials in M3D structures demonstrates significant advancements in terms of scalability, energy efficiency, and functional diversity. Challenges in manufacturing and scaling are discussed, along with prospects for future research directions. Overall, the M3D integration with low-dimensional materials presents a promising pathway for the development of next-generation electronic devices and systems.



KEYWORDS: monolithic three-dimensional (M3D) integration, two-dimensional (2D) material, logic circuit, static random access memory (SRAM), resistive random access memory (RRAM), sensor, optoelectronics, artificial intelligence

1 Introduction

1.1 Development of transistor architecture in the vertical direction

1.1.1 *Innovations in transistor geometry*

The size of transistors has been continuously scaled down based on the principle of Performance, Power, Area, and Cost (PPAC). However, as size of transistors gradually shrinks down to the nanoscale, it brings up significant short-channel effects (SCEs). One notable issue is the increased tunnelling effect between source and drain, which weakens the gate's electrostatic control over the channel. Consequently, channel leakage current becomes a critical problem that cannot be ignored. This raises an important question: How can we improve transistor performance while increasing area efficiency?

To strengthen the gate's electrostatic control over the channel and effectively mitigate the SCEs, researchers have been exploring the use of vertical physical space to enhance this control for decades. In 1999, Professor Hu proposed the FinFET [1–3], a novel transistor geometry that transitioned transistor architecture from planar to three-dimensional (3D) forms. The introduction of FinFETs marked a significant milestone, paving the way for the development of low-dimensional silicon nanosheets and nanowires. Following this, the gate-all-around (GAA) transistor architecture [4–11] was proposed to further enhance the gate's electrostatic control over the channel at the nanoscale. GAA transistors, which utilize nanosheets and nanowires, extend the benefits of novel

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geometries to both in-plane and vertical carrier transport [4, 5, 10, 12]. This advancement helps maintain transistor performance within a small footprint, thereby addressing the challenges posed by continued scaling.

1.1.2 *Innovations in semiconductor materials*

As the thickness of conventional silicon-based bulk semiconductors is reduced to the nanometer scale, the influence of surface defects and dangling bonds becomes more serious, resulting in reduced carrier mobility [13]. At this stage, low-dimensional materials such as CNTs [14–16], graphene [17–19], and transition metal dichalcogenides (TMDCs) [20–22], have garnered widespread attention due to their excellent surface properties and electrical characteristics. For example, the 2D materials (2DMs) lack dangling bonds and are passivated, which minimizes scattering effects and prevents the decrease in mobility when decreasing the channel thickness. Consequently, transistors based on low-dimensional materials [23–36] are considered among the most promising candidates for next-generation high-density electronics.

The first CNT field-effect transistors (CNFETs) [37] were first demonstrated in 1998 and their characteristics have been improved continuously. Cao et al. [27, 31, 32] have been working on improving the performance of p-type CNFETs. For instance, they reported a single-walled-CNFET with a Mo end-bonded contact [31] scheme which was beneficial for minimizing contact resistance when scaling the contacts to 10 nm and beyond compared to other works, as depicted in Fig. 1(a). However, the high annealing temperature of 850 °C in this process is incompatible with the fabrication of channels below 60 nm. To solve this issue, they changed the end contacts to Co-Mo alloy contacts [32], where Co acted as a catalyst to reduce the reaction temperature to 600 °C. Therefore, they reported a high-performance p-type transistor with

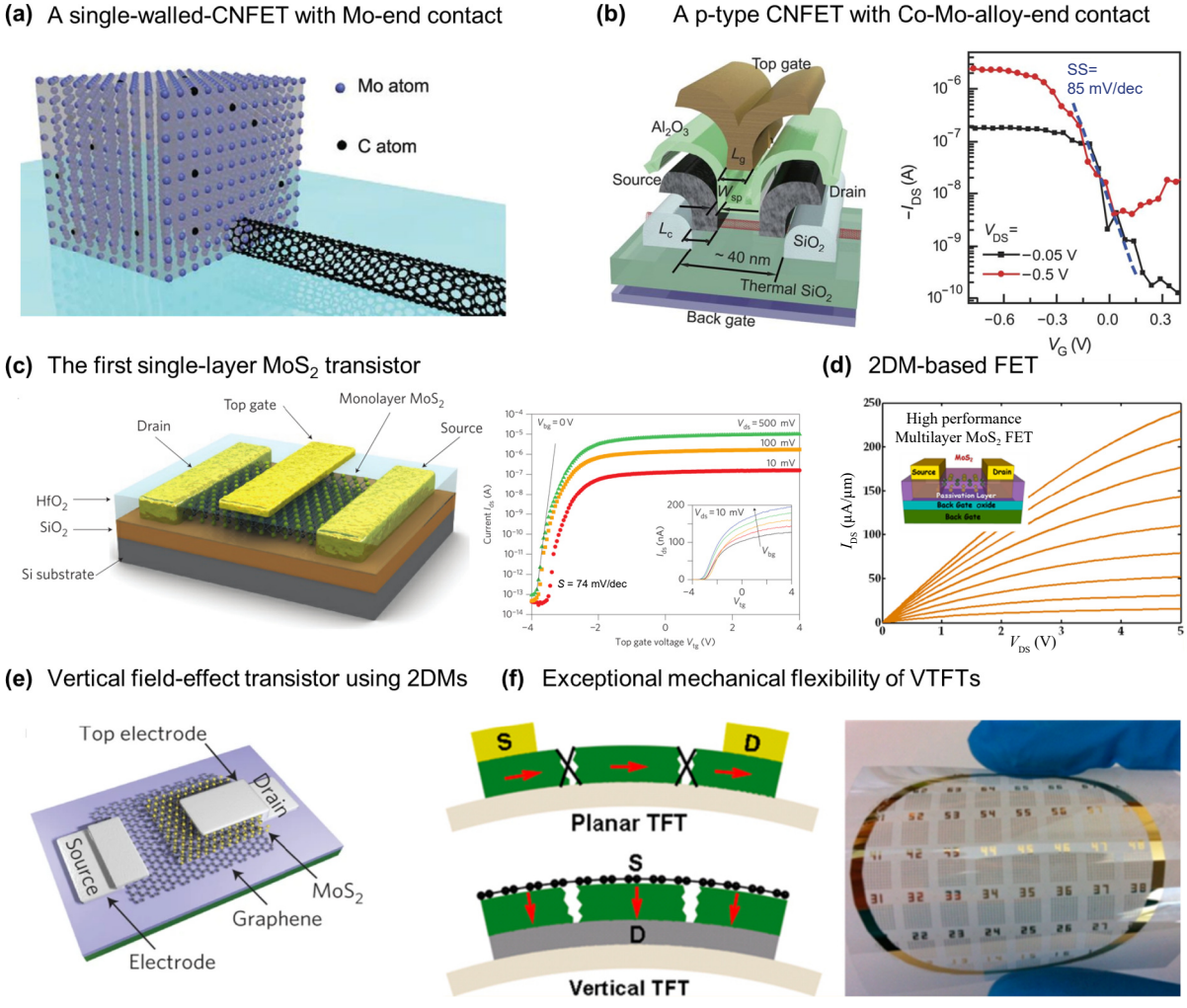

Figure 1 FETs based on low-dimensional materials. (a) Mo end-contacted single-walled-CNFET, in which the CNT is bonded to the Mo electrode via carbide connections. Reproduced with permission from Ref. [31], © The American Association for the Advancement of Science 2015. (b) Schematic of a transistor using a single-walled CNT as channel and its subthreshold curves. Reproduced with permission from Ref. [32], © The American Association for the Advancement of Science 2017. (c) Three-dimensional schematic view of MoS_2 monolayer transistors and its I_{ds}–V_{tg} curve recorded for a bias voltage ranging from 10 to 500 mV, showing low subthreshold swing of 74 mV/dec. Reproduced with permission from Ref. [24], © Springer Nature Limited 2011. (d) Output characteristics of a high-performance MoS_2 transistor demonstrating exceptionally high mobility. Reproduced with permission from Ref. [28], © American Chemical Society 2013. (e) Schematic illustration of the vertically stacked graphene-MoS_2-metal FETs, with the graphene and top metal thin-film functioning as the source and drain electrodes, and the MoS_2 layer as the vertically stacked semiconducting channel. Reproduced with permission from Ref. [26], © Springer Nature Limited 2012. (f) Schematics illustrating the operation of the planar TFT and VTFT on a flexible plastic substrate and photograph of a large array of VTFTs integrated on a bent flexible substrate, demonstrating good mechanical robustness of VTFTs. Reproduced with permission from Ref. [52], © American Chemical Society 2014.

a single-walled CNT as the channel (Fig. 1(b)), which occupies less than half the space of silicon-based technologies and shows a subthreshold swing of 85 mV per decade and good potential for low-voltage applications. In year 2011, 2D material, single-layer MoS_2 transistors [24] demonstrated room-temperature current on/off ratios of 10^8 and ultralow standby power dissipation (Fig. 1(c)). By using low work function metals like scandium contacts, Das et al. [28] realized multilayer MoS_2 transistors with high effective mobilities of 700 $cm^2/(V·s)$, as shown in Fig. 1(d). Moreover, 2D semiconductor materials have been shown to enable the vertical integration of their multi-heterostructures [25, 26, 38], suggesting their potential [39–41] in traditional GAA structures and facilitating the development of a new generation of vertical field-effect transistors (VFETs) [25, 26, 35, 42–51]. As depicted in Fig. 1(e), the channel of these VFETs, based on 2D semiconductors, is sandwiched between the source and the drain, with the channel length defined by the semiconductor thickness. This configuration allows for scaling down to the sub-5 nm range while maintaining exceptional electrical performance and reducing energy consumption. Unlike planar FETs, the channel current of VFETs is unaffected by planar cracks caused by external bending forces, as shown in Fig. 1(f). Therefore, these unique VFETs can enable ultrashort channel devices with very high current delivery and exceptional mechanical flexibility [52, 53] in addition to improving area efficiency.

1.2 The emergence of 3D integration

Although FinFET, GAAFET and VFET utilize the vertical physical space of a logic chip to improve device performance and enhance the electrostatic control of a single transistor, their impact on increasing circuit integration density is limited [54]. Instead of focusing solely on enhancing the performance of individual transistors, it is imperative to adopt an integrated approach. Therefore, 3D integration circuits [55–61], in which chips or device layers are stacked vertically, offering a practical solution to increasing device density and alleviating the limitations of the von Neumann architecture. This vertical stacking facilitates area scaling without shrinking essential device sizes and pitches, thereby maintaining device performance while circumventing the limitations associated with photolithography.

1.2.1 3D chips stacking based on through-silicon via

Through-silicon via (TSV) technology is crucial for enabling 3D integration. Over the past few decades, the technology has been extensively developed [55–57, 59–61]. TSVs (Figs. 2(a) and 2(b)) establish vertical connections between chips or wafers by filling vias with conductive materials like copper, tungsten or polysilicon, achieving vertical electrical interconnection [59]. Compared to chips utilizing a 2D architecture, TSVs significantly reduce the distance between circuits, enhancing interconnect density [56] and enabling high-bandwidth interconnection. High bandwidth memory (HBM) exemplifies this, with its stacked DRAM architecture using the TSV technology (Fig. 2(c)), which improves capacity, bandwidth, and power efficiency compared to conventional 2D DRAMs [60].

1.2.2 Monolithic 3D integration

Although the TSV technology has been commercialized, the size of its vias is larger compared to standard back-end-of-line (BEOL) vias in planar CMOS technology. This results in increased parasitic capacitance and stress in the wafer [53, 62], causing RC delay and heat dissipation. Moreover, reducing transmission latency and energy consumption through continuous shrinking of TSV sizes is challenging. To address these issues, researchers have introduced monolithic 3D (M3D) integration [53, 58, 59, 63–66], which involves the vertical stacking of device layers interconnected by dense nanoscale inter-layer vias (ILVs) instead of bonding fabricated dies using microscale TSVs. ILVs enable high-density parallel communication. In M3D integration [58], multiple stacked tiers are fabricated sequentially on the same wafer via deposition and etching [53] with each tier comprising an active layer, BEOL layer and interlayer dielectric (ILD) layer (Fig. 2(d)).

M3D integration has achieved a maximum density of 10^7 vias/mm^2, compared to 10^5 vias/mm^2 for TSV technology [67]. Furthermore, since devices and ILVs in M3D are fabricated sequentially, their alignment accuracy surpasses that of TSV technology, which requires bonding alignment [64, 68–70]. The M3D integration is thus considered a promising technology for continuing transistor integration as Moore's law sunsets, primarily due to its enhanced inter-tier connectivity, higher circuit density [53], and reduced parasitic capacitance [65].

In this review, we will focus on examples of M3D integration using various semiconductor materials. Section 2 will briefly discuss the M3D integration involving conventional bulk semiconductor materials. Section 3 will explore M3D integration using emerging low-dimensional semiconductor materials, which have gained prominence in recent research. Considering practical feasibility for commercial applications, Section 4 will examine the M3D integration of low-dimensional material transistors with silicon transistors. Finally, Section 5 will summarize the applications of M3D integration in different fields.

2 Monolithic 3D integration using bulk semiconductors

The development of M3D integration has taken various directions. Here, we discuss the progress in M3D integration across different semiconductor materials, including traditional semiconductors like Si and Ge, highlighting their advancements in GAA and complementary FET (CFET) structures. We also delve into the M3D integration of compound semiconductors such as the IGZO and Si. Additionally, we cover the vertical structures and integration of power devices in third-generation and fourth-generation semiconductors, like GaN and Ga_2O_3.

2.1 Monolithic 3D integration based on Si/Ge

Over a decade ago, demonstrations of 3D integration [73] were presented. Advancements in wafer-to-wafer bonding [74] and molecular bonding using low-temperature processes [75] led to the emergence of 3D sequential integration [75–77], a promising approach to fully exploiting the third dimension in semiconductor devices. Concurrently, with the development of FinFET [78–80] structures, the GAA [79–84] architecture was proposed and continuously refined to enhance gate control. To achieve smaller technology nodes and reduce the footprint of individual units, CFET structures [72, 80, 82, 84–86] have been introduced, encompassing a diverse range of materials. CFET represents the simplest form of 3D integration, wherein n-type and p-type transistors are vertically stacked and controlled using a common gate. This configuration allows for standard cells and SRAM cells

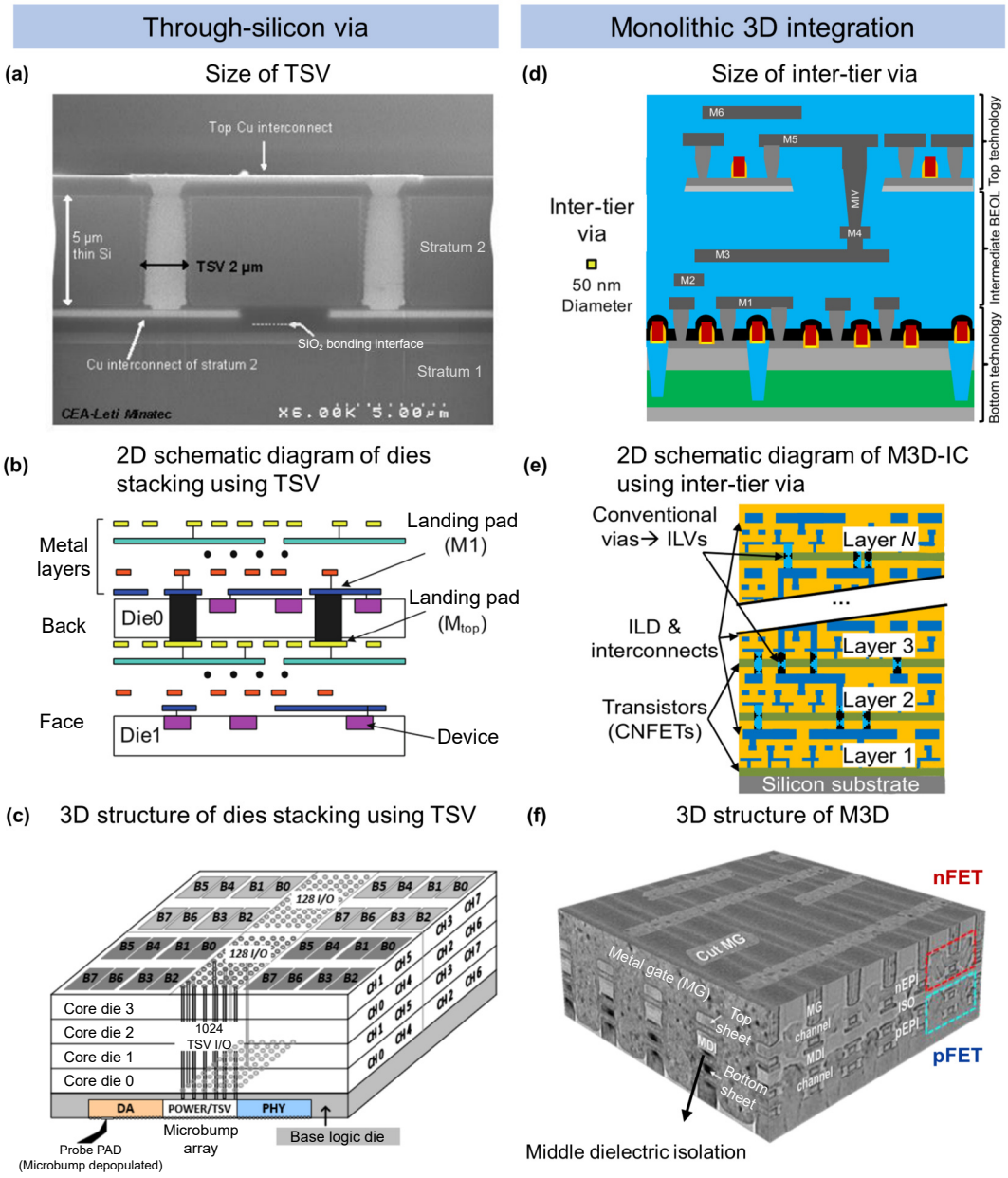

Figure 2 Schematic comparison of TSV and M3D. (a) SEM cross-section of a copper TSV chain and schematic of TSV size. Reproduced with permission from Ref. [57], © IEEE 2008. (b) 2D schematic diagram of dies stacking using TSV. Reproduced with permission from Ref. [58], © IEEE 2012. (c) 3D structure of dies stacking using TSV. Reproduced with permission from Ref. [60], © IEEE 2017. (d) Schematics of a generic 3D-monolithic integration and size of Inter-tier via. Reproduced with permission from Ref. [64], © IEEE 2018. (e) Schematic of the first monolithic 3D ICs use CNFETs. Reproduced with permission from Ref. [71], © IEEE 2013. (f) TEM demonstration of monolithic 3D integration. Reproduced with permission from Ref. [72], © IEEE 2023.

with a 25% smaller layout area, a 25% higher pin density, and twice the routing flexibility compared to FinFETs with the same overall active footprint [87], making it suitable for nodes smaller than N2 nm. By minimizing the space between n-type and p-type transistors, CFET structures can significantly reduce the standard unit area. Furthermore, to achieve higher mobility, different channel materials can be introduced into both transistors, providing strong flexibility in CFET construction.

The sequential integration of original CFET involves several stages. Initially, the process focuses on fabricating the underlying devices to establish a foundational layer. Following this, dielectric-to-dielectric wafer bonding technology is employed, facilitating the creation of a semiconductor layer that overlays the initial layer through wafer transfer. In the final stage, the emphasis shifts to the integration of top-layer devices and the establishment of electrical connections between the top and bottom gates. A key advantage of this approach lies in the ability to process both bottom and top devices using the same manufacturing methods as planar semiconductor devices. This flexibility allows sequential CFET integration to accommodate a wide range of channel materials, supporting variations for both n-type and p-type configurations. Despite advancements in power performance [88] optimization and the development of novel transistor-level 3D standard cell layouts [89] in original CFET, challenges such as power degradation and reliability issues persist in the implementation of sequential integration of CFET [90].

M3D integration emerges as a viable integration solution. The process for a single-chip CFET begins with the epitaxial growth of the bottom channel, followed by the deposition of an intermediate sacrificial layer, and concludes with the epitaxial growth of the top channel. In nanosheet channels, the initial configurations for both bottom and top channels can manifest as Si fins or Si/SiGe multilayer stacks. While a single-chip CFET is relatively cost-effective, the complexity significantly escalates when pursuing vertical integration.

Chang et al. [82] proposed the CMOS inverter and 6T-SRAM demonstration based on the GAA CFET structure (Fig. 3(a)). The low-temperature process (≤ 600 °C) employed in this approach is conducive to M3D integration and paves the way for future advancements. Compared to 2D COMS counterparts, the 3D inverters exhibit lower input parasitic capacitance, leading to reduced gate delay and lower power consumption. Moreover, a stack GAA CFET with three channels and an inverter device has been fabricated, showing the potential of future multi-layer stacking structures.

The two materials composing CFETs can be either identical or different, with numerous combinations proposed. Ge has been considered a replacement for Si as the channel material due to its superior hole transport properties. Rachmady et al. [79] demonstrated a short-channel Ge PMOS integrated with Si NMOS through sequential monolithic 3D stacking, which does not degrade the MOS device characteristics (Fig. 3(b)). Through layer transfer and 3D stacking technologies, high-density, low-power, high-performance CMOS devices were achieved without degradation in the bottom device during the fabrication process. This was accomplished through the meticulous design of the metal gate stack and contact. The 3D stacked heterogeneous Ge-Si CMOS inverter maintained drive performance in both Ge PMOS and Si NMOS.

A critical consideration in the monolithic integration process arises when the bottom-layer transistor is already fabricated. The subsequent processing steps for the top-layer structure must account for the impact of temperature on the bottom layer. To address this concern, significant efforts have been directed toward minimizing the processing temperature during integrated manufacturing. In the fabrication process of gallium arsenide (GaAs) transistors below 400 °C [81], techniques such as plasma-assisted atomic layer etching (PA-ALE), plasma immersion ion implantation (PIII), and far-infrared laser activation (FIR-LA) are employed. These methods facilitate the realization of 3D stackable GaAs transistors. Furthermore, the Ge pFET fabrication process offers a distinct advantage due to its lower temperature budget compared to Si. Abedin et al. [91] have proposed an optimized low-temperature process for germanium-on-insulator (GOI) substrate fabrication, achieving a thickness of less than 25 nm and a maximum temperature of 350 °C.

The advancement of large-scale manufacturing in CFET technology necessitates leveraging existing silicon-based manufacturing technologies. Subramanian et al. [86] proposed a pioneering monolithic integration of 3D CFET on 300mm wafers. The CFET architecture consists of top NMOS nanosheet FETs and bottom PMOS FinFETs (Fig. 3(c)). In this configuration, the NMOS and PMOS devices are stacked vertically and share a common gate. Monolithic integration offers several advantages over sequential integration, including reduced parasitic resistances and

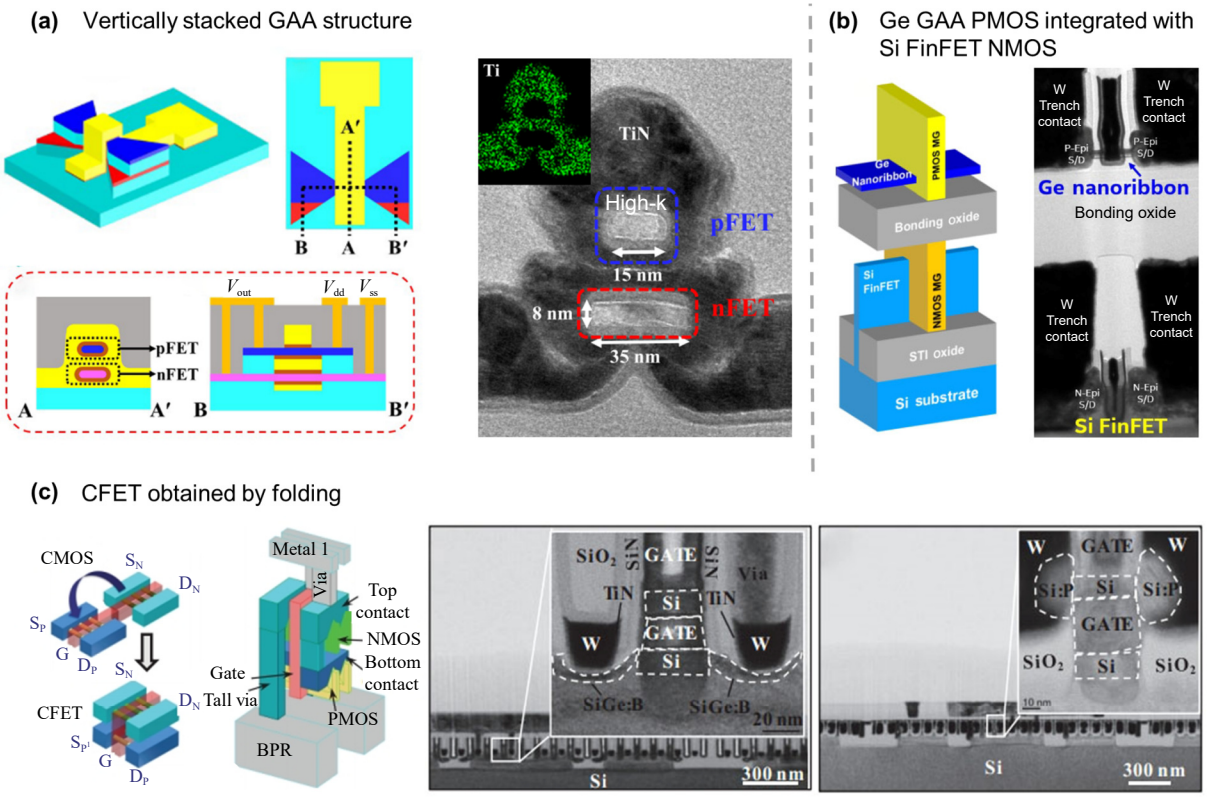

Figure 3 Si/Ge-based monolithic 3D integration. (a) Schematics of the CFET process and its TEM image of the vertically stacked GAA structure. Reproduced with permission from Ref. [82], © IEEE 2019. (b) Ge GAA PMOS in the upper layer and Si FinFET NMOS in the bottom layer and the cross-section view through sequential heterogeneous integration. Reproduced with permission from Ref. [79], © IEEE 2019. (c) Scheme of a CFET obtained by folding an NMOS on the top of a PMOS and the cross-section TEM images of two stacked transistors. Reproduced with permission from Ref. [86], © IEEE 2020.

capacitances. It is anticipated that the monolithic CFET integration scheme will achieve the requisite footprint scaling for future technology nodes, thus providing a viable pathway for the continued miniaturization of electronic devices.

2.2 Monolithic 3D integration based on other semiconductors

Compound semiconductors, particularly III-V materials, offer significant advantages over Si [92], including superior speeds due to higher electron mobility and diverse optical properties arising from unique bandgaps. Integrating Si and III-V materials on a single chip holds substantial promise for enhancing the functionality of microelectronic systems. In the context of monolithic 3D-IC integration, indium gallium zinc oxide (IGZO) emerges as a compelling channel material for thin film transistors (TFTs). IGZO can be deposited at room temperature, offering benefits, such as high electron mobility, improved sub-threshold slope, and minimal off-state leakage, all contributing to the overall efficacy of the integration process. However, a notable limitation of IGZO is its exclusive suitability for n-type transistors, necessitating an additional p-type transistor to achieve a complementary structure like CFET.

Significant efforts have been devoted to forming heterogeneous transistor structures incorporating IGZO [93–98]. Irisawa et al. [93] introduced a novel method integrating 3D stacked InGaAs-OI n-MOSFETs and SGOI p-MOSFETs through a sequential M3D integration process (Fig. 4(a)). This configuration aims to achieve dual-channel CMOS devices with enhanced electron and hole mobility. To further improve mobility and optimize power management, strategic utilization of wire channels and back gate control was implemented. However, independent gate voltage control for the two MOSFETs remains unexplored.

In recent years, the advent of the CFET structure has spurred considerable research into IGZO heterostructure transistors [95, 96] (Figs. 4(b) and 4(c)). Chang et al. [95] introduced vertically stacked inverters and a 6T-SRAM configuration, employing an innovative heterogeneous dual-work-function gate CFET design. This approach incorporates n-type IGZO and p-type polysilicon channels, utilizing a dual-work-function gate structure combined with tailored gate biasing to enable precise tuning of the channel potential to align with the threshold voltage. Moreover, extensive research continues to explore CFET structures based on various materials. It is anticipated that future developments in integrated circuits adopting CFET structures will yield significant performance optimizations and structural enhancements.

Vertical structures are extensively utilized in power devices to enhance their performance and adaptability to various applications. While power FETs commonly employ horizontal structures in low-power applications, such as small-power switches in integrated circuits, modern high-power FETs have increasingly transitioned to vertical structures. This shift allows FETs to improve high-power processing capabilities, enhance thermal stability, reduce on-resistance and operate at high voltages. The widespread adoption of third and fourth-generation semiconductors, such as gallium nitride (GaN) [99] and gallium oxide (Ga_2O_3) [100], has significantly advanced the functionality and efficiency of vertical structure power devices (Figs. 4(d) and 4(e)).

Additionally, the concept of vertical integration of vertical Schottky barrier transistors (v-SBTs) has been proposed, offering a potential architectural framework for vertical complementary logic circuits, as shown in Fig. 4(f). An innovative alternative to conventional vertical transistor structures has been introduced, showcasing distinct characteristics. Choi et al. [101] developed a novel method for modulating a Schottky barrier formed at a graphene-semiconductor heterojunction. This technique involves controlling the work function of graphene via a gate positioned laterally from the graphene-semiconductor junction, inducing a shift in the work function across the entire material (Fig. 4(g)).

3 Monolithic 3D integration using low-dimensional materials

High process temperature of upper-layer devices in M3D integration can potentially damage the pre-fabricated bottom-layer devices [102]. In other words, the bottom-layer devices should withstand the high-temperature processes of upper fabrication. Low-dimensional materials present a promising solution for M3D integration due to their compatibility with low-temperature layer transfer techniques [71, 103]. These techniques allow for decoupling high-temperature nanomaterial growth from low-temperature M3D integration [103, 104]. Additionally, the intrinsic thinness of low-dimensional materials results in exceptionally low stiffness and minimal internal stress, thereby overcoming the physical constraints posed by traditional bulk materials in M3D integration. Moreover, M3D integration based on low-dimensional materials can achieve an integration density improvement of over 150% [53] compared to conventional M3D integration using bulk materials. This significant enhancement offers a superior platform for realizing ultra-high-density M3D integrated circuits with minimal thickness.

3.1 Monolithic 3D integration based on CNTs

CNFETs have emerged as a promising candidate for future digital ICs due to their high performance and low power dissipation. However, integrating CNTs into ICs requires addressing the challenge of removing mispositioned and metallic CNTs (m-CNTs) while preserving semiconducting CNTs (s-CNTs). In conventional 2D digital systems, electrical breakdown is employed to deactivate m-CNTs. During this process, the wafer substrate serves as a back-gate to turn off the s-CNTs, thereby protecting them from damage. However, the control of the back-gate on the s-CNTs in the upper layers of M3D IC progressively weakens, leading to the undesirable electrical breakdown of the s-CNTs. To address this issue, Wei et al. [71] developed an innovative technique called 3D-VLSI m-CNT Removal, which employs local back-gates on each layer to turn off s-CNTs during the electrical breakdown of m-CNTs in an M3D IC. This advancement facilitates scalable M3D integration based on CNFETs, as illustrated in Fig. 2(e). Complementary CNFETs with high switching ratios were strategically placed on arbitrary layers of M3D ICs and interconnected using traditional platinum vias, enabling inter-layer and intra-layer logic operations. Importantly, as depicted in Fig. 5(a), the maximum process temperature during back-end-of-line for this technique was below 250 °C, significantly lower than the thermal budget limit of traditional processes (500 °C). Therefore, the performance of bottom layer devices will remain unaffected by excessive manufacturing temperatures, ensuring that the switching ratio of each layer exceeds 10^3, as shown in Fig. 5(b). This approach not only maintains the integrity of s-CNTs but also ensures the scalability and efficiency of M3D CNFET-based ICs, thereby advancing the development of high-density high-performance digital systems.

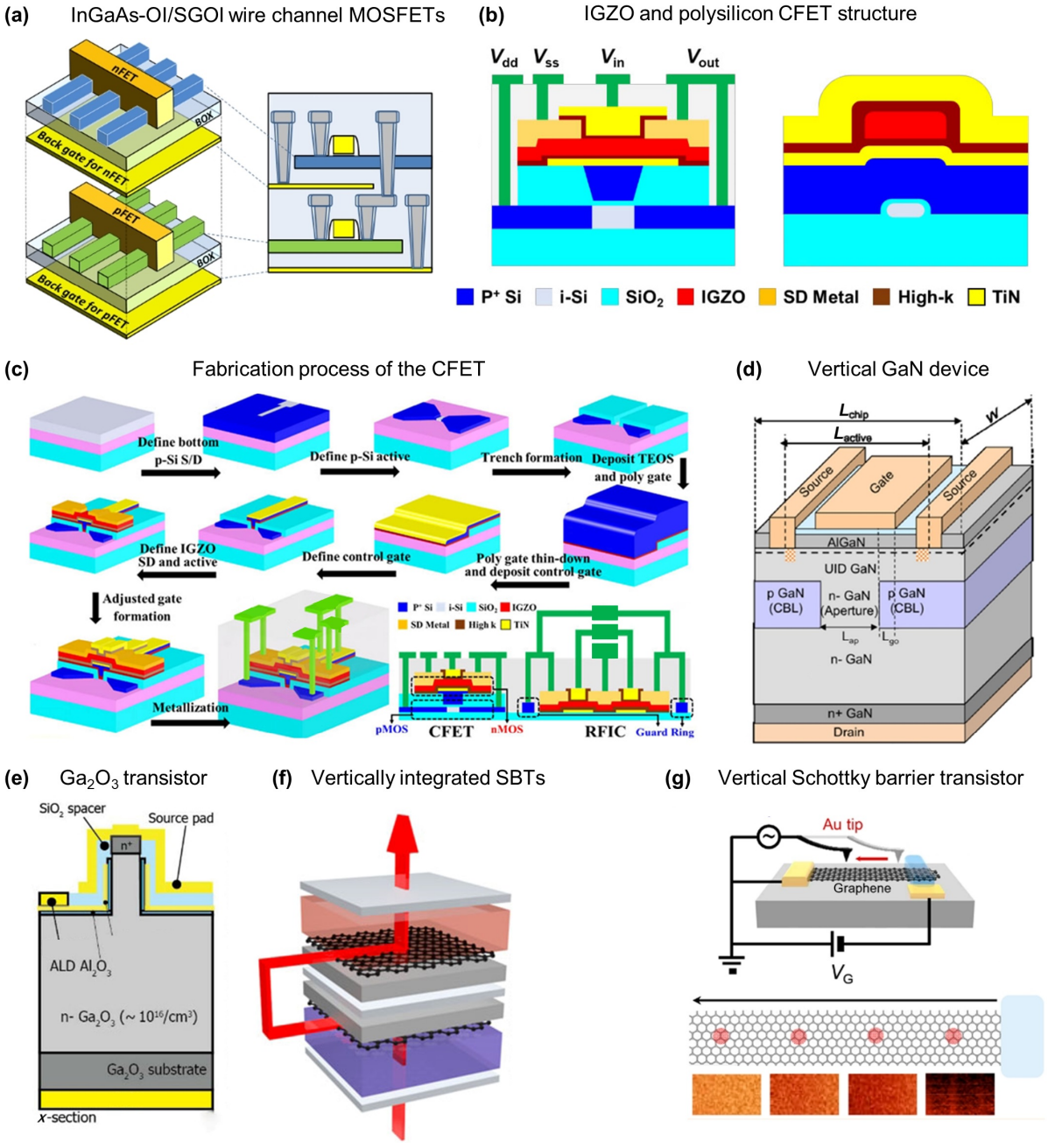

Figure 4 Schematics of IGZO compound semiconductor 3D integration and vertical structure of power transistor and heterojunction. (a) The scheme of the 3D stacked InGaAs-OI/SGOI wire channel MOSFETs with back gate control independently. Reproduced with permission from Ref. [93], © IEEE 2014. (b) The scheme of the IGZO transistor and polysilicon transistor with a trench gate and the dual-work-function-gate heterogeneous CFET structure. Reproduced with permission from Ref. [96], © IOP Publishing Ltd. 2022. (c) The fabrication process of the CFET inverters and 6T-SRAM with n-type IGZO and p-type polysilicon channels. Reproduced with permission from Ref. [95], © IEEE 2021. (d) Vertical cross-sectional view of a GaN device. Reproduced with permission from Ref. [99], © Wiley-VCH GmbH 2022. (e) Schematic representation of a vertical power transistor utilizing Ga_2O_3. Reproduced with permission from Ref. [100], © IEEE 2018. (f) A schematic description of the current path between vertically integrated Schottky barrier transistors (SBTs). (g) Vertical SBTs with remote gating, featuring a Schottky barrier formed at a graphene-semiconductor heterojunction. (f) and (g) are reproduced with permission from Ref. [101], © American Chemical Society 2019.

Single-walled CNTs (SWCNTs) are widely recognized as one of the most promising materials in flexible electronics due to their exceptional mechanical properties. However, they typically exhibit p-type behavior, which presents a challenge for the development of complementary CNT transistors. Zhao et al. [105] addressed this issue by using plasma-enhanced chemical vapor deposition (PECVD) to grow silicon nitride (Si_3N_4) as a dielectric passivation layer, promoting the formation of n-type SWCNTs. Subsequently, they fabricated p-type CNFETs on top of the Si_3N_4 layer to create CMOS circuitry, as shown in Fig. 5(c). Additionally, the same structure was fabricated on a polyimide substrate to produce high-performance M3D flexible circuits, which maintained excellent and stable electrical properties even after extensive bending tests, indicating their potential applications in flexible and wearable electronic ICs as shown in Fig. 5(d).

Despite these advancements, the upper-layer CNTs often lack

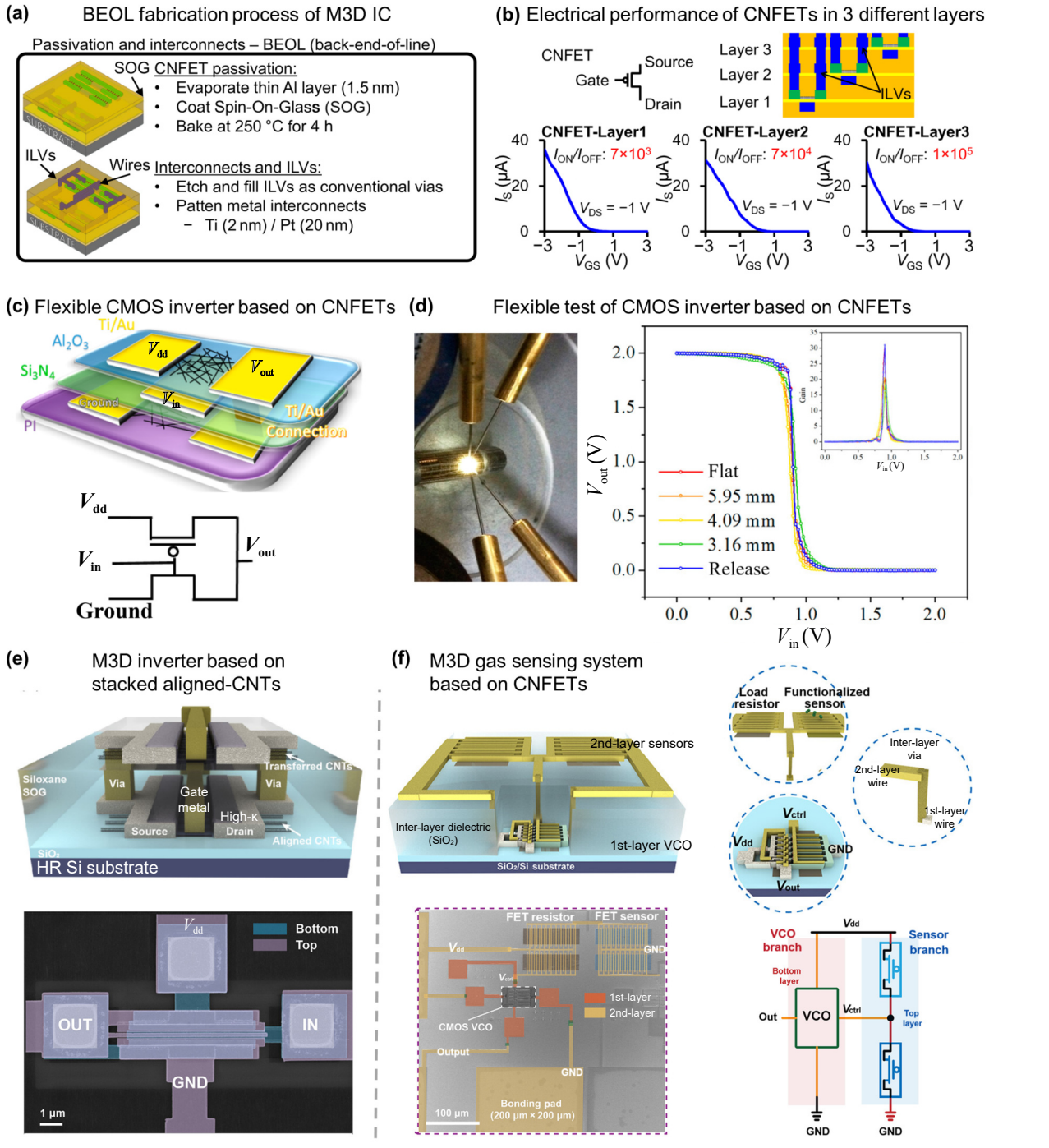

Figure 5 M3D integration based on CNTs. (a) BEOL fabrication process for fully-complementary CNFET monolithic 3D ICs. The maximum temperature is 250 °C. (b) Transfer characteristic curves of CNFETs in 3 different layers, each with an on/off ratio exceeding 10^3. (a) and (b) are reproduced with permission from Ref. [71], © IEEE 2013. (c) Schematic of 3D flexible CMOS inverter using CNFETs. (d) Photograph of flexible test with different bending radii and voltage transfer curve of 3D flexible CMOS inverter with various bending radii, working at V_{dd} of 2 V. (c) and (d) are reproduced with permission from Ref. [105], © American Chemical Society 2016. (e) 3D architecture and SEM image of M3D inverter based on stacked aligned-CNTs. Reproduced with permission from Ref. [107], © Fan, C. et al., InfoMat published by UESTC and John Wiley & Sons Australia Ltd. 2023. (f) Illustration and mechanism of the M3D gas sensing system based on CNFETs. Reproduced with permission from Ref. [108], © American Chemical Society 2023.

the necessary high quality due to their random orientation during preparation [106]. Furthermore, the use of atomic layer deposition (ALD) or PECVD [106] for high-k interlayer dielectrics (ILDs) introduces high interlayer parasitic capacitance and rough interfaces, rendering the reported M3D ICs based on CNFETs incapable of delivering the predicted high performance. In recent years, Fan et al. [107, 108] have focused on developing high-performance M3D integration based on CNTs (Fig. 5(e)). They employed spin-on-glass [107] processes with a maximum temperature of 220 °C to prepare interlayer SiO_2 with a low dielectric constant, contributing to low-parasitic ILD and an ideal surface. Additionally, their aligned CNTs were prepared using the

dimension-limited self-alignment method. This method leverages the hydrogen bonds between $C_4H_8O_2$ and poly[9-(1-octylonoyl)-9H-carbazole-2,7-diyl] (PCz) to confine CNTs with 3D random orientations at the 2D interface, subsequently, these CNTs self-assemble onto the wafer surface along the horizontal orientation due to the strong affinity between $C_4H_8O_2$ and SiO_2 as the wafer is pulled out [109]. These aligned CNTs, exhibiting a high mobility of 650 $cm^2/(V·s)$, were transferred onto the ILD layer through a clean, low-temperature process, ensuring that the bottom aligned CNFETs retained their pristine high performance after upper-layer fabrication. The high drive capability of their upper-layer CNFETs exceeds that of most advanced Si/Ge upper-layer transistors. Furthermore, Fan et al. proposed an M3D sensing system [108] as shown in Fig. 5(f). By evaluating the performance changes of the bottom-layer FETs before and after ILD packaging, they observed that the performance degradation did not exceed 20%, demonstrating the stability of their bottom-layer CNT CMOS for subsequent upper-layer fabrication.

3.2 Monolithic 3D integration based on 2D materials

As discussed in Section 1, 2D materials facilitate the vertical integration of multi-heterostructures due to their inherent immunity to stacking induced parasitic effects, which can significantly impact ultrathin silicon devices [53]. Additionally, 2D materials exhibit high in-plane thermal conductivity, [102] which is advantageous for reducing the overall thickness of M3D systems. This reduction in thickness effectively minimizes the overall dielectric thermal resistance and mitigates self-heating effects, thereby enhancing the thermal management and performance reliability of M3D integrated circuits.

Yu et al. [26] successfully demonstrated the vertical stacking of n-type and p-type 2D FETs, realizing a vertical structure based on exfoliated 2D materials (Fig. 6(a)). In this configuration, the $Bi_2Sr_2Co_2O_8$ (BSCO) layer functions as a p-channel while the MoS_2 layer serves as an n-channel, both controlled by a common silicon-based back-gate. The back-gate electrical field effectively penetrates through the bottom p-type device to modulate the top device, and thus enabling vertical stacking of 2D materials to achieve logic functions. However, this structure necessitates the gate electric field to permeate through the bottom device to control the upper layer, imposing strict requirements on the thickness of the bottom layer device and leading to disparities in control strength of the two layers. To address this asymmetry, Sachid et al. [110] implemented a shared gate structure in silicon-based CFETs, wherein NMOS and PMOS transistors share a common gate. This approach facilitated the sequential stacking of 2D MOSFETs (Fig. 6(b)). To further enhance the performance [111], forming gas annealing was used to eliminate organic residues from transferred WSe_2.

Beyond integrated solely with transistors, Wang et al. [112] demonstrated 3D monolithically integrated two-level stacked memory cells using monolayer MoS_2 transistors and few-layer hBN Resistive Random-Access Memory (RRAM). As shown in Fig. 6(c), to address topography issues, the second level 1T1R cells are horizontally offset by 1 mm from the first level 1T1R cells. ILDs were deposited at 150 °C using ALD, representing the maximum process temperature throughout the fabrication process. Both levels exhibit similar gradual set and reset switching with an operation voltage of less than 1.5 V, indicating no damage after the fabrication of the top layer. Additionally, Hu et al. [113] proposed an energy-efficient M3D SRAM cell featuring BEOL back-gated MoS_2 FETs and conducted a comprehensive analysis on the impact of interconnect resistance caused by layouts and wire routing. The analysis underscored the viability of M3D integration for creating high-density low-power memory.

As we know, conventional von Neumann computing systems consist of separate central processing units (CPU) and memory units. This separation leads in significant transmission latency and increased power consumption due to the large volumes of data exchanged between these units [115]. With the rapid advancement in big data analytics and deep learning, the demand for high-speed data transmission and low-latency memory access has grown substantially. One of the most effective solutions to address these challenges is to shorten the transmission path between CPU and memory units. 2D material-based M3D integration presents a promising opportunity to vertically stack memory units on top of logic units within the same chip, thereby enabling alleviating the von Neumann bottleneck. Tang et al. [114] achieved vertically stacked multilayers of high-performance all-exfoliated-2D FETs. Specifically, using a repeated layer-by-layer stacking process, they realized the vertical integration of multilayered devices with distinct functions, including memory, logics and sensors, as depicted in Fig. 6(d). Each layer is interconnected through ILVs, demonstrating cooperative functionality between the top optical sensor and bottom memory devices.

To meet the demands of large-scale production, many groups have focused on developing 3D device architecture using CVD-grown 2D materials [116–121]. For instance, Xiong et al. [116, 118] from Peking University demonstrated MoS_2/WSe_2 CFETs (Fig. 6(e)) based on large-scale CVD-grown 2D materials. Considering the mismatch in threshold voltages between n-type MoS_2 FETs and p-type WSe_2 FETs, which can degrade inverter performance, they employed chemical doping to align the threshold voltages. Additionally, the upper WSe_2 FET can lead to performance degradation after integration [122]. To mitigate this, they conducted low-temperature post-metal annealing at 200 °C under an argon atmosphere on the p-type WSe_2 transistor with a top-gate structure to improve the interface state and optimize electrical performance [118], achieving a record-high I_{on} and g_m with a short channel length compared to previous studies (Fig. 6(f)). The performance of these CFETs can still be optimized by adjusting device parameters and refining the fabrication process [123]. In addition to p-type WSe_2 FETs, by virtue of its ability to be doped by oxygen and water molecules in the air, $MoTe_2$ [117, 121] can be p-type doped with higher hole density. Therefore, Jia et al. [121] firstly realized high-performance M3D inverter array based on CVD-grown n-MoS_2 and p-$MoTe_2$. Recently, Liu et al. [119] reported high-performance M3D complementary inverters. They used SiO_2 as a buffer layer during the ALD of HfO_2, which can protect MoS_2 from damage during the ALD process and ensure a conformal, pinhole-free deposition of HfO_2.

Most earlier studies focused on the vertical stacking of planar transistors, but the vertical stacking of 2D VFETs has not yet been realized. In planar 2D transistors, current transmission between the source and drain occurs in-plane, implying that the channel length is still constrained by the photolithography limitations. Addressing this limitation, Xiao et al. [124] pioneered the vertically stacking of multiple VFETs using a van der Waals (vdW) lamination process and employed a hybrid drain to overcome the size constraints of VFETs in the vertical direction, thereby advancing the development of high-density integration, as illustrated in Fig. 6(g). In this

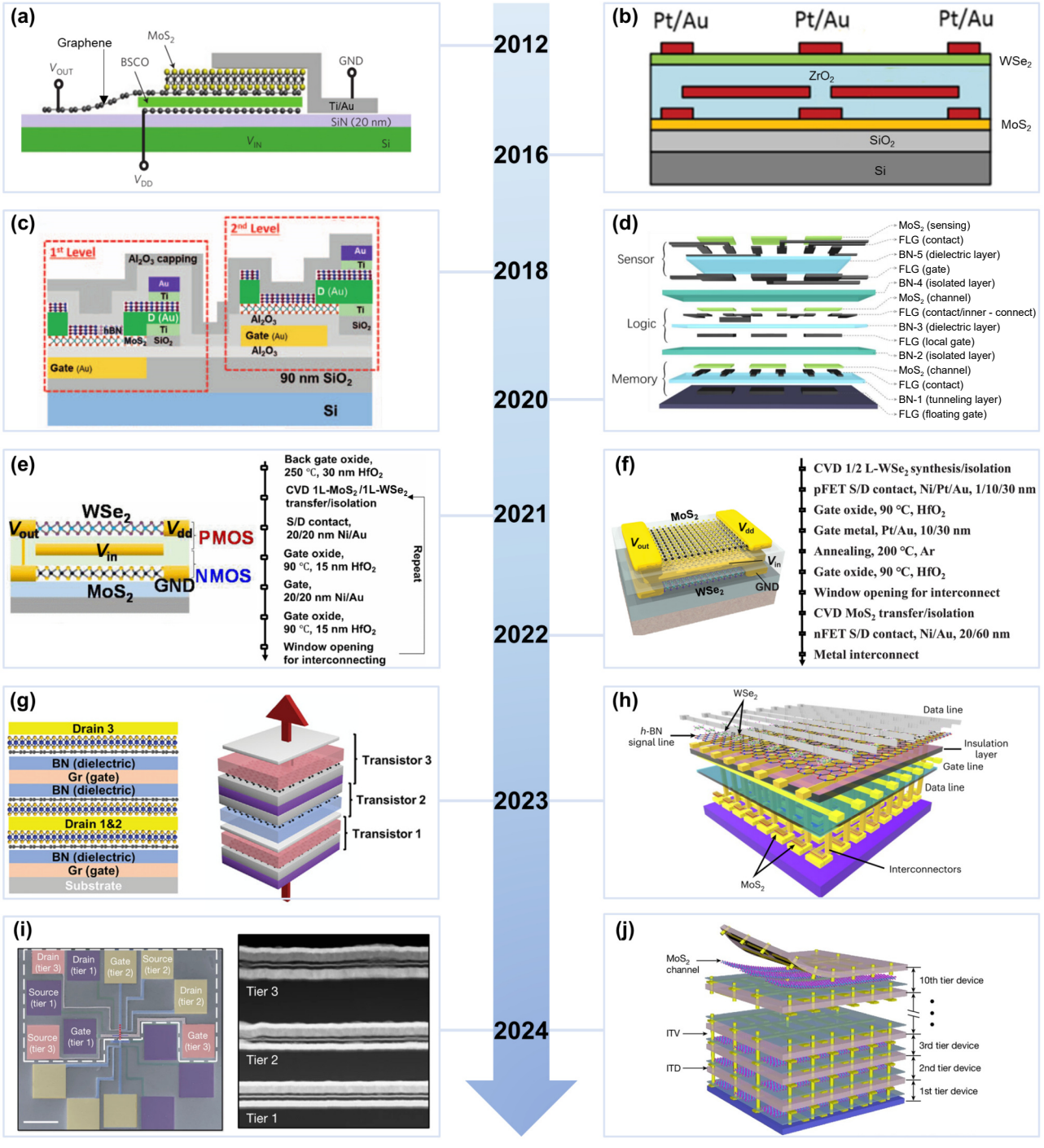

Figure 6 The development history of M3D integration based on 2DMs. (a) The first reported multi-heterostructures of complementary inverters using vertical stacking of layered materials. Reproduced with permission from Ref. [26], © Springer Nature Limited 2012. (b) Device cross-sectional view of shared gate CMOS M3D architecture. Reproduced with permission from Ref. [110], © WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim 2016. (c) The cross-section schematic of two-level stacked 1T1R cells. Reproduced with permission from Ref. [112], © IEEE 2018. (d) Schematic of vertically integrated electronic system with memory, logic and sensor layers. Reproduced with permission from Ref. [114], © Tang, J. et al., published by Wiley-VCH GmbH 2020. (e) Structure of the MoS_2/WSe_2 CFET and its process flow. Reproduced with permission from Ref. [116], © IEEE 2021. (f) The optimized structure of MoS_2/WSe_2 CFET and its optimized process flow. Reproduced with permission from Ref. [118], © IEEE 2022. (g) Cross-sectional and perspective schematics of three vertically integrated GVFETs. Reproduced with permission from Ref. [124], © Xiao, Z. et al., Advanced Science published by Wiley-VCH GmbH 2023. (h) Schematic of one of six stacked device layers, which is a M3D-integrated AI processor comprising memristors and MoS_2 transistors. The drain electrode line of the transistors is connected to the bottom electrode of the memristors. Reproduced with permission from Ref. [125], © Kang, J. et al., under exclusive license to Springer Nature Limited 2023. (i) Top view of SEM image and TEM image of the three-tier 3D integration of 2D FETs. Reproduced with permission from Ref. [126], © Jayachandran, D. et al., under exclusive license to Springer Nature Limited 2024. (j) Schematic of a 10-tier M3D system integrated by van der Waals lamination. Each part of this system is prefabricated on a sacrificial wafer including inter-tier dielectric. Reproduced with permission from Ref. [127], © Lu, D. et al., under exclusive license to Springer Nature Limited 2024.

configuration, the middle VFET shares both the drain and the gate with adjacent VFETs, further reducing vertical spacing. Their three-layer stacked VFETs achieved a total vertical height of 59 nm, equating to a mere 20 nm vertical distance between individual transistors, which is significantly smaller than the lateral spacing between transistors in 2D circuits. However, it is important to note that there is no electrical interconnection between VFETs in different layers, only an isolation layer facilitates stacking. Thus, methods for achieving interconnection between VFETs require further exploration.

In recent years, the M3D solution based on 2D materials has developed rapidly and achieved fruitful results. In 2023, Kang et al. [125] reported an 2D material-based M3D integration comprising up to six multifunctional layers (Fig. 6(h)). The role of WSe_2 is to enhance the electrical performance of memristors. After fabricating the transistor array on an ultrathin flexible polyimide substrate, an Al_2O_3 layer was deposited as ILD using ALD. Subsequently, a via hole was etched on the source region of the bottom MoS_2 transistor array, followed by the construction of a memristor array on top using a transfer method. Given that the properties of neuromorphic memristors are greatly influenced by the interface—where even minor contaminants can affect the ion migration responsible for resistance switching—A semi-dry transfer method was used to maintain interface cleanliness. Simultaneously, Jayachandran et al. [126] also achieved an all-2D-based monolithic 3D integration with three-tier on a large scale (Fig. 6(i)), demonstrating wafer-scale M3D integration of 2D FETs based on two different materials (n-type MoS_2 and p-type WSe_2), with more than 500 FETs in each tier. However, in the studies discussed above, all ILD and ILVs were directly fabricated on top of existing device layers using ALD and electron beam evaporation, which will result in strong Fermi level pinning effect. On the contrary, Lu et al. [127] prefabricated all components including ILD and vertical ILVs on a sacrificial wafer. And then, all components were mechanically released from the sacrificial wafer and vdW laminated tier-by-tier, realizing M3D integration with 10 circuit tiers, as depicted in Fig. 6(j). This approach can be attributed to the use of cross-linked polyvinyl alcohol (CPVA) as ILD, which exhibits low adhesion force with the substrate and is flexible enough to avoid damages during the mechanical peeling.

4 Monolithic 3D integration combining hybrid materials

Although ICs composed entirely of low-dimensional materials possess tremendous potential for next-generation high-density electronics, their commercial production is currently impractical due to the exorbitant costs associated with establishing dedicated production lines for these materials. Consequently, there is a growing interest in combining low-dimensional materials with conventional semiconductor materials. This approach leverages existing silicon-based technologies to reduce costs while capitalizing on the unique advantages offered by low-dimensional materials. One significant challenge in silicon-based technologies is achieving performance parity between p-type and n-type FETs due to the intrinsic mobility mismatch between electrons and holes. However, the electron mobility of certain 2D materials closely matches the hole mobility in silicon, potentially resolving the mobility mismatch issue inherent in all-silicon systems. The M3D integration discussed earlier typically involves the use of silicon wafers, but it is crucial to note that in these contexts, the silicon wafer primarily serves as a substrate [128]. In these instances, low-dimensional materials are not fully integrated with silicon devices or CMOS processes. Therefore, we will now comprehensively explore M3D integration that involves the amalgamation of low-dimensional semiconductor materials with conventional semiconductor materials, focusing on achieving synergistic enhancements in electronic performance and manufacturability.

4.1 Monolithic 3D integration of CNTs transistors with silicon transistors

In 2006, Ahn et al. [129] realized the vertical stacking of Si MOSFETs and SWCNT transistors. However, they did not demonstrate electrical interconnections between the different layers. Over the past decades, Shulaker et al. [71, 130–133] have conducted significant studies on the integration of CNFETs. In 2014, they reported the first VLSI-compatible M3D integration, utilizing low-temperature fabrication of CNFETs with silicon CMOS [130]. Their method involved transferring CNTs onto a wafer-scale silicon CMOS substrate at 125 °C, thereby avoiding degradation of the bottom silicon CMOS devices. At the circuit level, they integrated CNFET-based inverters with silicon-based inverters to create hybrid CNFET–silicon CMOS circuits, as depicted in Fig. 7(a). In addition to logic circuits, Shulaker and colleagues further demonstrated M3D integration of logic and memory components in arbitrary stacking orders using CNFETs, RRAM, and silicon FETs [131]. Similar to low-dimensional materials, the low-temperature processing of RRAMs enables their feasibility for stacking on top of the bottom logic layer, contributing to high-capacity storage. They successfully achieved the stacking of multiple layers, including CNFET layers and RRAM layers, on a starting silicon-FET substrate. The corresponding process flow is shown in Fig. 7(b), illustrating a total of four different functional layers, with silicon FETs used as access transistors for the upper RRAMs. This integration demonstrates the potential for advanced, multi-functional 3D IC architectures that leverage the unique properties of both conventional and low-dimensional materials.

Following this advancement, this four-layer structural unit was further expanded into an array and applied to actual chips [132]. As shown in Fig. 7(c), the processing and data storage layers were stacked sequentially on top of silicon logic circuitry on a single chip, with each layer containing millions of memory cells or transistor cells. This approach breaks the limitations of the von Neumann architecture and demonstrates compatibility with existing silicon-based technology infrastructure. This nanosystem not only processes massive amounts of captured data but also stores the processed information directly on-chip. For demonstration purposes, the researchers designed the fourth CNFET-inverter layer as simple chemical vapor sensors. The fine-grained connectivity provided by M3D integration allowed each sensor to interconnect with its underlying memory cell. They successfully demonstrated that the system can sense and classify different ambient gases. More excitingly, the fourth layer could be substituted with alternative processing or storage systems to enable more powerful chips for data-intensive applications. Similar to the von Neumann architecture, the traditional imaging system experiences high transmission latency due to long transmission paths between components. To address this issue, Shulaker et al. [133] demonstrated an M3D imaging system by vertically stacking CNT

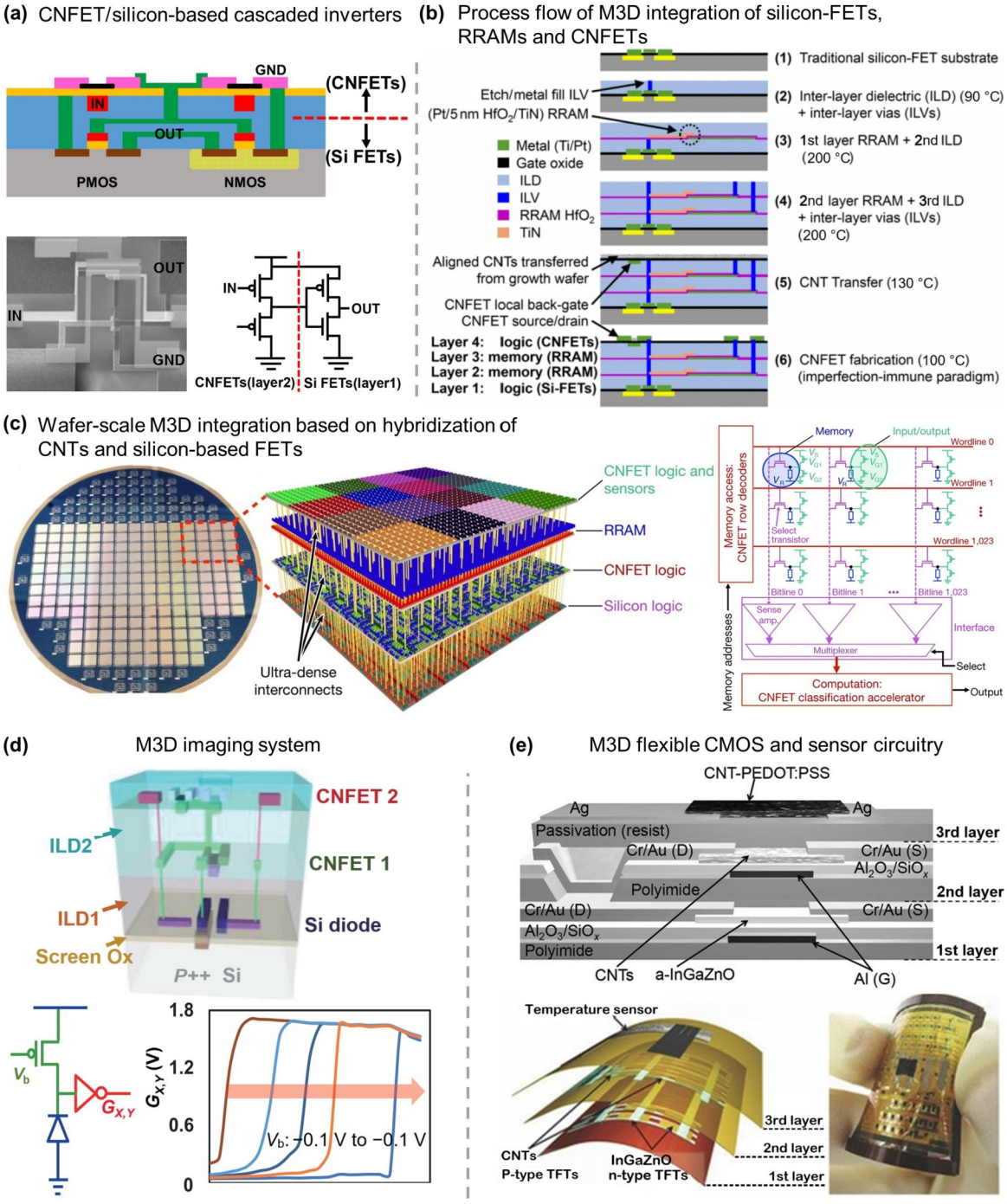

Figure 7 Demonstration of M3D integration using CNFETs and conventional-semiconductor-based FETs. (a) Schematic of M3D CNFET/silicon-based cascaded inverters, and below are the SEM image and circuit schematic. Reproduced with permission from Ref. [130], © IEEE 2014. (b) Process flow of M3D integration of silicon-FETs, RRAMs and CNFETs. All post-silicon fabrication processing is below 200 °C. Reproduced with permission from Ref. [131], © IEEE 2014. (c) Photograph of a 100-mm-wide wafer showcasing the fabrication of integrated circuits and corresponding zoom-in illustration of nano-system. On the right, a circuit-level schematic of the system is presented. Reproduced with permission from Ref. [132], © Macmillan Publishers Limited, part of Springer Nature 2017. All rights reserved. (d) 3D model of M3D imaging system and corresponding circuit diagram. Reproduced with permission from Ref. [133], © VLSI Symposium 2019. All Rights Reserved. (e) Schematic of M3D flexible CMOS and sensor circuitry. Reproduced with permission from Ref. [134], © WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim 2015.

computing circuitry directly over a conventional silicon imager substrate. This system eliminated the need for sequentially reading pixel array data from memory before processing. All silicon pixel data from layer 1 is read in parallel through ILVs to layer 2, where the CNFETs convert the pixel current into voltage. Subsequently, all pixel voltages are transmitted in parallel to layer 3 via ILV, and the CNFET inverter converts them into a digital voltage for output, as shown in Fig. 7(d). This innovative approach significantly reduces transmission latency and enhances the efficiency of data processing and storage, paving the way for more advanced and efficient electronic systems.

In addition to integrating with silicon FETs, Honda et al. [134]

realized an M3D CMOS with p-type CNT transistors stacked on n-type InGaZnO transistors. Specifically, they constructed a vertical 3D CMOS circuitry comprising a temperature sensor device and three active layers on a flexible substrate, as illustrated in Fig. 7(e). Notably, the top temperature sensor and interconnections were fabricated using printing methods, addressing the challenge in achieving high integration in flexible devices. The inverter, formed by connecting the two layers of transistors below, exhibited a gain of up to 45 at 5 V. Additionally, after conducting bending cycle tests on the 3D inverter, the researchers observed that its electrical performance remained intact. This observation underscores the excellent mechanical flexibility of the device, indicating its potential for the next generation of wearable health monitoring devices.

4.2 Monolithic 3D integration of 2DM transistors with silicon transistors

As mentioned previously, CNTs computing circuitry can be directly stacked over a conventional silicon imager substrate using ILVs, facilitating the parallel processing of pixel data. Similarly, 2DMs phototransistor arrays can be integrated onto silicon-based integrated circuits via ILVs [135, 136] as depicted in Fig. 8(a). Following the completion of the TMDCs transfer process, oxides were deposited onto the TMDCs using an ALD process with low processing temperatures, ensuring a low thermal budget for the upper-layer manufacturing process. Similarly, Zhu et al. [137] transferred a multilayer hBN onto silicon microchips without high temperature process, creating 2D-CMOS hybrid microchips for memristive applications. However, transfer of 2DMs [138] introduces a variety of organic polymers and cracks which will result in residual contamination and degradation of performance. Therefore, researchers tried to develop a variety of relatively low-temperature CVD methods to directly grow TMDCs on the underlying device layer [139–141]. The monolayer TMDCs prepared via CVD not only enable large-scale production but also hold promise for applications in portable flexible electronics. For instance, in 2020, Su et al. [139] reported the first instance of M3D integration involving heterotransistors comprising a MoS_2 nFET and a Si pFET (Fig. 8(b)), with MoS_2-based RRAM directly fabricated on the drain of the Si FET to form an embedded structure by a cold-wall CVD. Beyond that, Zhu et al. [141] ingeniously designed a metal-organic CVD method, which can

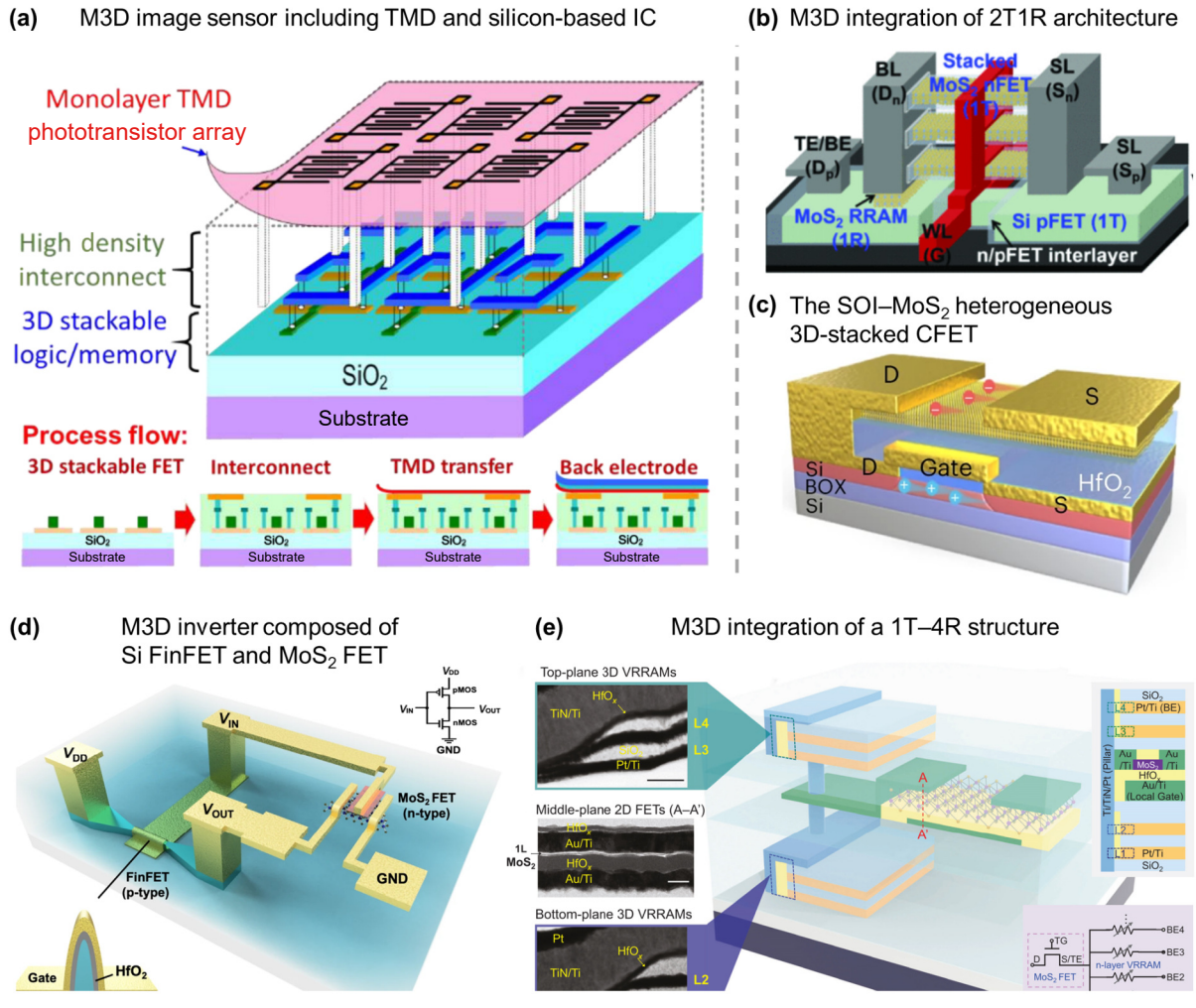

Figure 8 Demonstration of M3D integration using 2DFETs and silicon FETs. (a) Schematic of an M3D image sensor including TMD phototransistor array and 3D+ Si NWFETs-based IC. Reproduced with permission from Ref. [135], © IEEE 2016. (b) M3D 2T1R architecture composed of a MoS_2 nFET and a Si pFET featuring an embedded MoS_2 RRAM. Reproduced with permission from Ref. [139], © IEEE 2020. (c) Schematic of the SOI–MoS_2 heterogeneous 3D-stacked CFET. Reproduced with permission from Ref. [142], © Tong, L. et al., under exclusive license to Springer Nature Limited 2022. (d) Schematic of a CMOS inverter fabricated by vertically integrating a p-channel Si FinFET and an n-channel monolayer MoS_2 transistor. Reproduced with permission from Ref. [138], © Guan, S. et al. 2023. (e) M3D integration of a 1T–4R structure composed of 2D MoS_2 transistors and 3D VRRAMs. Reproduced with permission from Ref. [143], © Xie, M. et al. 2023.

segregate the low-temperature growth region from the high-temperature region. This innovation enabled the direct deposition of MoS_2 at a low growth temperature of 275 °C on top of the silicon CMOS wafer. And they also demonstrated that the performance loss of the underlying silicon circuits is negligible.

In light of the comparable electron mobility in MoS_2 to the hole mobility in silicon, Tong et al. [142] introduced heterogeneous CFETs (Fig. 8(c)) consisting of p-type FETs fabricated using SOI technology and large-size wafer-level MoS_2 n-type FETs, effectively addressing the mobility mismatch inherent in conventional all-silicon systems. Additionally, their SOI-MoS_2 CFET exhibited a voltage gain of 1.2 even at a supply voltage of 0.1 V, showing its potential for low-voltage and low-power applications. Similarly, Guan et al. [138] also fabricated an M3D complementary inverter, in which the bottom silicon transistor featured a FinFET structure, while the top MoS_2 FET utilized a top-gate structure, as shown in Fig. 8(d). To safeguard the MoS_2 layer from damage, the top-gate dielectric was fabricated via e-beam vapor deposition instead of ALD. Additionally, they leveraged mature industrial technologies such as chemical mechanical planarization and electron beam evaporation, affirming their compatibility with existing silicon-based 3D integration technologies.

Xie et al. [143] recently presented M3D integration of MoS_2 FET and HfO_2-based vertical RRAMs, forming a 1T4R structure beneficial for high-density memory (Fig. 8(e)). Notably, monolayer-MoS_2 FET was selected to drive multiple switching cycles of all vertical RRAMs. To minimize delay discrepancies in control across the four vertical RRAMs by the 2D FET, the 2D FET was positioned in the middle layer, with four vertical RRAMs distributed on the upper and lower sides. The maximum temperature during fabrication was set by the temperature used for growing the isolation oxide layer through PECVD, specifically at 300 °C. Moreover, owing to the low fabrication temperature of the upper layer, this process holds potential for expansion into 1TnR structures.

5 Applications of monolithic 3D integration

Applications of M3D integration encompass a wide range of fields, including logic circuits, memory, analog systems, sensors, and other related domains [144], presenting novel opportunities for the advancement of future chip technology.

As 2D material transistors progress towards incorporation in 3D architectures, fundamental circuit elements such as inverters, SRAM and RRAM exhibit continual improvements. The unique attributes of the 3D structure impart numerous benefits to the corresponding logic circuit units. Vertical stacking within 3D structures notably minimizes the device footprint, resulting in enhancements in both power consumption and overall performance. The M3D approach utilizing 2D material transistors offers a viable pathway for the evolution of future logic circuits and the realization of next-generation chips. This section will provide an in-depth analysis of the implementation and applications of M3D-based logic circuit units, as well as other systems utilizing low-dimensional materials across various domains.

5.1 Logic circuit units

5.1.1 Inverters and other logic devices

An inverter, whose function is to reverse the phase of the input signal by 180 degrees. As the most fundamental unit in logic circuits, the inverter is critical to realization of the new technological node or structure. With the continuous advancement of silicon-based semiconductor circuits, inverters have shown progressive reduction in gate length [75, 76] and have been fabricated using different materials [26, 71, 83, 95, 116, 139, 142] and integrated in various ways like sequential 3D integration [93] and monolithic 3D integration [82, 94, 96, 110, 118, 145, 146]. As integrated technology continues to advance, circuit components are required to shrink further, similar to the challenges faced by planar integrated circuits, which have reached their physical size limits. To maintain high performance in compact chips, device architectures evolve towards 3D configurations, incorporating 2D material transistors.

Inverters constructed through the integration of 2D material transistors demonstrate remarkable performance at extremely low operating voltages. The M3D integration of MOSFET utilizing 2D materials such as MoS_2 and WSe_2 [110] has achieved a power consumption of CMOS devices are approximately 4.2 and 0.11 nW, respectively, at a supply voltage (V_{DD}) of 1 V. The stacked structure mentioned in Fig. 6(e) [116] was meticulously constructed layer by layer and achieved sub-1 nm channel thickness and I_{on} > 400 μA/μm per channel footprint at V_d of 1 V. The utilization of vertically stacked MoS_2/WSe_2 CFET inverters in the study demonstrated a significant reduction in footprint, highlighting the potential of M3D integration with 2D materials for high-density, ultra-low voltage, and low-power applications. The M3D integration of 2D materials transistors not only paves the way for integrating 2D material channels in 3D architecture but also opens up new opportunities for electronic devices. Beyond that, MoS_2 and Si CMOS are vertically stacked to create a heterogeneous CMOS [139, 142]. The CMOS inverter is constructed within the framework of a Si FET, combining a p-type FET fabricated using SOI technology and an n-type FET constructed with 2D MoS_2.

Apart from the application in inverters, low-dimensional materials have demonstrated significant advancements in the construction of analog circuits, including amplifiers, signal mixers, and ring oscillators (ROs) [110]. These circuits not only exhibit exceptional integration capabilities but are also highly suited for low-voltage and low-power applications. Notably, ROs, which are typically composed of a series of inverters connected in a loop, have achieved reduced delay and higher frequency ranges through the use of 3D structures, particularly when CNTs are employed as the channel material in CNFETs.

Xie et al. demonstrated the fabrication of a 3D five-stage RO circuit with an oscillation frequency of up to 680 MHz and a stage delay of 0.15 ns [106] (Fig. 9(c)). Another team utilized high-performance aligned carbon nanotube (A-CNT) transistors and obtained ROs with oscillation frequency ranging from 2.58 to 5.78 GHz and gate propagation delay of 17 ps, representing the highest speed of 3D CNT integrated circuits [107] (Fig. 9(d)).

5.1.2 SRAM

SRAM is a type of memory with a static access function that can store data inside without the need for a refresh circuit. It is integral to high-performance and rapid-response digital systems, providing swift and reliable data storage and retrieval. SRAM cells typically occupy a significant portion of the chip area, underscoring their critical role in these systems.

In silicon-based logic circuits [75, 149], SRAM has evolved from a planar structure to vertical stacking structure [94] (Fig. 9(e)), TFT [150–152] and beyond. Various configurations, such as integrating

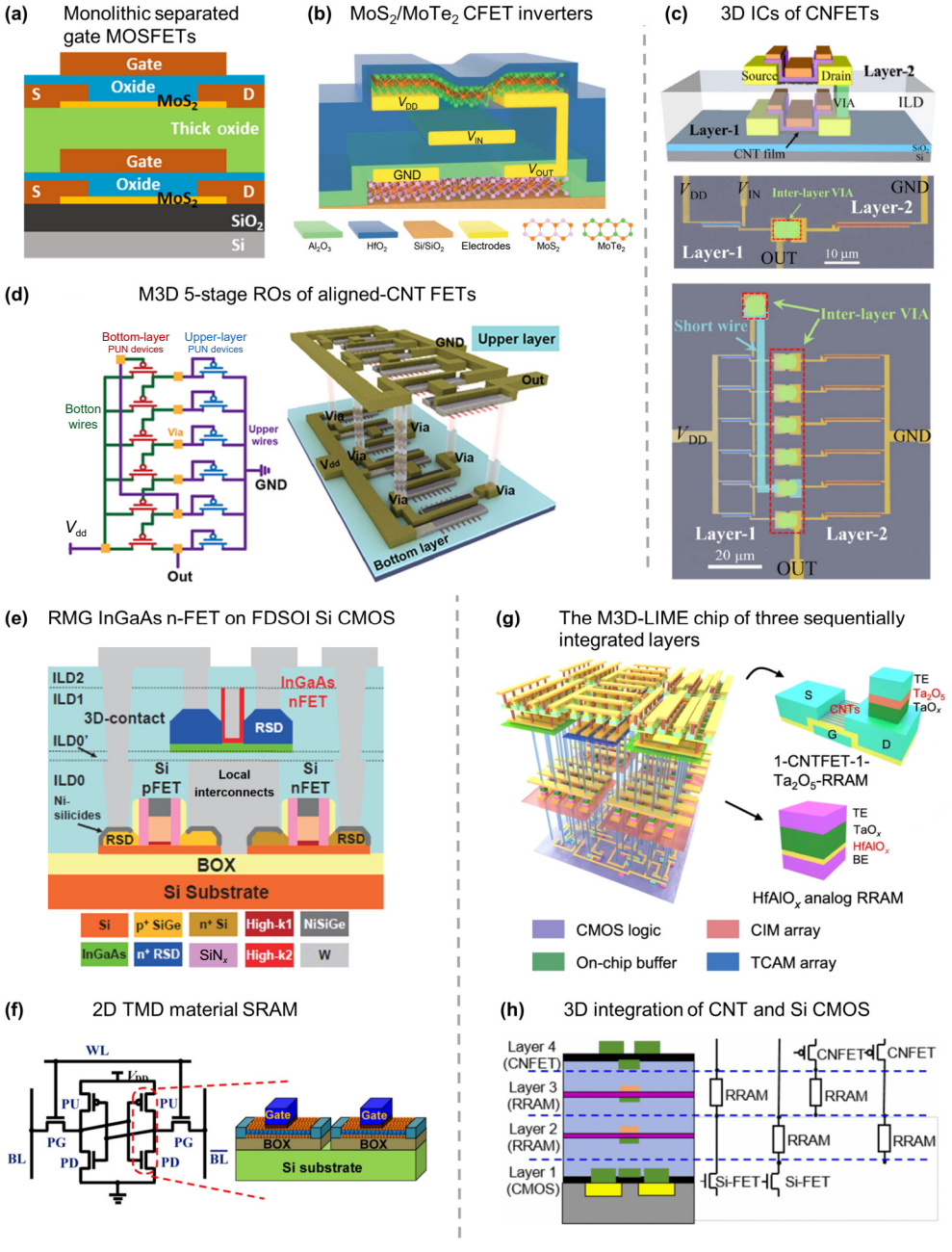

Figure 9 Applications of monolithic 3D integration: (a) Schematic cross-sectional view of a monolithic 3D architecture with separated gate MOSFETs. Reproduced with permission from Ref. [110], © WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim 2016. (b) Inverters achieved by $MoS_2/MoTe_2$ CFET based on CVD growth. Reproduced with permission from Ref. [121], © Wiley-VCH GmbH 2023. (c) Monolithic 3D ICs composed of dual layers of CNFETs and a false-colored SEM image of the fabricated ROs. Reproduced with permission from Ref. [106], © Tsinghua University Press and Springer-Verlag GmbH Germany, part of Springer Nature 2019. (d)The circuit diagram of the M3D 5-stage ring oscillators with drive and load FETs and the schematic of the M3D 5-stage ROs consists of stackable aligned-CNT FETs. Reproduced with permission from Ref. [107], © Fan, C. et al., InfoMat published by UESTC and John Wiley & Sons Australia 2023, Ltd. (e) Schematic showing the 3D monolithic stack of Replacement Metal Gate (RMG) InGaAs n-FET layer on FDSOI Si CMOS layer of a 3D 6T-SRAM at different stages of the fabrication. Reproduced with permission from Ref. [94], © VLSI Symposium 2017. All Rights Reserved. (f) SRAM structure is achieved by utilizing monolayer and bilayer 2D TMD material devices. Reproduced with permission from Ref. [147], © IEEE 2016. (g) The M3D-LIME chip consists of three sequentially integrated layers: Si CMOS logic for control and data interfacing, $HfAlO_x$-based analog RRAM 1T1R arrays for CNN feature extraction, and TCAM with CNFET and Ta_2O_5-based digital RRAM. Reproduced with permission from Ref. [148], © Li, Y. et al. 2023. (h) Implementing a vertical stacking 3D integration of CNT and Si CMOS, utilizing a 1T1R structure. Reproduced with permission from Ref. [131], © IEEE 2014.

FinFET technology with 3D monolithic techniques [82, 153], offer novel approaches to SRAM manufacturing. The use of TSV-free designs and small monolithic interior vias (MIVs) [154] has improved packaging density and reduced power consumption. To optimize performance, SRAM has transitioned from traditional 6T-SRAM cells to 8T-SRAM [155, 156], and from a 6N2P to a 4N4P structure [157]. These improvements will enhance access times, reduce leakage, and improve stability. However, as device dimensions shrink, SRAM faces challenges like process variations and short-channel effects. To address this, materials such as IGZO

[95, 158] and 2D materials [159] are being explored as potential alternatives for SRAM, offering promising solutions to improve performance and reliability.

Research by Yu et al. [147] has demonstrated that single-layer TMDs possess excellent electrostatic properties and superior stability (Fig. 9(f)), making them highly suitable for low-power SRAM applications. It is worth noting that double-layer TMDs exhibit higher carrier mobility, making them more appropriate for applications that require longer channel lengths and high-performance SRAM functionality.

Besides, monolithic 3D SRAM units incorporating n-MoS_2/p-WSe_2 configurations have also been proposed [160] to leverage the advantages of monolithic 3D integration, enabling the use of single- or multiple-layer TMDs for n-FET and p-FET layers. Superior nominal stability and enhanced read/write performance in 6T SRAM can be achieved by stacking a single-layer p-FET on a dual-layer n-FET, compared to conventional planar technology. When the device is near-threshold/sub-threshold, the optimal 3D configuration appears to be a single-layer p-FET stacked on a single-layer n-FET. Although three-layer TMD devices exhibit higher mobility, their implementation can negatively impact the performance of 3D logic circuits. Additionally, the exploration of monolithic 3D integration for near-threshold/sub-threshold operation in 8T SRAM cells has identified the configuration of a single-layer n-FET on top of a double-layer p-FET as the most effective design for 8T near-threshold/sub-threshold memory cells.

Currently, most studies have concentrated on substituting materials while maintaining the conventional 6T structure. The exploration of TMDC SRAM with an 8T configuration remains relatively scarce. Recently, SRAM cells based on silicon and MoS_2 have been proposed [141]. This development holds significant potential for pioneering new approaches in the realization of next-generation logic circuits, potentially enhancing their performance and energy efficiency.

5.1.3 *RRAM*

RRAM is a non-volatile memory technology that utilizes changes in resistance for information storage and retrieval. In conventional 2D integrated circuits, logic cells and memory cells are typically located in separate regions of the chip, resulting in extended data transmission distances. This spatial separation causes a significant mismatch in data transfer speeds between storage and computation, leading to the von Neumann bottleneck. To surpass this bottleneck, the M3D integration of logic and storage [131, 132, 150, 161, 162] offers a promising solution. A notable application is the development of non-von Neumann architectures enabling memory computing by vertically integrating logic and memory units [115]. Establishing computing and access circuits adjacent to memory arrays necessitates the vertical stacking of logic and memory layers, which concurrently reduces access delays and energy consumption [103].

A noteworthy structure was proposed by Li et al. [148], the M3D-LIME chip, a 3D integrated RRAM-based hybrid memory architecture for efficient one-shot learning which is shown in Fig. 9(g). There are three functional layers in the chip, the first one is for control and data interface which is fabricated by using a 130 nm CMOS process, the second layer for feature extraction uses $HfAlO_x$-based analog RRAM 1T1R arrays. The third layer is for template storage and matching comprised of Ta_2O_5-based digital RRAM TCAM arrays. The design achieves GPU-level accuracy with significant improvements in energy efficiency and processing speed.

Another vertical stacking 3D integration of CNT and Si CMOS using a 1T1R structure is illustrated in Fig. 9(h) [131]. This advanced integration approach interweaves logic and storage components vertically across different layers, substantially reducing data transmission distances. Consequently, this vertical alignment mitigates the von Neumann bottleneck by harmonizing data transfer speeds between storage and computation. Additionally, this integration methodology allows for the incorporation of a greater number of memory units on the same chip, significantly enhancing memory density and overall system performance.

Beyond improvements in data transfer efficiency and memory density, 3D monolithic integration offers additional advantages such as reducing power consumption due to shorter data transmission paths, thereby it will enhance energy efficiency in computing systems at the same time. Furthermore, 3D monolithic integration supports heterogeneous integration, enabling the seamless combination of various functionalities on a single chip. This flexibility facilitates the incorporation of diverse components, such as sensors and accelerators, resulting in a more versatile and powerful computing architecture.

2D materials have emerged as promising candidates for monolithic 3D memory, thanks to their exceptional electrical properties and low thermal requirements [114]. The ability to manufacture transistors based on 2D materials at lower temperatures is advantageous for integrating monolithic 3D memory. Various 2D materials have been explored for the creation of memory cells. For instance, Wang et al. [112] successfully fabricated 3D monolithically stacked 1T1R cells using single-layer MoS_2 FETs and hBN RRAM.

Moreover, the 3D integration of 2D materials transistors has achieved large-area memory structures. Vertical 3D integration based on 2D materials and Si CMOS technology has enabled the embedded 2T1R structure across the entire wafer [139], incorporating a 3-channel MoS_2 nFET meticulously engineered to match the threshold voltage. Besides, recent advancements mentioned in Section 4 have achieved the monolithic 3D integration of 2D transistors and vertical RRAMs within 1T-4R structures, facilitating the development of high-density memories [143]. Experimental results have validated the monolithic 3D integration of atomically thin MoS_2 transistors and 3D vertical RRAM, demonstrating the successful fabrication of 1T-nR structures. Utilizing high on/off-ratio MoS_2 transistors effectively suppresses leakage current and allows scalability to large-scale memory arrays. This integration strategy offers significant advantages, including a substantial reduction in chip area, read latency, and read and write energy consumption. Notably, the 1T-4R structure exhibits the best overall performance in these aspects, highlighting its potential for future high-density, energy-efficient memory technologies.

The synergy between low-dimensional materials and traditional semiconductors holds great promise, particularly for ultra low power systems and the advancement of both digital and analog circuits. The M3D integration of low-dimensional materials has great prospects in these areas, with enormous potential for expansion and breakthrough innovation.

5.2 Other applications

The M3D integration of low-dimensional materials extends beyond logic circuits, encompassing various applications such as utilizing CNT films and 2D materials as different kinds of sensors, as well as

optoelectronic integration.

As a 1D material, CNT has significant applications in M3D integration due to its unique properties. CNT logic transistors and sensors are compatible with low-temperature manufacturing processes, providing ample thermal budget for smart sensors in the construction of M3D systems. For instance, as mentioned before, Fan et al. [108] demonstrated the M3D sensing system was implemented by fabricating CNT CMOS ICs and CNT sensor arrays in two distinct layers in Fig. 10(a). Their sensing chips successfully achieved collaborative operation between the upper sensor layer and the bottom logic processing layer, opening up new possibilities for constructing universal sensing System-on-Chip architectures. M3D sensing technology holds the promise of constructing a universal sensing system and contributing to future smart sensing chips capable of multi-target detection and ultra-low power sensor functions.

Furthermore, CNTs lend themselves to monolithic optoelectronic integration, facilitating the production of photovoltaic receivers, electrically driven transmitters, and on-chip electronic circuits through CMOS-compatible low-temperature processes. For instance, Liu et al. [165] proposed versatile-functionality optoelectronic integrated circuits manufactured using low-temperature doping-free technology. These circuits employ a stacked processor and storage functional layers for optical communications, achieving higher communication speeds between layers compared to traditional optical fiber communications. In short, CNTs exhibit significant potential for achieving high-frequency and high-speed information transmission in the post-

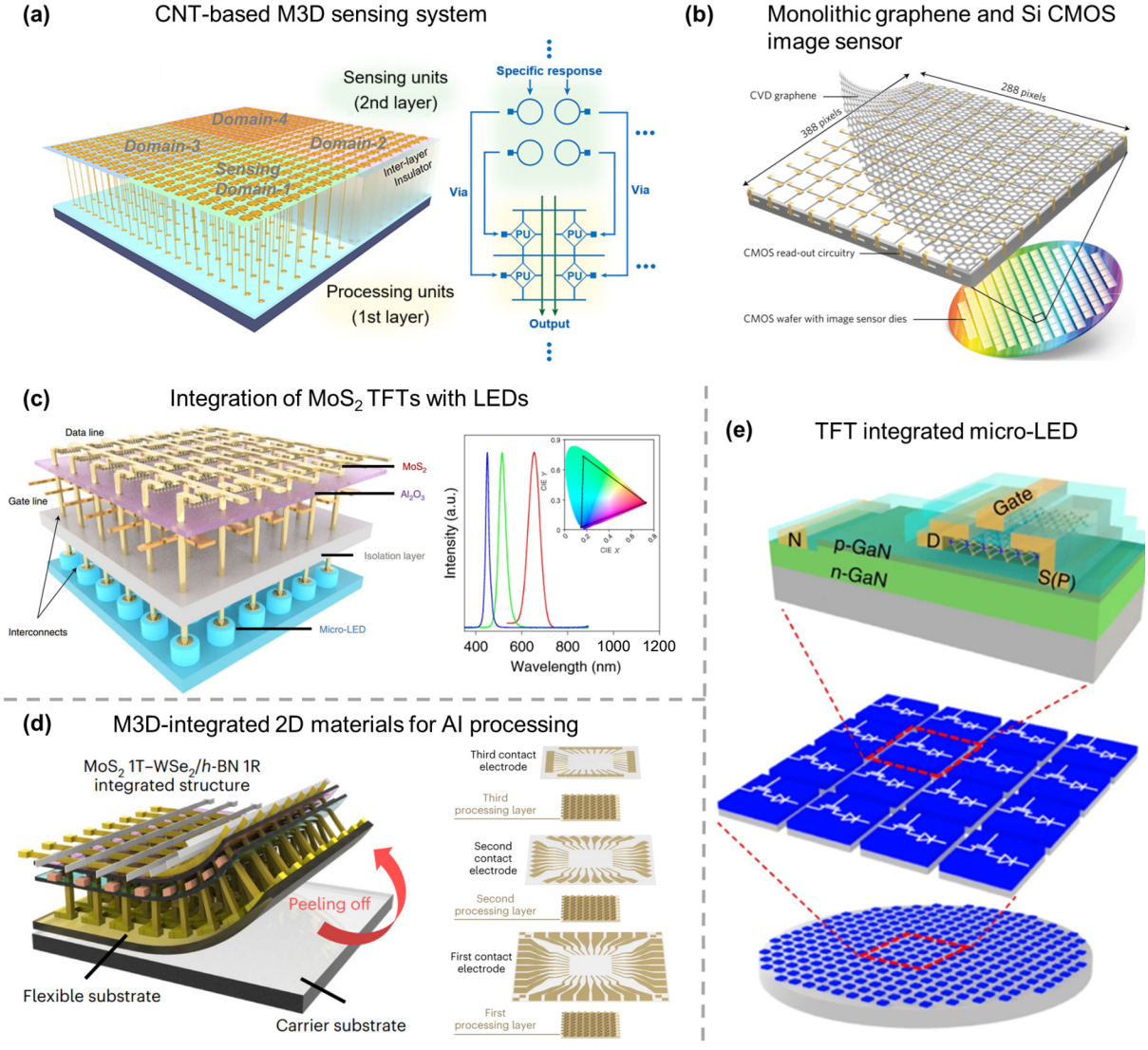

Figure 10 Other applications of 3D monolithic integration. (a) 3D schematic of the CNT-based M3D sensing system, featuring laminated CNT sensing and processing units connected through interlayer vias. Reproduced with permission from Ref. [108], © American Chemical Society 2023. (b) The back-end CMOS integration of CVD graphene and a 388 × 288-pixel image sensor readout circuit. Reproduced with permission from Ref. [136], © Springer Nature Limited 2017. (c) Monolithic integration of MoS_2 thin film transistors (TFTs) with micro-light emitting diodes (LEDs) and electroluminescence spectra and color range of RGB micro-LEDs. Reproduced with permission from Ref. [166], © Meng, W. et al., under exclusive license to Springer Nature Limited 2021. (d) Arrays of 1 transistor-1 memristor based on M3D-integrated 2D materials for AI processing and multiple stacked layers of M3D integrated AI processors. Reproduced with permission from Ref. [125], © Kang, J. et al., under exclusive license to Springer Nature Limited 2023. (e) Schematic illustration of the monolithic integration process, where GaN epitaxial layers for LEDs, MoS_2 layers for transistors, and QDs for color conversion are deposited and patterned on the same substrate. Reproduced with permission from Ref. [140], © Hwangbo, S. et al., under exclusive license to Springer Nature Limited 2022.

Moore era, enabling rapid communication and diverse functionalities within the same device.

2D materials have also been applied in many aspects beyond logic circuits. As shown in Fig. 6(d), when the top optical sensor is exposed to light, the photoelectric effect generates a photocurrent. The photocurrent passes through the intermediate logic circuit layer, where it is converted and amplified into a voltage signal. This signal is then output and loaded onto the bottom-layer storage devices, allowing the magnitude of the output signal from the storage devices to determine the presence or absence of light. Similarly, when the top sensor layer is replaced with other types of sensing layer or different logic and data storage devices, these vertically structured ICs can still work cooperatively, demonstrating their versatility and potential for various applications.

Recently, Xue et al. [163] introduced a bioelectronic sensing platform that employs high-speed readout electronics and machine learning for rapid, portable, and reliable measurements. Although their biosensors exhibit excellent performance, they are confined to planar structures. The incorporation of 3D structures, as discussed below, offers unique advantages.

3D integration of CMOS and single-layer graphene in gas sensors [164] combines graphene's exceptional properties with silicon's advantages, including low power consumption and cost-effectiveness. This development represents a significant stride toward scalable radio frequency gas sensors. Furthermore, the monolithic integration of graphene and Si CMOS can be employed in an image sensor (Fig. 10(b)) [136], functioning as a high-mobility phototransistor. A notable example includes an image sensor with a 388 × 288 array of graphene quantum dot photodetectors, serving as a highly sensitive digital camera for visible and short-wave infrared light. This demonstrates the capability of M3D graphene to realize image sensors with multi-million-pixel resolution, featuring a pixel pitch as low as 1 μm. Additionally, it underscores the potential of multi-layer stacking of graphene and other 2D materials to achieve more intricate functionalities in electronic devices.

In a recent study by Meng et al. [166] (Fig. 10(c)), an active matrix display with exceptional performance was developed, demonstrating excellent electrical properties and uniformity. This approach holds promise for wearable display devices, new transparent displays, and widespread applications in biomedicine and human-computer interaction. Moreover, M3D integration of 2D materials can be seamlessly integrated with the field of artificial intelligence. Researchers have achieved M3D integration of artificial intelligence processing hardware [125] (Fig. 10(d)), including 3 layers of artificial intelligence (AI) computing layers, 2 layers of signal-processing layers, and a sensor layer. The AI computing layers consist of a bottom MoS_2 transistor array and a top WSe_2/h-BN-based memristor neuromorphic computing array through M3D integration. This multi-layer M3D integration enhances functionality and reduces surface area, improving efficiency in terms of delay and occupied space. The short interconnections enable simultaneous processing of large volumes of sensor data with high bandwidth and low latency. M3D integration, coupled with near/in-sensor computing architecture, facilitates power-efficient edge computing solutions, providing material-level solutions for electronic devices and paving the way for future multifunctional computing hardware. By designing different layers, this approach can meet various demands for commercial applications, demonstrating the versatility and potential of this advanced integration technique. It is also worth mentioning that the integration of MoS_2 TFTs and micro-LEDs on a single chip can yield high-resolution displays (Fig.10(e)). By directly synthesizing a MoS_2 thin film on a GaN-based epitaxial wafer, a thin film wafer is created. The MoS_2 thin film transistor is then monolithically integrated with a micro-LED, resulting in a matrix micro-LED. Additionally, by printing quantum dots onto a blue micro-LED, the team successfully achieved scalable fabrication of full-color micro-LED displays.

In summary, low-dimensional materials and their monolithic 3D integration have found many applications in the fields of digital circuits, including inverters, SRAM, RRAM, etc. In addition to logic circuits, they are also used in various sensors, optoelectronics, and other fields. We believe that in the future, with the continuous development of material research and manufacturing processes, low-dimensional materials will achieve more applications and developments in a wider range of fields.

6 Conclusion

In conclusion, M3D integration represents a transformative approach in semiconductor technology, offering a pathway to enhance device density, performance, and functionality. By vertically stacking layers of devices within a single chip, M3D integration addresses the limitations of conventional 2D scaling, while maintaining high integration density and energy efficiency. This review highlights the key developments from bulk semiconductor-based M3D integration to the use of advanced low-dimensional materials like 2D TMDCs and CNTs, which offer superior electrical properties and scalability for next-generation electronics. The integration of these emerging materials into M3D structures has demonstrated substantial potential for applications in logic circuits, memory, sensors, optoelectronics, and AI processing, with benefits such as reduced power consumption and increased bandwidth. Despite these advancements, challenges remain in the areas of manufacturing scalability and integration with existing silicon-based technologies. Future research should focus on overcoming them to fully realize the potential of M3D integration for commercial applications. Overall, M3D integration with low-dimensional materials presents a promising avenue for the continued evolution of electronic devices and systems in the post-Moore's Law era.

Data availability

Not applicable.

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Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

Z. Y. H.: Writing manuscript, data compilation. H. T. L.: Writing manuscript, data compilation. M. D. Z., Z. M. J., J. X. L., W. K. F., and Y. Y. D.: Data compilation. X. L.: Writing manuscript, data curation, project administration. Y. H. and Y. L. W.: Project administration, funding acquisition. All the authors have approved the final manuscript.

Use of AI statement

None.

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