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High-performance trench-structured thin film transistor with a micropatterned double-layer oxide semiconductor of varying thickness

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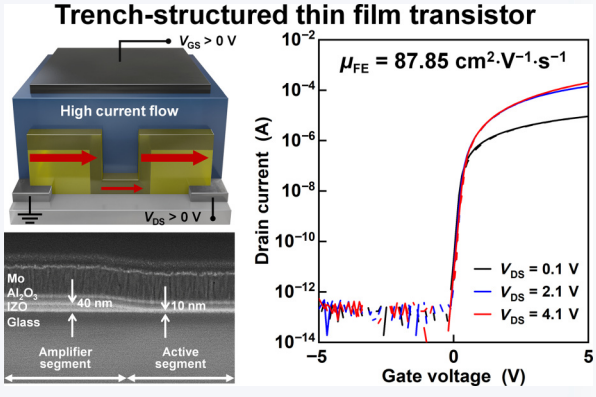
ABSTRACT: Amorphous oxide semiconductor thin film transistors (TFTs) are essential for next-generation high-resolution displays due to their superior electrical properties, stability, and compatibility with flexible substrates. This paper reports a novel TFT architecture featuring a trench-structured oxide semiconductor layer of varying thickness and a corresponding fabrication process, offering excellent current-driving capabilities, switching characteristics, and wafer-scale producibility compared to planar-structured TFTs and previous trench-structured TFTs (TS-TFTs). Our approach forms trenches through micropatterning the first oxide semiconductor layer deposited on the substrate, followed by the deposition of the second oxide semiconductor layer using an atomic layer deposition supercycle method. This process introduces a trench structure, comprising a micropatterned double-layer oxide semiconductor with a thin active segment and thick amplifier segments, between source and drain electrodes. This configuration allows for precise dimensional control of the active segment, facilitating an optimized TFT architecture design. The developed TS-TFTs exhibit excellent electrical properties, including a field-effect mobility of 87.84 $cm^2 \cdot V^{-1} \cdot s^{-1}$, a subthreshold swing of 0.074 $V \cdot dec^{-1}$, near-zero threshold voltage, negligible hysteresis, and a threshold voltage shift of 0.4 V under positive bias stress over 3600 s. Furthermore, an electrical performance analysis of 16 TS-TFTs fabricated on a 4-inch wafer shows that their transfer curves are almost coincident, demonstrating the feasibility of the proposed fabrication process for wafer-scale production.



KEYWORDS: thin film transistor, trench structure, oxide semiconductor, current-driving capabilities, switching properties, scalable fabrication

1 Introduction

Display technology has continually evolved to offer users high-resolution and large-scale visual information [1–3]. In these applications, thin film transistors (TFTs) are essential as driving switches that control light-emitting diodes in display backplanes, making their electrical performance critical [4–6]. Among various TFTs, amorphous oxide semiconductor TFTs have emerged as particularly advantageous for driving high-resolution displays while maintaining consistent quality over extensive areas [7–15]. These TFTs are fabricated at relatively low temperatures, which facilitates efficient processing and renders them suitable for next generation displays [16], wearable touch sensors [17], and neuromorphic chips [18]. However, the disordered atomic structure of amorphous oxide semiconductors can create defects in the charge migration pathway, limiting field-effect mobility and thereby degrading electrical

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performance [19–22]. Therefore, to meet the evolving requirements of high-performance electronic devices, it is urgent and crucial to develop oxide semiconductor TFTs with enhanced efficiency and reliability [23–28].

In conventional oxide semiconductor TFTs with a planar structure, the electrical properties significantly depend on the total number of carriers in the oxide semiconductor channel layer [29–31]. Therefore, the TFTs become more conductive with increasing channel thickness, which increases the total number of carriers in the channel. Conversely, they exhibit better switching characteristics when the channel is thin due to the reduction in the total number of carriers. Based on this principle, TFTs with an intriguing structural architecture featuring a trench-structured oxide semiconductor layer have recently been reported [32–34]. The core of the proposed trench-structured TFTs (TS-TFTs) is the creation of a trench structure on the substrate surface using dry etching. Subsequently, radiofrequency sputtering is employed to deposit the oxide semiconductor. This process results in an anisotropic deposition rate between the horizontal part and the side wall of the trench structure. Consequently, the thickness and surface roughness of the oxide semiconductor differ between the horizontal and vertical sections of the trench. The side wall of the trench structure forms a thin oxide semiconductor layer with a rough surface, which dominates the switching characteristics of the TFTs, effectively acting as the active channel. In contrast, the horizontal part forms a thick oxide semiconductor layer with a smooth surface, which determines the TS-TFT's current-driving capabilities.

Due to this mechanism, the proposed TS-TFTs comprise a thin active segment that controls switching characteristics and a thick amplifier segment that governs current-driving capabilities. This configuration results in superior electrical properties, including both enhanced current-driving capabilities and improved switching characteristics. However, in the proposed fabrication method, the process of depositing the oxide semiconductor into the trench structure using radiofrequency sputtering fails to precisely control the dimensions (thickness and length) of the oxide semiconductor deposited on the side wall. This lack of control makes it challenging to design the structural architecture of the TS-TFTs. Additionally, creating trench structures on a thermal oxide silicon (Si/SiO_2) wafer using dry-etching with CF_4 or CHF_3 gas often results in uneven etching across the entire wafer surface, making it unsuitable for large-area production. Moreover, the use of dry etching imposes limitations on the substrate materials that can be used. This method cannot be applied to flexible electronic applications, such as the fabrication of TFTs on flexible polymer substrates, posing a significant disadvantage.

In this study, we develop a novel TS-TFT architecture and a corresponding fabrication process to address the shortcomings identified in previous TS-TFT manufacturing methods. Unlike previous TS-TFTs, our approach creates trenches on a substrate by micropatterning the first oxide semiconductor layer deposited on the substate, which is followed by the deposition of the second oxide semiconductor layer. This process introduces a trench-structured oxide semiconductor layer of varying thickness, comprising a thin active segment and a thick amplifier segment, between the source and drain electrodes. This approach enables accurate dimensional control of the active segment in the trench structure, facilitating the structural architecture design of TS-TFTs. We demonstrate the feasibility of the developed TS-TFTs by scrutinizing the operating mechanism and electrical properties. Furthermore, the scalability of the developed TS-TFT fabrication method for large-area production is examined by comparing the electrical properties of TS-TFTs fabricated on a 4-inch wafer.

2 Experimental

2.1 Plasma-enhanced atomic layer deposition

Plasma-enhanced atomic layer deposition (PEALD) equipment based on a showerhead-type design (Atomic-premium, CN1, Korea) was utilized for the deposition of indium oxide (In_2O_3), zinc oxide (ZnO), and aluminium oxide (Al_2O_3). The precursors employed for this process were 3-(dimethylamino)propylindium (DADI) for indium, diethylzinc (DEZ) for zinc, and trimethylaluminum (TMA) for aluminum. DADI was stored at 40 °C in a specialized bubble-type container, whereas DEZ and TMA were kept at room temperature in single-valve canisters. The deposition of metal oxides involved utilizing a 100 W oxygen plasma as the reactive species, which was introduced into the reaction chamber via a radio frequency generator. The oxygen gas flow for the plasma was maintained at a constant rate of 500 sccm. Argon gas served both as a carrier gas to transport the precursor to the substrate, with flow rates of 50 sccm for DADI and 500 sccm for DEZ and TMA, and as a purging agent, with purge rates of 1000 sccm for DADI and 500 sccm for DEZ and TMA. The In_2O_3 deposition sequence included a DADI pulse for 1 s, an argon purge for 10 s, oxygen gas exposure for 1 s, oxygen plasma for 2 s, followed by an argon purge for 10 s. The ZnO deposition sequence consisted of a DEZ pulse for 0.1 s, an argon purge for 10 s, oxygen gas exposure for 1 s, oxygen plasma for 2 s, followed by an argon purge for 10 s. The Al_2O_3 deposition sequence consisted of a TMA pulse for 0.1 s, an argon purge for 10 s, oxygen gas exposure for 1 s, oxygen plasma for 2 s, followed by an argon purge for 10 s.

To precisely control the thickness of the IZO and Al_2O_3 layers deposited via PEALD, we first calibrated the deposition process on a Si wafer. Using the PEALD supercycle method, we deposited 50 cycles of IZO and Al_2O_3 and measured the thickness using ellipsometry at variable angles of 65°, 70°, and 75°. Based on these measurements, we calculated the required number of cycles to achieve the desired thickness for the actual deposition.

2.2 Structural and dimensional measurements

Optical microscopy (BX53M, Olympus, Japan) was used to measure the overall structures of the TFTs. The microscope was configured with Olympus Stream image analysis software, employing a bright field contrast method. A scanning electron microscopy (SEM) combined with a focused ion beam milling system (Helios G5, Thermo Fisher Scientific, USA) was used to characterize microstructural features and dimensions of the TFTs by capturing top-view and cross-sectional images. The SEM, equipped with an Everhart-Thornley secondary electron detector, was operated at an accelerating voltage of 5 kV and a working distance of 4 mm. To characterize the dimensions and surface roughness of an indium-zinc oxide (IZO) semiconductor layers in the TFTs, atomic force microscopy (AFM) (MFP-3D, Oxford Instruments, UK) was employed. Measurements were conducted in tapping mode using a soft tip (ATEC, Nanosensors, Switzerland) with a spring constant of 68 $N \cdot m^{-1}$. The scan rate was set between 0.1 and 0.5 Hz, and the set point was fixed at 680 mV.

2.3 Measurements of electrical properties

The transfer curves, output curves, capacitances, and positive bias stress stability of the TFTs were measured using a semiconductor parameter analyzer (HP 4156A, Keysight, USA) equipped with a four-point probe station under controlled conditions of room temperature and darkness. The transfer curves were obtained by measuring the drain current (I_D) while sweeping the gate voltage (V_{GS}) from −5 to 5 V at three drain voltages (V_{DS}): 0.1, 2.1, and 4.1 V. The output curves were obtained by measuring the drain current while sweeping the drain voltage from 0 to 10 V at gate voltages of 0, 1, 2, 3, 4, and 5 V. The capacitance of the Al_2O_3 gate insulator layer was measured by sweeping the voltage from −5 to 5 V, using an alternating current (AC) signal with a frequency of 1 MHz. Positive bias stress stability was assessed under an electric field of 1 MV·cm^{-1} with stress times up to 3600 s, during which transfer curves were measured by sweeping the gate voltage from −5 to 5 V at a drain voltage of 0.1 V. For all measurements, the voltage interval was set at 0.1 V, which was sufficient to detect changes in the current-voltage characteristics and provided an accurate assessment of the electrical properties.

The field-effect mobility (μ_{FE}) of the TFTs was calculated in the linear region at low gate voltages of the transfer curve using the relation $\mu_{FE} = Lg_m/WC_iV_{DS}$, where W is the channel width, L is the channel length, g_m is the transconductance (defined as $\partial I_D/\partial V_{GS}$), and C_i is the capacitance per unt area of the gate insulator. The subthrshold swing (s.s) was calculated as the reciprocal of the maximum slope of the transfer curve, using the relation s.s = $(\partial \log_{10}(I_D)/\partial V_{GS})^{-1}$. The dielectric contant (k_{ox}) of the gate insulator was determined using the relation $k_{ox} = CT/A\varepsilon_0$, where C is the capacitance, T is the thickness of the gate insulator layer, A is the capacitor area, and ε_0 is the permittivity of free space.

3 Results and discussion

3.1 Design and fabrication of TS-TFTs

Figure 1(a) illustrates the schematics of the structural configurations and operating mechanisms of a planar-structured TFT (PS-TFT) and the proposed TS-TFT. Both TFTs utilize a top-gate bottom-contact structure, comprising a substrate, source/drain electrodes, an oxide semiconductor channel, a gate insulator, and gate electrodes. The PS-TFT features a typical TFT configuration, employing a homogeneous monolayer oxide semiconductor. In contrast, the proposed TS-TFT incorporates a trench-structured oxide semiconductor layer with varying thickness. The mask layout and the top-view optical microscope image are presented in Figs. S1 and S2 in the Electronic Supplementary Material (ESM). In this design, a thin active segment is located at the horizontal part of the trench, while thick amplifier segments are situated on either side of the active segment.

The critical difference in structural architecture compared to previously reported TS-TFTs lies in the creation of trench structures. In our design, these trenches are formed by

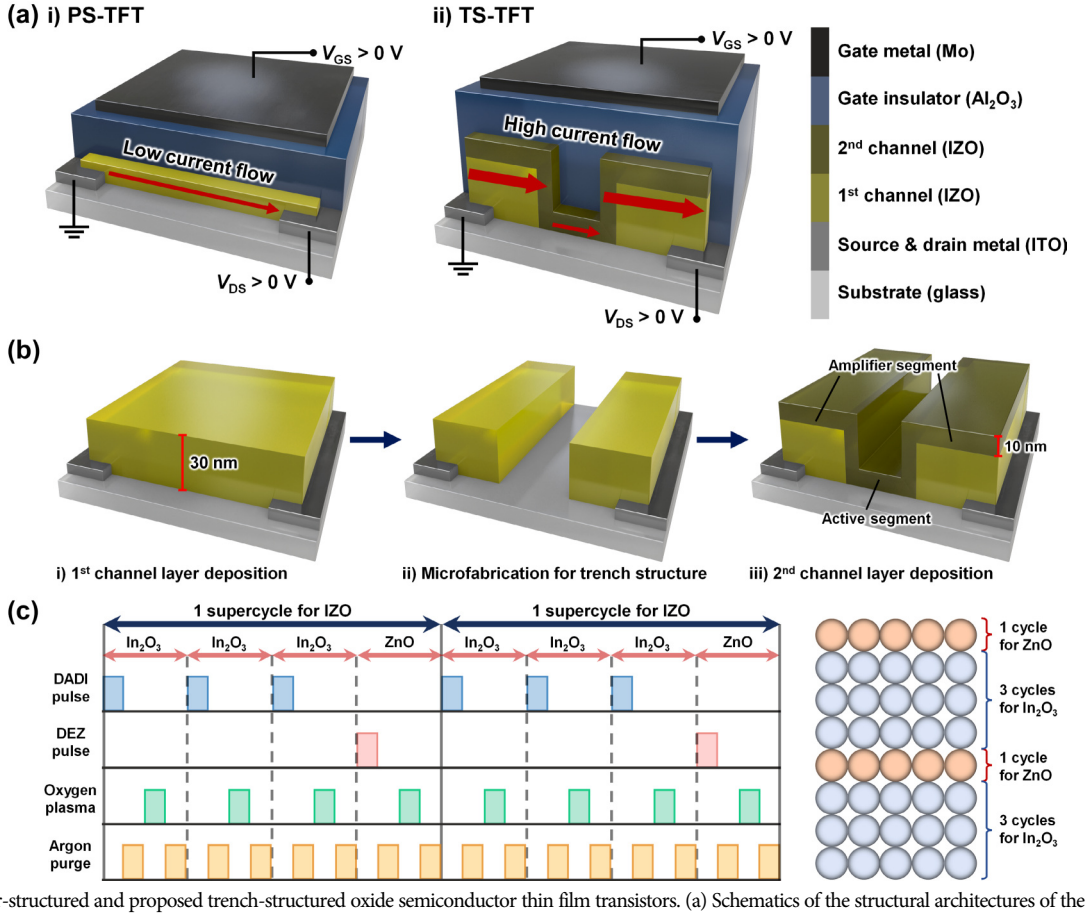

Figure 1 Planar-structured and proposed trench-structured oxide semiconductor thin film transistors. (a) Schematics of the structural architectures of the two TFTs with a top-gate bottom-contact configuration. (b) Fabrication process of the trench structure in the TS-TFT, where different colors are used to distinguish the first and second IZO semiconductor layers, despite both being made of the same material. (c) Plasma-enhanced atomic layer deposition supercycle for depositing the IZO semiconductor layers.

micropatterning the first oxide semiconductor layer deposited on the substrate, whereas in previous TS-TFTs [32–34], the trench structures were created by dry etching directly into the substrate (Fig. S3 in the ESM). Subsequent deposition of the second oxide semiconductor results in a micropatterned double-layer oxide semiconductor with the thin active segment and the thick amplifier segments between the source and drain electrodes. This approach allows for accurate dimensional control of the active segment in the trench structure, facilitating the structural architecture design of TS-TFTs. Additionally, by avoiding the dry etching process to create trench structures in the substrate, our method achieves dimensional uniformity for TS-TFTs fabricated on a large-area substrate, ensuring wafer-scale producibility. Furthermore, since there is no need to etch the substrate to create the trench structure, TS-TFTs can be fabricated on various substrate materials, including polymers. This expands the applicability of TS-TFTs to various industrial fields, including flexible electronic applications.

The operating principle of TFTs is based on the modulation of current flowing between the source and drain electrodes, regulated by the gate voltage [35, 36]. Under a negative gate voltage, TFTs remain non-conductive with minimal current flow. However, when a positive voltage is applied, an electric field is induced in the semiconductor, controlling the movement of charges. When the gate voltage reaches a specific threshold, it induces the formation of a conductive channel in the semiconductor layer, allowing for electron flow between the source and drain electrodes. In the proposed TS-TFT, the oxide semiconductor layers with different thicknesses, namely the thin active segment and the thick amplifier segment, play distinct roles in the electrical properties. The thick amplifier segments act as fast-current paths, boosting the on-current and increasing the field-effect mobility of charge carriers, thereby enhancing current flow. Meanwhile, the thin active segment functions as the channel, controlling the switching properties. More details on this issue will be provided in Section 3.3.

Figure 1(b) shows the fabrication process of the trench structure with the top-gate bottom-contact configuration in the proposed TS-TFT. First, source/drain electrodes are micropatterned on a glass substrate pre-deposited with a 150-nm-thick transparent conductive oxide (indium tin oxide, ITO). Subsequently, the IZO semiconductor layer is deposited using the PEALD supercycle method. The PEALD supercycle method is a cyclical approach integrating three cycles for In_2O_3 and a single cycle for ZnO per sequence (Fig. 1(c)), and provides superior IZO semiconductor quality [37–39]. The first IZO layer is deposited to a thickness of 30 nm at 200 °C and then micropatterned into trench structures. A second IZO layer is subsequently deposited using the PEALD supercycle method at 200 °C, forming a 10-nm-thick active segment. It should be noted that after the deposition of the first IZO layer, micropatterning for the trench structure is performed with a 1 μm pattern margin between the mask layouts of the first and second IZO layers (Fig. S1(b) in the ESM). This ensures precise alignment during the second IZO layer deposition, allowing micropatterning to occur within the defined region, thereby achieving the accurate formation of the trench structure. To minimize excessive free-carrier generation due to hydrogen incorporation and to ensure optimal on/off characteristics, the active segment is treated with oxygen plasma [40]. After that, a 50-nm-thick Al_2O_3 layer of gate insulator is deposited using PEALD at 200 °C with a trimethylaluminum source. Finally, a 150-nm-thick molybdenum (Mo) layer of gate electrode is deposited by direct current sputtering. After fabrication, all TFTs are annealed at 270 °C for 2 h, followed by an additional annealing at 300 °C for 2 h, to enhance electrical properties through hydrogen diffusion [41–44].

3.2 Structural and dimensional characterization

The structural configurations and dimensions of the fabricated TS-TFT with a 40-nm-thick amplifier segment and a 10-nm-thick, 2-μm-long active segment (channel legnth: 10 μm) were characterized using SEM and AFM. Figure 2(a) presents the top-

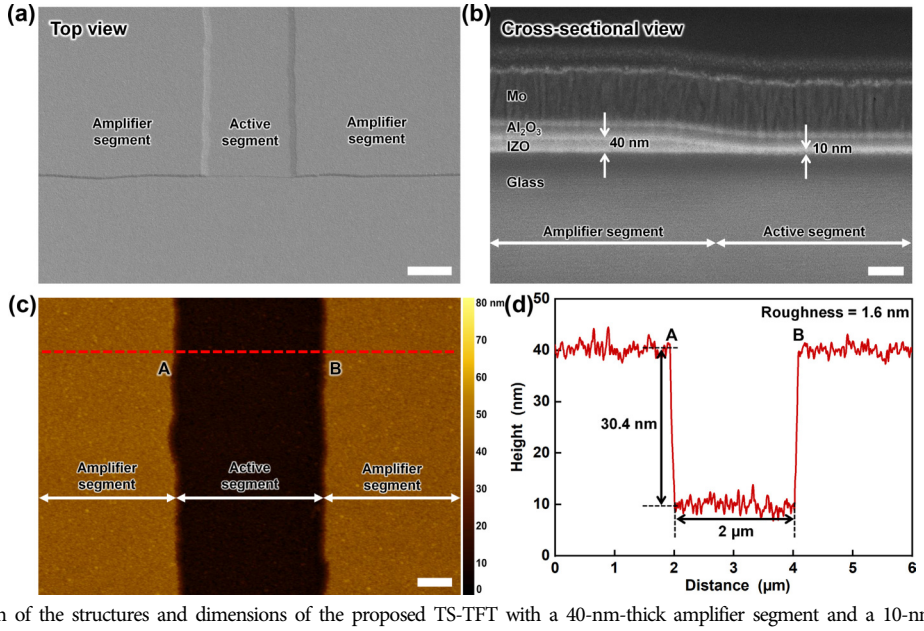

Figure 2 Characterization of the structures and dimensions of the proposed TS-TFT with a 40-nm-thick amplifier segment and a 10-nm-thick, 2-μm-long active segment (channel length: 10 μm). (a) Top-view SEM image of the trench-structured oxide semiconductor layer taken at a 40° tilt angle (scale bar: 1 μm). (b) Cross-sectional SEM image of the TS-TFT after focused ion beam milling (scale bar: 100 nm). (c) AFM topographic image of the trench-structured oxide semiconductor layer (scale bar: 500 nm). (d) Height profile along lines A and B in (c). Note that (a) and (c) were taken in regions where the gate insulator and gate electrode were not deposited.

view SEM image of the IZO semiconductor layer in the TS-TFT. The step-like features between the active segment and the amplifier segments indicate a thickness difference, suggesting the formation of a trench structure in the IZO semiconductor layer. The cross-sectional SEM image of the TS-TFT (Fig. 2(b)) clearly shows the IZO semiconductor layer with distinct regions of different thicknesses: the active segment at 10 nm and the amplifier segments at 40 nm. This confirms the varying thickness of the IZO semiconductor layer. Figures 2(c) and 2(d) show the AFM topographic image of the trench structure in the IZO semiconductor layer and the height profile along lines A and B in Fig. 2(c), respectively. The active segment exhibited a length of 2 μm and a thickness difference of approximately 30 nm compared to the amplifier segments. Additionally, the surface roughness of the IZO semiconductor layer was measured to be 1.6 nm, enabling precise dimensional control of the TS-TFTs.

The uniformity of the Al_2O_3 gate insulator layer thickness across the entire channel was further examined by measuring the capacitance per unit area. Capacitor pads comprising a metal (ITO)-insulator (50-nm-thick Al_2O_3)-metal structure (Mo), with two different areas of 100 μm × 100 μm and 200 μm × 200 μm, were fabricated on the same wafer used for the TS-TFTs (Fig. S4(a) in the ESM). As shown in Fig. S4(b) in the ESM, the capacitance per unit area–voltage curves for all capacitors were nearly identical, converging into a single curve. Moreover, the capacitance per unit area remained constant at an average of 0.135 μF·cm^{-2}, regardless of the applied voltage. The dielectric constant, calculated based on the thickness, was found to be 7.6 on average (Fig. S4(c) in the ESM), which is consistent with previous studies [45, 46]. This uniformity in the electrical properties demonstrates that the PEALD-deposited Al_2O_3 gate insulator layer has a precisely controlled thickness, ensuring consistent electrical characteristics [47–49].

These results confirm that the structural configurations and dimensions of the fabricated TS-TFT are consistent with the structural architecture design. This demonstrates the capability for accurate dimensional control using the proposed method and suggests the scalability of this process for large-area production.

3.3 Role of channel thickness in electrical properties

To understand the operating mechanism of the proposed TS-TFTs, we fabricated PS-TFTs with two different IZO semiconductor layer thicknesses of 10 nm (thin channel) and 40 nm (thick channel), corresponding to the thicknesses of the active segment and the amplifier segment in the TS-TFT, respectively. We explored their electrical properties by measuring the transfer curves using a four-point probe station (Fig. S5 in the ESM). The width and length of the IZO layer in the PS-TFTs were fixed at 20 and 10 μm, respectively, and the same fabrication process used for TS-TFTs was employed.

Figure 3 presents the transfer curves (drain current–gate voltage characteristics) and the output curves (drain current–drain voltage characteristics) of two PS-TFTs. The PS-TFT with a thin channel (Fig. 3(a)) exhibited well-operating TFT characteristics with a field-effect mobility of 36.11 cm^2·V^{-1}·s^{-1}, an on-current per width of 3.85 μA·μm^{-1} at drain voltage of 4.1 V, a hysteresis of 0.1 V, a threshold voltage of 0.1 V, and a subthreshold swing of 0.072 V·dec^{-1} (Fig. 3(b)). Note that the electircal properties, including field-effect mobility, hysteresis, threshold voltage, and subtreshold swing, were calculated at V_{DS} = 0.1 V. As shown in Fig. 3(c), the output characteristic curves of the PS-TFT with a thin channel exhibited linear behavior at low drain voltages, indicating ohmic contact. However, as the drain voltage increased, the drain current saturated, demonstrating its functionality as a TFT. Despite having good switching properties, with minimal hysteresis, a nearly zero threshold voltage, and a high subthreshold swing, the thin-channel PS-TFT had low field-effect mobility and a small on-current per width, which limited its current-driving capabilities.

On the other hand, the PS-TFT with a thick channel (Fig. 3(d)) exhibited conductive properties without switching behavior during the gate voltage sweep from −5 to 5 V (Fig. 3(e)). The output

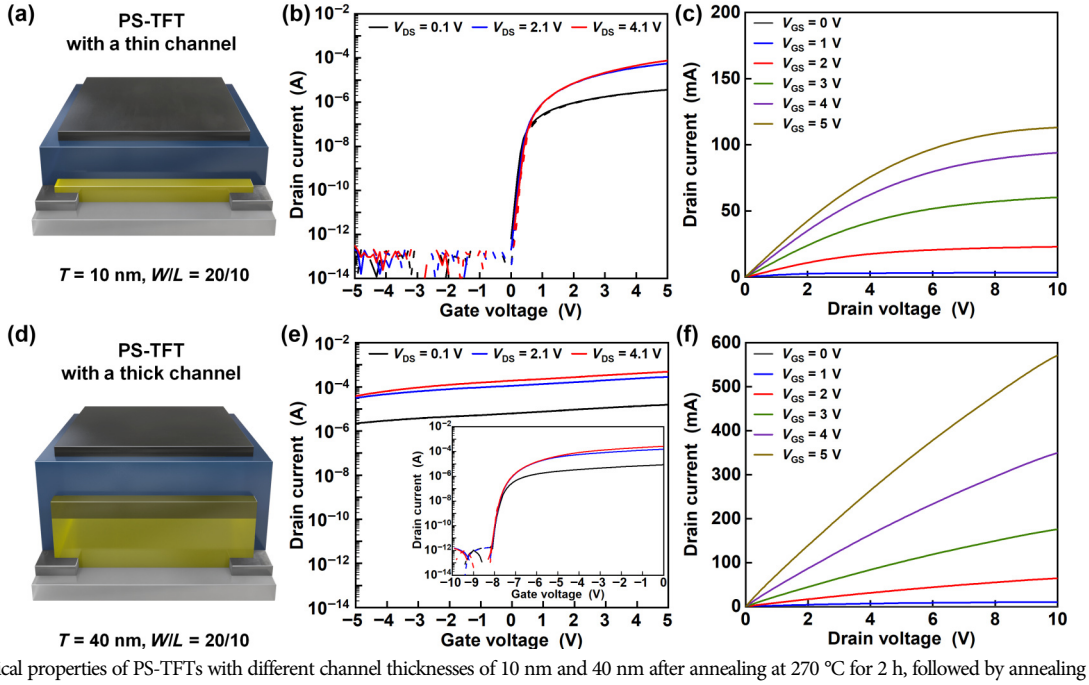

Figure 3 Electrical properties of PS-TFTs with different channel thicknesses of 10 nm and 40 nm after annealing at 270 °C for 2 h, followed by annealing at 300 °C for 2 h. (a) Schematic, (b) transfer curves, and (c) output curves of the PS-TFT with a 10-nm-thick channel. (d) Schematic, (e) transfer curves, and (f) output curves of the PS-TFT with a 40-nm-thick channel. The solid and dashed lines in (b) and (e) represent forward and reverse sweeps, respectively.

characteristic curves also showed that the drain current increased almost linearly with the drain voltage, without reaching saturation (Fig. 3(f)), failing to demonstrate typical TFT characteristics. However, the transfer curves of the thick-channel PS-TFT differed significantly from those of a conductor (Fig. S6(a) in the ESM). While the drain current in the conductor remained constant during the gate voltage sweep from −5 to 5 V (Fig. S6(b) in the ESM), the drain current in the PS-TFT with a thick channel increased with increasing gate voltage (Fig. 3(e)). To further investigate the current-voltage characteristics of the thick-channel PS-TFT, we obtained transfer curves by sweeping the gate voltage from −10 to 0 V. Interestingly, as shown in the inset of Fig. 3(e), on/off switching behavior appeared with a significantly negative-shifted threshold voltage of −8.1 V, indicating that the thick-channel PS-TFT was still operational as a TFT. Despite its poor switching characteristics, the thick-channel PS-TFT exhibited a high on-current per width of 24.64 μA·μm^{-1} at a drain voltage of 4.1 V, demonstrating enhanced current-driving capabilities.

In thick-channel PS-TFTs [50–52], the number of charge carriers generated by donors is relatively higher. These charge carriers transition into the conduction band, acting as free electrons and enabling current flow within the semiconductor channel. Although surface defects or impurities trap some electrons, forming a depletion region, the large number of charge carriers in the thick channel ensures sufficient carriers remain to contribute to channel formation, even if some are trapped at the surface. As a result, thicker semiconductor layers are less influenced by surface states, reducing the gate voltage required for channel formation and causing a negative shift in the threshold voltage. Additionally, the increased number of charge carriers raises the charge density in the channel, reducing resistance and improving current flow. Consequently, the current passing between the source and drain (on-current per width) increases.

Based on these results, we infer that in the TS-TFTs, the thin active segment controls the on/off switching properties, while the thick amplifier segment enhances current-driving capabilities. Therefore, the combined operation of these two mechanisms enables the TS-TFTs to achieve both good switching properties and high current-driving capabilities.

3.4 Enhanced electrical properties

Figure 4 and Fig. S7 in the ESM illustrate the transfer curves of the TS-TFT with a 40-nm-thick amplifier segment (Fig. 4(a)) and a 10-nm-thick, 2-μm-long active segment at drain voltage of 0.1, 2.1, and 4.1 V (the widths of both the amplifier and active segments were fixed at 20 μm), comparing how they change with thermal annealing. The as-fabricated TS-TFT without thermal annealing exhibited a field-effect mobility of 7.80 cm^2·V^{-1}·s^{-1}, an on-current per width of 0.81 μA·μm^{-1} at drain voltage of 4.1 V, a hysteresis of 2.8 V, a threshold voltage of 0 V, and a subthreshold swing of 0.075 V·dec^{-1} (Fig. S7(a) in the ESM). After annealing at 270 °C for 2 h (Fig. S7(b) in the ESM), the electrical properties improved, resulting in a field-effect mobility of 40.57 cm^2·V^{-1}·s^{-1}, an on-current per width of 4.08 μA·μm^{-1} at drain voltage of 4.1 V, a hysteresis of 1.9 V, a threshold voltage of 0 V, and a subthreshold swing of 0.064 V·dec^{-1}. Further annealing at 300 °C for 2 h achieved high-performance TFT characteristics by enhancing both current-driving capabilities and switching properties, as shown in Fig. 4(b). The field-effect mobility and on-current per width at at drain voltage of 4.1 V were 87.85 cm^2·V^{-1}·s^{-1} and 9.86 μA·μm^{-1}, respectively, with hysteresis and threshold voltage approximately zero and a subthreshold swing of 0.073 V·dec^{-1}. These results reveal that compared with the counterpart PS-TFT featuring a 10-nm-thick and 10-μm-long channel (Figs. 3(a)–3(c)), the field-effect mobility and on-current per width of the TS-TFT increased by 2.4-fold and 2.6-fold, respectively, while maintaining excellent switching properties. Moreover, according to the positive bias stability test under an electric field of 1 MV·cm^{-1}, the TS-TFT exhibited a threshold voltage shift of only 0.4 V over 3600 s, indicating superior stability (Fig. 4(c)). Therefore, we can infer that incorporating the trench-structured IZO semiconductor layer with two distinct thicknesses between the source and drain electrodes results in high-performance TFTs, offering a desirable combination of superior current-driving capabilities, good switching properties, and high stability.

To understand the roles of the trench-structured IZO semiconductor layer in the electrical properties of TS-TFTs in detail, we fabricated a PS-TFT with an IZO channel layer of 2 μm length, 10 nm thickness, and 20 μm width, corresponding to the dimensions of the active segment in the TS-TFT, by extending a transparent oxide conductor, which reduces the distance between the source and drain electrodes (i.e., the channel length) to 2 μm (the inset in Fig. S7(e) in the ESM). As shown in Fig. S7(c) in the ESM, the as-fabricated PS-TFT showed inferior current-driving capabilities with a field-effect mobility of 10.27 cm^2·V^{-1}·s^{-1} and an on-current per width of 8.38 μA·μm^{-1} at V_{DS} = 4.1 V, along with poor switching properties with a hysteresis of 2.2 V, a threshold voltage of 0 V, and a subthreshold swing of 0.080 V·dec^{-1}. However, annealing significantly improved the electrical properties, achieving a field-effect mobility of 37.77 cm^2·V^{-1}·s^{-1}, an on-current per width of 40.39 μA·μm^{-1} at V_{DS} = 4.1 V, a hysteresis of 0.1 V, and a subthreshold swing of 0.087 V·dec^{-1} (Figs. S7(d) and S7(e)). This field-effect mobility is comparable to that of the PS-TFT with an IZO semiconductor layer of 10 μm length, 10 nm thickness, and 20 μm width (Figs. 3(a)–3(c)), but is approximately 43% of that of the TS-TFT. These results indicate that channel thickness dominates the field-effect mobility of TFTs, and in TS-TFTs, the thick amplifier segment controls the field-effect mobility.

The high on-current per width of 40.39 μA·μm^{-1} is attributed to a significant negative shift in threshold voltage after annealing. A high negative threshold voltage of −2.3 V was measured for the PS-TFT. As the channel length decreases, oxide semoconductor TFTs operates in depletion mode due to the high charge density in the channel, requiring higher negative gate voltages for depletion. Therefore, shorter channels lead to transfer characteristics that are negatively shifted compared to TFTs with longer channels [43, 44]. A negative threshold voltage impairs the switching properties of TFTs, thereby degrading performance and reliability through increased leakage current, reduced noise margin, and higher power consumption [45–47]. These findings suggest that the PS-TFT structure cannot achieve both high current-driving capabilities and good switching properties simultaneously, which can only be accomplished through our proposed TS-TFT structural design.

We examined the effects of the active segment length on the electrical properties of TS-TFTs, where the active segement length varied from 2 to 6 μm while keeping the active segment thickness and width constant at 10 nm and 20 μm, respectively (the total length of the active and amplifier segments, i.e., the channel length, was fixed at 10 μm). Figures 4(d) and 4(e) present the transfer curves while sweeping the gate voltage from 0 to 5 V at drain

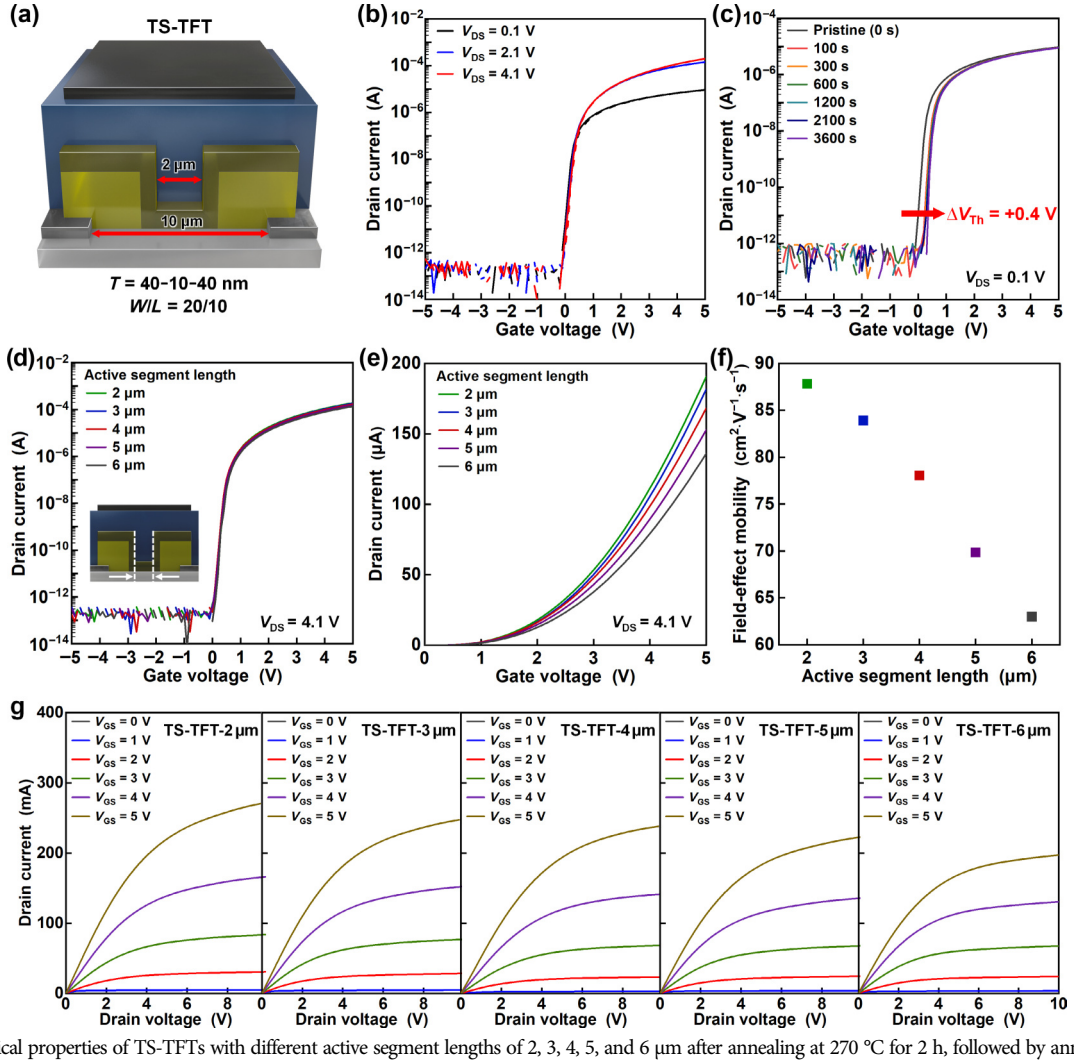

Figure 4 Electrical properties of TS-TFTs with different active segment lengths of 2, 3, 4, 5, and 6 μm after annealing at 270 °C for 2 h, followed by annealing at 300 °C for 2 h. (a) Schematic, (b) transfer curves, and (c) positive bias stress stability test results of the TS-TFT with a 40-nm-thick amplifier segment and a 10-nm-thick, 2-μm-long active segment (channel length: 10 μm). Comparison of the transfer curves at V_{DS} = 4.1 V for TS-TFTs with different active segment lengths of 2, 3, 4, 5, and 6 μm (channel length: 10 μm), plotted with (d) a logarithmic *y*-axis and (e) a linear *y*-axis. (f) Calculated field-effect mobility values. (g) Output curves of the five TS-TFTs. The solid and dashed lines in (b)–(d) represent forward and reverse sweeps, respectively.

voltage of 4.1 V. As the active segment length increased, both the field-effect mobility and on-current per width, i.e., the current-driving capabilities, gradually decreased (Table S1 in the ESM). The field-effect mobility was 87.85 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at the active segment length of 2 μm and decreased to 62.99 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at the active segment length of 6 μm (Fig. 4(f)). For on-current per width, it was 9.86 $\mu A \cdot \mu m^{-1}$ at the active segment length of 2 μm and decreased to 6.79 $\mu A \cdot \mu m^{-1}$ at the active segment length of 6 μm. However, the good switching properties, including almost zero hysteresis and threshold voltage, and a high subthreshold swing of approximately 0.074 $V \cdot dec^{-1}$, remained unchanged irrespective of the active segment length (Table S1 in th ESM). Figure 4(g) shows the output characteristic curves of TS-TFTs with different active segment lengths. The linear relationship between the drain voltage and drain current at low drain voltages confirms good ohmic contact between the source/drain electrodes and the channel. Additionaly, as the active segment length decreased, the drain current in the saturation region increased. Based on these findings, we can infer that in the proposed TS-TFT structure, a shorter active segment length leads to superior electrical performance. The electrical properties of all PS-TFTs and TS-TFTs with different IZO semiconductor layer dimensions are summarized in Table S1 in the ESM.

3.5 Scalability for large-area production

To examine the scalability of the proposed method for large-area production, we fabricated TS-TFTs with a 40-nm-thick amplifier segment and a 10-nm-thick, 2-μm-long active segment on a 4-inch glass wafer coated with a 150-nm-thick indium-tin-oxide layer. As shown in Fig. 5(a), the wafer was divided into 16 regions, and a single TS-TFT from each region was selected to measure and compare their electrical properties. Figures 5(b) and 5(c) compare the transfer curves of all 16 TS-TFTs with the gate voltage sweeping from −5 to 5 V at V_{DS} = 4.1 V. The transfer curves merged into a single curve, indicating consistent electrical performance across all 16 TS-TFTs. Statistical analysis further supports this, showing small variations in measured electrical properties: a field-effect mobility of 87.84 ± 1.35 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (Fig. 5(d)), a hysteresis of 0.04 ± 0.05 V (Fig. 5(e)), near-zero threshold voltage, and a subthreshold swing of 0.074 ± 0.002 $V \cdot dec^{-1}$ (Fig. 5(f)). These results clearly demonstrate that the proposed TS-TFT structural architecture and the

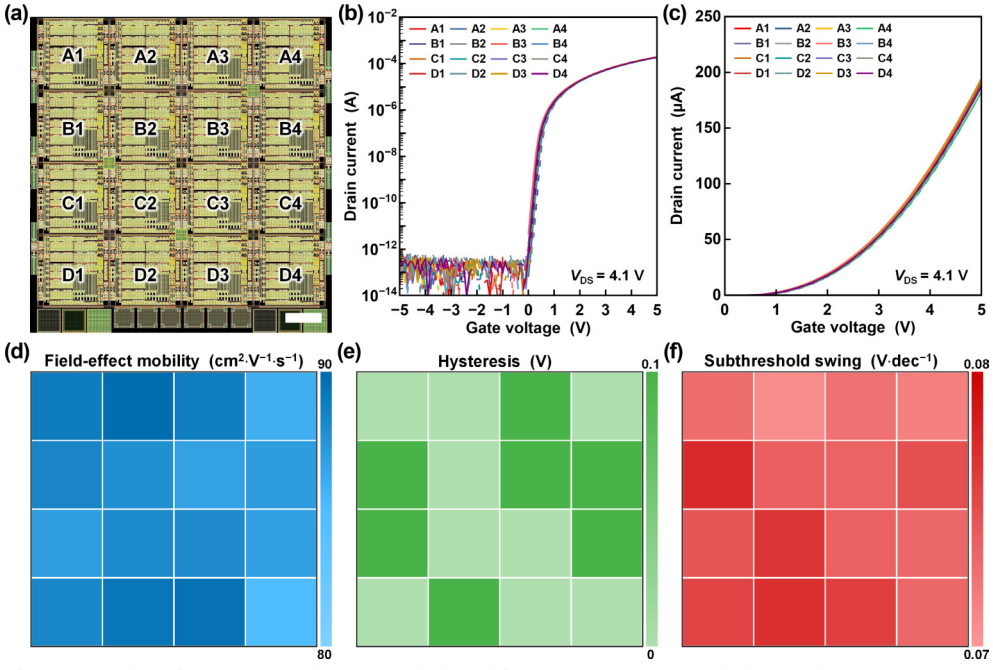

Figure 5 Electrical performance analysis of 16 TS-TFTs with a 40-nm-thick amplifier segment and a 10-nm-thick, 2-μm-long active segment, fabricated on a 4-inch wafer, after annealing at 270 °C for 2 h, followed by annealing at 300 °C for 2 h. (a) Locations of the 16 selected TS-TFTs on the 4-inch wafer (scale bar: 1 cm). Comparison of the transfer curves at V_{DS} = 4.1 V for the 16 TS-TFTs, plotted with (b) a logarithmic *y*-axis and (c) a linear *y*-axis, where the solid and dashed lines represent forward and reverse sweeps, respectively. Distributions of (d) field-effect mobility, (e) hysteresis, and (f) subthreshold swing values across the 4-inch wafer.

corresponding fabrication method are viable for wafer-scale large-area production.

4 Conclusions

In this study, we developed a novel TS-TFT architecture featuring a micropatterned double-layer oxide semiconductor of varying thickness and a corresponding fabrication process to address the shortcomings, such as inferior electrical performance and poor scalability for large-area production, identified in conventional PS-TFTs and previous TS-TFTs. Our approach forms a trench structure on a substrate by micropatterning the first oxide semiconductor layer deposited on the substrate, followed by the deposition of the second oxide layer using a PEALD supercycle method. This introduces a trench-structured oxide semiconductor layer with a thin active segment and thick amplifier segments between source and drain electrodes. This TFT architecture combined with the fabrication process allowed for an accurate dimensional control of the oxide semiconductor layer, facilitating an optimized TS-TFT structural design and ensuring dimensional uniformity over the large area. Our results showed that the active segment and the amplifier segment in the trench-structured oxide semiconductor layer played distinct roles in the electrical properties of the developed TS-TFTs. The active segment controlled switching properties (hysteresis, threshold voltage, and subthreshold swing), whereas the amplifier segment dominated current-driving capabilities (field-effect mobility and on-current per width). Therefore, the combined operation of these two mechanisms enabled the TS-TFTs to achieve the desirable feature of both good switching properties and high current-driving capabilities. The electrical performance analysis of 16 TS-TFTs fabricated on a 4-inch wafer demonstrated that the transfer curves and electrical properties calculated from them were almost coincident among all 16 TS-TFTs, indicating feasibility for large-area production and scalability for wafer-scale production. We believe that the superior electrical performance and wafer-scale producibility of the developed TS-TFTs open up possibilities for their potential use in high-performance electronic devices and large-area displays.

Electronic Supplementary Material: Supplementary material (mask layout design of the TS-TFT, optical microscope image of the TS-TFT, fabrication workflow of the trench structure, electrical characterization of the Al_2O_3 gate insulator, experimental setup for measuring electrical properties, comparison of the transfer curve between the PS-TFT and the conductor, effects of hydrogen annealing on electrical properties, and a summary of the electrical properties of all TFTs) is available in the online version of this article at https://doi.org/10.26599/NR.2025.94907065.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the ESM. Additional data related to this paper may be requested from the corresponding author upon request.

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Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

M. K.: Conceptualization, investigation, experimental design, data curation, validation, writing – original draft. J. C. B.: Investigation, formal analysis, writing – review & editing. D. K.: Investigation, validation, writing – review & editing. R. S. S.: Investigation, formal analysis, writing – review & editing. P. N.: Investigation, visualization, writing – review & editing. M.-S. K.: Funding acquisition, validation, writing – review & editing. S.-G. H.: Conceptualization, project administration, supervision, writing – review & editing.

Use of AI statement

None.

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