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Three-layer stacked PCB design of a low-voltage high-current inverter for motorsport applications

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ABSTRACT

Motorsport applications demand highly efficient, compact, and reliable power conversion systems capable of withstanding extreme dynamic conditions. This study focuses on the design and evaluation of a custom inverter tailored for a race electric motorcycle, with the objective of optimizing performance, thermal behavior, and component reliability under mission-specific constraints. The hardware design process involved selecting suitable power devices, optimizing printed circuit board (PCB) layout for minimal parasitics, and integrating a compact cooling solution. A detailed thermal model was developed to predict temperature profiles under typical racing conditions. Additionally, a reliability assessment was conducted based on real mission profiles, with lifetime estimations performed for metal-oxide-semiconductor field-effect transistors (MOSFETs) using stress data extracted from simulations. The results show that by aligning the inverter design with the actual usage profile, it is possible to significantly reduce the overall system size and cost while maintaining the required performance and ensuring component lifetimes compatible with racing demands.

KEYWORDS

Inverter; Two-level voltage source inverter; PCB design; MOSFET; DC-bus; Thermal design; Reliability

Nowadays, traction applications require extremely high power density conversion units. The great challenge in automotive applications consists of finding the best compromise between cost, volume and efficiency. This task is often addressed by developing segmented traction inverters, which can achieve over 99.2% efficiency but represent a highly effective, though technologically complex, solution that does not meet the cost constraints of most applications[1]. Mikhaylov et al.[2] noted that most applications favor modules optimized for heat transfer; however, they also demonstrated that discrete components can, under certain conditions, offer even better thermal performance, in addition to bringing considerable flexibility wwhen paired with a well-designed printed circuit board (PCB) layout. For the application discussed in this work, this flexibility is essential: modules are not a viable option, since the large number of parallel devices required by the target current rating cannot be accomodated within a standard module package. A notable alternative based on discrete devices is proposed by Bucher et al.[3], where six silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are paralleled to meet demanding voltage and current requirements. While effective, the SiC-based solution remains prohibitively expensive for a low-voltage application such as the one considered in this work. Given a maximum voltage of 126 V and a maximum current of 900 A_{rms}, a high number of parallel silicon (Si) MOSFETs was therefore identified as the most suitable solution. The choice is further supported by Peng et al.[4] who reported a lifetime improvement when using traditional Si devices under certain load conditions. An alternative to Si power MOSFETs in low-voltage, high-current applications is represented by gallium nitride (GaN) semiconductors. The extremely high switching frequencies achievable, together with the low drain-source on resistance $R_{DS,on}$ of these devices, make them very promising. However, the technology has three big limitations at the moment: high-cost of the single die or discrete component, reliability issues and very few investigations on the lifetime. Lu et al.[5] studied the power losses distribution among paralleled GaN high electron mobility transistors (HEMTs) and Huang et al.[6] proposed a remarkable lifetime model based on the saturated $R_{DS,on}$ of the transistor. Both studies have shown that voltage stress leads to a mismatch in $R_{DS,on}$ variation among the devices, resulting in an unbalanced, and indeed irreversible, current sharing. This mismatch makes the paralleling of GaN devices particularly challenging, further limiting their suitability for the high-current configuration required in this application. Due to the requirements on rating, costs and lifetime of the application, in this work a parallel connection of Si MOSFETs was chosen. A complete design of a low-voltage high-current inverter with ten parallel Si MOSFETs has been designed and a detailed lifetime assessment that converged to a certain number of parallels was carried out. After a brief description of the application requirements in Section 1, the electrical design and the thermal design of the heatsink are explained in detail in Sections 2 and 3, respectively. The design ends with the mechanical considerations of Section 4, mainly regarding the employment of the bus bars. Then, an accurate lifetime assessment is carried out in Section 5 following the mission profile based methodology presented in Ref. [7]. However a revised version of the CIPS2008 model[8] has been employed, that is more suitable to the type of transistor used. This model belongs to the physics-of-failure (PoF) family of reliability models, which characterizes component degradation as a function of one or more governing stress or damage variables. Consistent with this approach, Kovacevic et al.[9] and Drofenik et al.[10] also adopted PoF formulations, identifying the solder interconnection as the dominant failure mechanism and weakest link in the system. PoF models represent only one methodological category within reliability prediction; data-driven and hybrid approaches constitute alternative frameworks[11]. However, these

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latter methods are characterized by substantially higher uncertainty margins compared to PoF-based models, which motivates the modeling approach adopted in this work. Both MATLAB and PLECS software are employed for the lifetime estimation in this work, and an open-source solution was used[12]. Finally, conclusions are drawn on the inverter design and lifetime estimation in Section 7, which can be easily transferred to similar applications. Novelties of this work lie in:

- Reliability analysis of a low-voltage, high-current inverter. The most important studies on reliability, which have been cited in this work, addressed high-voltage inverters of two or more levels and mainly for renewable applications. Studies on automotive inverters employing parallel power devices are rarely reported in the literature. This paper addresses this gap by presenting a comparative analysis that quantifies the expected lifetime as a function of the number of parallel devices and the load conditions. These results demonstrate that the proposed method is effective in supporting designers in selecting the appropriate number of parallel devices according to the converter's target specifications and application requirements.
- Reliability analysis based on a recent and accurate switching losses model for the transistors. Most of the works on this subject, as this work, do not include experimental results as they would require a notable financial expense and a significant amount of prototypes. However, the reliability analyses reported in the literature typically rely on switching loss curves derived directly from manufacturer datasheets. Such curves may be incomplete or unavailable, as is the case for the switch selected in this work, which necessitates the use of an alternative approach. Accordingly, the model presented in Ref. [13] is employed to generate the switching loss curves required for thermal simulation and junction temperature estimation.

1 Application requirements

The designed inverter is intended to be used in a racing electric motorcycle taking part to the MotoStudent competition. MotoStudent is an advanced educational program that prepares undergraduate and graduate students in various fields related to the mobility sector. It focuses on promoting future innovation leaders by challenging them with a real motorsport project. The projects and prototypes presented will be judged and assessed in a series of different tests, divided into two different phases, called MS1 and MS2. The MS1 phase primarily evaluates teams' engineering and management skills, focusing on creative problem-solving rather than relying on available resources. This phase provides students with an opportunity to apply their academic knowledge in a practical, professional setting. It showcases the challenges and procedures involved in real-world project development, from the initial concept to its completion. As an engineering competition, MotoStudent places significant emphasis on design choices, with the MS1 phase constituting half of the total score. Technical solutions are evaluated through a comprehensive technical documentation that describes the design of each component of the prototype. The MotoStudent competition provides all teams with a MotoStudent kit, including tires, brakes, an insulation monitoring device (IMD), and the electric motor (i.e CIRCE MS2425). All other components of the prototype can either be designed and manufactured by the team members or purchased from third-party suppliers meeting some technical requirements, such as the maximum voltage of the battery pack 126 V and both a nominal and a maximum root mean square (RMS) phase current, which depends on the electric motor. Notably, custom-designed components allow teams to earn a higher score in the MS1 phase. The MS2 phase consists of a series of tests aimed at assessing the dynamic behavior and performance of the manufactured prototype. The MS2 phase is segmented into several sub-parts: acceleration, gymkhana, braking and a standard race weekend including a free practice session, a qualifying session, and the race itself consisting of 6 laps of the Motorland of Aragon circuit shown in Figure 1. As a result, different power maps must be developed and tailored to each stage, in order to precisely control power delivery and regenerative braking. In particular in the acceleration stage, the prototype have to run for 150 m in the shortest time possible; this requires the highest amount of torque and power, overloading both the motor and the inverter. Inverter ratings have been defined and resumed in Table 1, based on motor operating limits in Table 2.

It is possible to note that the maximum rating of the inverter is much higher than the motor one. The reason for this is that the converter is the first prototype, and it must also accommodate certain testbench activities that demand higher current levels. As a result, the converter has been intentionally oversized relative to the motor's electrical limits to ensure adequate performance and flexibility during testing. This approach allows for thorough evaluation under various operating conditions and helps identify potential issues early in the development process. In Section 2, the electrical design of the inverter is presented, based on the requirements defined in this section.

2 Electrical design

Given the motor operating limits presented in Section 1 and due to the limited available voltage, achieving high power output means delivering a significantly high current to the motor. Consequently, to ensure high performance of the motorcycle we designed an efficient and robust inverter and control logic, capable of handling these elevated current levels. However, managing high currents presents significant challenges, especially in terms of thermal management, efficiency, and system reliability. To address

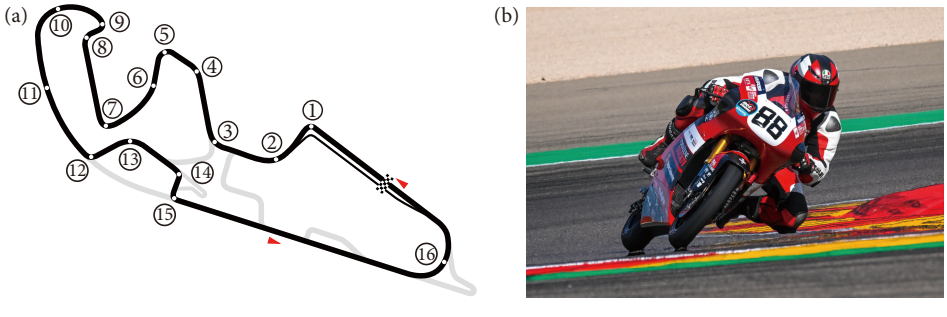


Figure 1 **(a)** Motorland of Aragon race track, and **(b)** UniBo Motorsport prototype during the 2023 Motostudent edition.

Table 1 Inverter design parameters

Parameter	Symbol	Value	Unit
Nominal voltage	V_{nom}	126	V
Nominal RMS phase current	I_{nom}	450	A_{rms}
Max RMS phase current (2 min)	I_{max}	900	A_{rms}

Table 2 Electric motor CIRCE MS2425 parameters

Parameter	Symbol	Value	Unit
Nominal torque	T_{nom}	50	Nm
Nominal power	P_{nom}	22	kW
Nominal RMS phase current	I_{nom}	250	A_{rms}
Max torque	T_{max}	120	Nm
Max power	P_{max}	48	kW
Max RMS phase current	I_{max}	600	A_{rms}
Pole pairs	PP	5	/

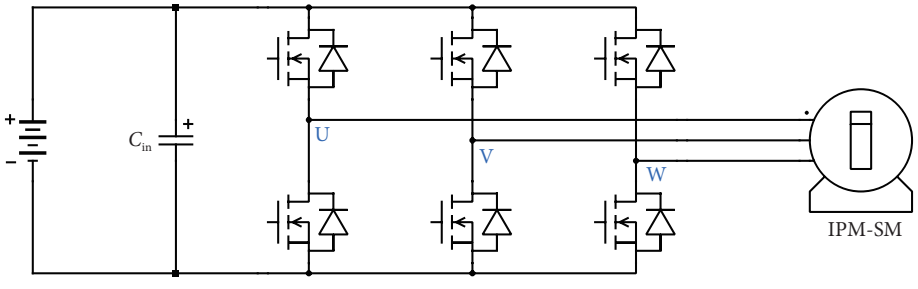


Figure 2 Three-phase two-level inverter topology schematic connected to a internal permanent magnet synchronous motor (IPM-SM).

switching components. When combined with the necessity for parallelization to reach the desired power levels, this results in a converter that is excessively large, heavy, and complex. Such a design would not only increase costs but also reduce the overall feasibility of the system for a high-performance motorcycle.

The design involves a three-layer stacked PCB. The base comprises the power insulated metal substrate (IMS) PCB, housing the switching devices forming the three legs of the inverter shown in Figure 2. In the middle of the stack, the power DC-link board is placed and it is almost entirely dedicated to the set of DC-bus capacitors represented by the C_{in} capacitor in Figure 2. Those capacitors are placed between the battery and the power rails of the inverter to help to ensure a stable voltage level by compensating for fluctuations caused by load variations and switching events in the power circuit. The third PCB contains the logic and driver circuitry. Each of the following subsection is dedicated to one PCB, briefly describing their features.

2.1 IMS-based power PCB with thermal and electrical safeguards

The power PCB uses IMS technology, which consists of metal plate, typically aluminum, interposed through a thermally conductive dielectric to the copper layer. IMS based PCBs offer superior heat dissipation compared with traditional FR-4 boards, which is essential due to the high currents flowing through the power devices. Only a ceramic PCB would allow lower thermal resistance and capacitance, but it is not suitable for this application, because of its fragility. The compliance with the international electrotechnical commission (IEC) standards regarding the electromagnetic interference (EMI) and electromagnetic compatibility (EMC) of the designed inverter has not been investigated in this work. It was experimentally proved in Ref. [14] that the parasitic coupling between the copper foil and the IMS base plate provokes higher EMI. The authors of the work highlighted the importance of common-mode filter optimization, placed between the power DC supply and the DC-bus. Skibinski et al.[15] provided a general reference on the EMI standards for AC motor drives and Zhao et al.[16] proposed a detailed AC filter design for EMI suppression in demanding applications, such as aircraft propulsion. However it is worth noting that due to the low DC bus voltage 126 V, the dV_{DS}/dt issues are inherently mitigated by the application.

The converter must handle peak and continuous RMS currents of 900 and 450 A_{rms}, respectively. Therefore, a proper selection of the power device started by choosing the package: D_2PAK-7 was selected for its excellent thermal performance. The drain-source voltage, V_{DS}, rating must also account for potential ringing, leading to a required minimum V_{DS} rating of 200 V, despite the DC supply being 126 V. Given the need for device paralleling, only MOSFETs were suitable, as insulated gate bipolar transistors (IGBTs) pose greater challenges in achieving even current distribution and offer fewer benefits in reducing conduction losses when paralleled. After those considerations, the Infineon IPF067N20NM6 MOSFET was determined to be the most suitable device for this application. Given the rating of this device, resumed in Table 3, and the requirement on the maximum phase current of the converter, it

Table 3 IPF067N20NM6 MOSFET ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	200	V
Continuous drain current at T_j = 25 °C	I_D	138	A
Maximum drain-source on resistance	$R_{DS,on,max}$	6.7	mΩ

has been chosen to use 10 MOSFETs in parallel as shown in Figure 3.

To ensure reliable operation, specific components are integrated into the gate drive circuitry: pull-down resistors are essential to ensure the discharge of the gate-drain capacitance C_{GD} and prevents accidental turn-on caused by noise or capacitive coupling at high dV_{DS}/dt; each MOSFET is equipped with its own gate resistor (R_{G1}–R_{G10}) to ensure an even distribution of the gate drive current; moreover additional gate source capacitors are added to provide a low-impedance path that helps to keep V_{GS} close to the off-state level, preventing spurious turn-on.

Based on past experience, such high current demands generated high-frequency parasitic oscillations, therefore, in this design a ferrite bead in combination with a resistor on each gate was added to mitigate this effect[17]. Ferrite beads are particularly effective because their impedance increases with frequency, suppressing noise and minimizing the risk of accidental turn-on of the devices. Finally, anti-series zener diodes (D_1 and D_2) are connected between the gate and source to clamp both positive and negative excursions of the gate-source voltage V_{GS}, protecting the gate of the MOSFET from over-voltage stress both on turn-on and turn-off phases clamping the voltage at ±18 V. To achieve stable operation, MOSFETs must be placed symmetrically to minimize parasitic inductance and ensure balanced current sharing as shown in Figure 4. Poor layout can lead to uneven current distribution, increased stress, and potential device failure due to thermal imbalances. The PCB in Figure 4 features two pads, highlighted in red, dedicated to the $+V_{DC}$ connection, while the two black squared copper pads are assigned to power-ground (PGND). These two $+V_{DC}$ and two PGND rails are respectively interconnected via the DC-link board and the power busbars, ensuring stable power distribution across the system. The blue highlighted pads, on the other hand, correspond to the three output phases U, V, and W. Finally, at the bottom of the board, a signal connector is present to receive gate drive signals from the logic board, enabling the control of the power devices.

2.2 DC-bus capacitance selection and PCB design

DC-bus capacitors play a crucial role in power electronics by stabilizing the DC-link voltage, filtering high-frequency noise, and providing the necessary energy storage to support fast switching transients. These capacitors help maintain a steady voltage level by compensating for fluctuations caused by load variations and switching events in the power circuit. In applications such as motor drives, inverters, and power supplies, DC-bus capacitors reduce voltage ripple and suppress EMI, electro-magnetic inter-

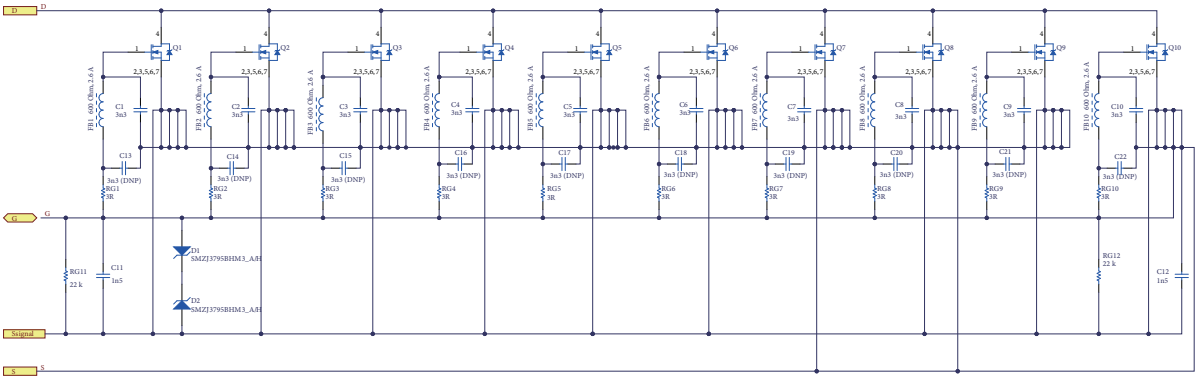


Figure 3 Parallel MOSFETs schematic.

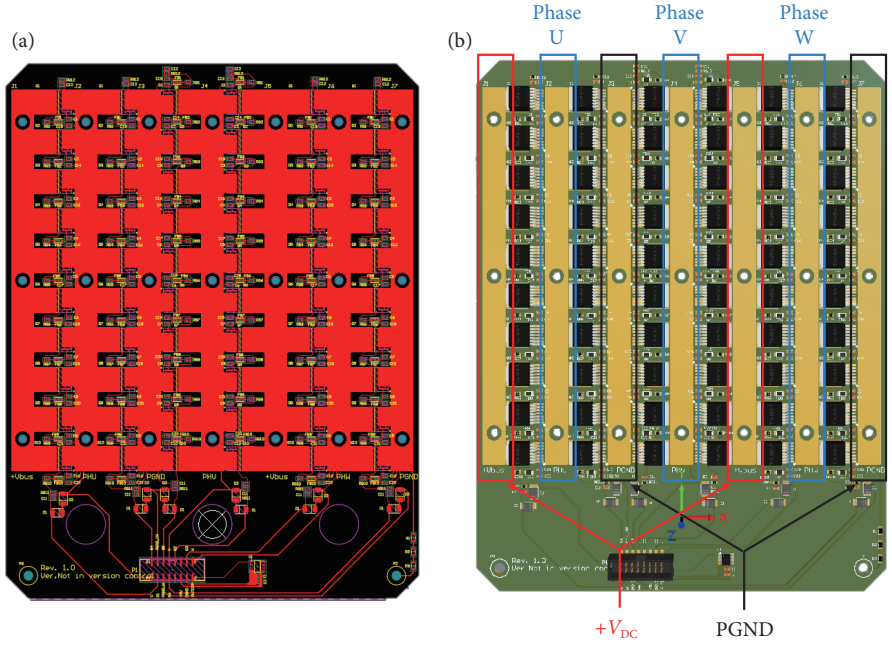


Figure 4 Power board layout. (a) 2D power PCB layout, and **(b)** 3D power PCB layout with the phases and DC-bus connections highlighted.

ference, ensuring efficient and reliable operation. Proper selection and placement of these capacitors are essential to minimize parasitic inductance and resistance, which can otherwise lead to excessive voltage spikes, increased losses, and potential damage to power semiconductors. Using a combination of ceramic and electrolytic capacitors in a DC-link capacitor board for a traction inverter is essential to achieve optimal performance in terms of stability, ripple reduction, transient response, and reliability. Each type of capacitor serves a specific purpose, complementing the limitations of the other. Ceramic capacitors are highly effective at filtering high-frequency switching noise and transient voltage spikes due to their low equivalent series resistance (ESR) and low equivalent series inductance (ESL). Thus, they help prevent overheating of the electrolytic capacitors, ensuring stable voltage levels during rapid load changes. In addition, ceramic capacitors offer excellent temperature stability and durability, making them highly reliable components in demanding automotive applications. However, electrolytic capacitors provide the bulk energy storage needed to maintain a stable DC-link voltage under dynamic load conditions. They effectively handle low-frequency ripple currents generated by inverter operation, preventing voltage drop and ensuring continuous power delivery. With their high capacitance values, electrolytic capacitors are a cost-effective solution for energy buffering, although they are characterized by higher ESR and ESL compared with ceramics. Combining both types of capacitors leverages their complementary frequency responses. Electrolytic capacitors handle low-frequency ripple and energy storage, while ceramic capacitors excel at high-frequency noise suppression and transient response. This integration improves system efficiency, reduces EMI, and enhances overall stability. Experimental power factor (PF) data, measured for phase currents ranging from 250 to 660 A_{rms}, are shown in Figure 5(a); these results show that the power factor reaches its minimum value of about 0.6, which was therefore adopted as the worst-case condition for the ripple analysis. Taking the analytical design process proposed in Ref. [18] as a reference, the required capacitance that would guarantee a maximum voltage ripple on the DC-bus ($\Delta V_{pp,max}$) can be estimated through Eq. (1):

$$C \geqslant \frac{I_o}{f_{sw}} \frac{r_{pp,max}}{\Delta V_{pp,max}} = 8.58\ (\text{mF}) \tag{1}$$

where f_{sw} is the switching frequency, $I_o = 1269$ A is the phase current amplitude and $r_{pp,max}$ is the maximum value of the normalized peak-to-peak voltage ripple amplitude in Figure 5(b) that corresponds to the worst-case condition.

$\Delta V_{pp,max}$ is the maximum voltage ripple allowed; it is a design parameter that has been set to 2% of V_{DC} for this application. Concerning the PCB design, bulk electrolytic capacitors are distributed across the entire board to ensure that the DC-bus power-line uniformly experiences the stabilizing effect of the input DC-link capacitors. To reduce the stress on the electrolytic capacitors,

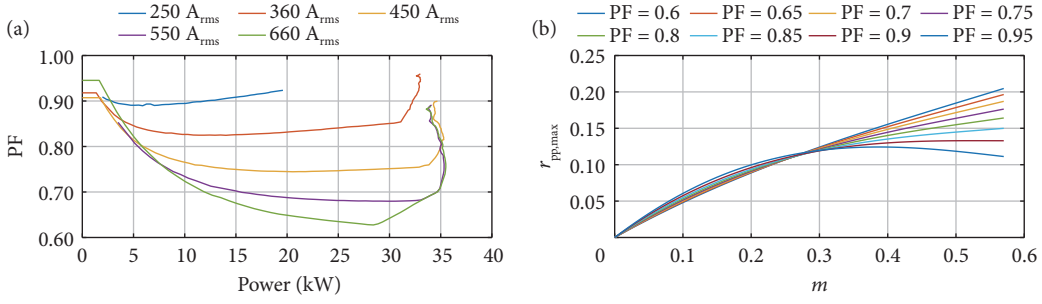


Figure 5 **(a)** Experimental power factor (PF) data vs output power, and **(b)** maximum normalized peak-to-peak voltage ripple amplitude $r_{pp,max}$ vs modulation index m. The worst case matches with $m = 1/\sqrt{3}$ and PF = 0.6.

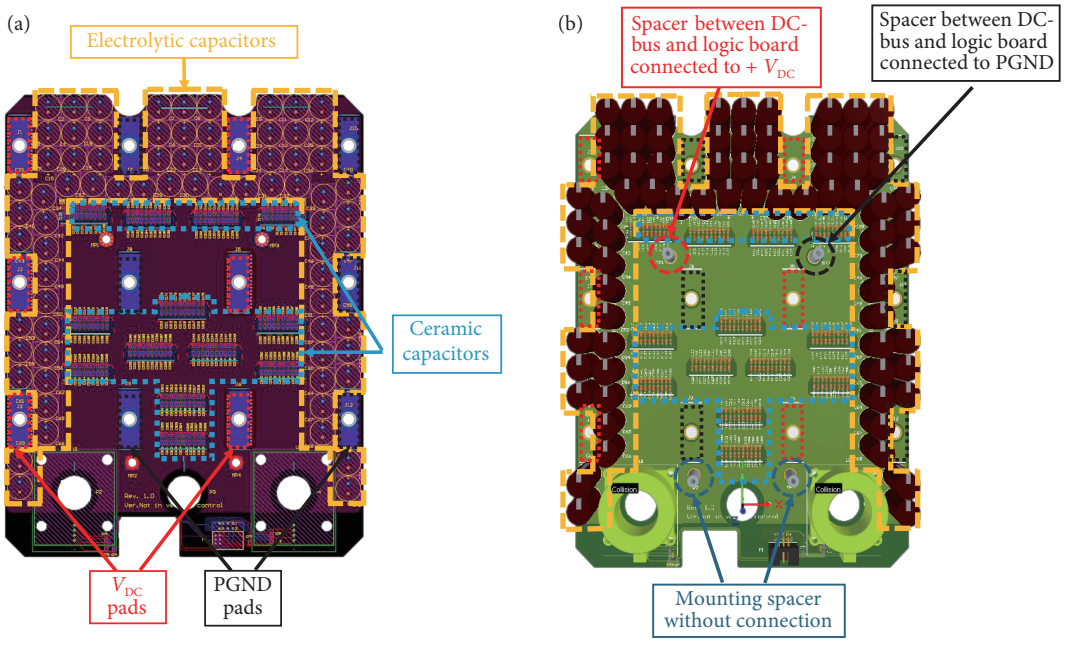


Figure 6 **DC-link capacitor board.** **(a)** PCB 2D view, and **(b)** PCB 3D view.

ceramic capacitors were added to leverage the beneficial effects discussed at the beginning of the Section 2.2. This PCB consists of two layers: the top layer is completely dedicated to $+V_{DC}$, while the bottom layer is assigned to power-ground. This design facilitates easy connections to the capacitor terminals and minimizes resistance in the current path. The blue pads on the bottom side visible in Figure 6(a) are necessary to establish a power connection between the DC-bus PCB and the power IMS PCB through the DC-bus bar. Additionally, four spacers, highlighted in Figure 6(b), are included to mount the logic and driver board. Two of them are connected to the two power polygons, enabling bus voltage measurement and the pre-charge of the DC-link.

2.3 Driver and control

The logic and driver board is densely populated with components and thus the most challenging to design because of the limited space available. For safety reasons and for noise rejection, the board is divided into two parts to fully isolate the high-voltage (HV) system from the low-voltage (LV) system through isolated DC-DC converters for the power supply and opto-couplers for the signals. For this application for HV, it is intended any circuit with a potential difference over 60 V and any other circuit working at a voltage lower than that threshold is considered LV. The HV side performs the pre-charge of the DC-link capacitors through the inverters turn on signal, called key-in, and generates the main isolated supply of the LV part. The LV side performs several crucial functions: it generates the various power supply levels required by the logic-level components, houses an micro-controller unit (MCU) that creates gate signals based on sensed current, generates the isolated supply voltages of the gate drivers, and contains the six gate driver circuits. It also provides input/output connectivity and acquires sensor data for converter control and operational monitoring. Table 4 resumes all the tasks performed by the logic board. Sections 2.3.1 and 2.3.2 provide a detailed explanation of the main schematics and how it contributes to the functions described above.

2.3.1 Gate driver isolated supply

Four isolated power supplies are generated for the six gate drivers of the inverter: three are dedicated to the high-side MOSFETs and one to the low-side MOSFETs. This configuration ensures proper gate drive voltage levels, minimizes noise interference and provides reliable switching performance in the power circuit. The gate drive circuit must be carefully designed to handle the increased gate charge and capacitance associated with the paralleling of multiple MOSFETs. When multiple MOSFETs are connected in parallel, the total gate capacitance increases, requiring higher drive current to achieve fast switching times. If not properly managed, this can lead to excessive power dissipation in the gate driver, reduced efficiency, and potential thermal issues. To mitigate these challenges, the gate driver should be capable of delivering sufficient peak current to charge and discharge the MOSFET gates quickly. Additionally, selecting gate resistors with appropriate values helps control switching speed, minimizing voltage overshoot and ringing. Proper layout techniques, such as minimizing trace inductance and ensuring tight coupling between the gate and the source, further enhance performance and reduce EMI. For the generation of the gate driver power supply, the L6986I integrated circuit was selected. The L6986I is a 38 V, 5 W synchronous isolated buck (iso-buck) by STMicroelectronics. One of its key advantages is the ability to generate an isolated secondary output using a transformer, without the need of an opto-coupler for the feedback signal. This simplifies the design complexity and reduces the number of required components. Additionally, the L6986I includes a primary sink capability of up to 1.9 A, ensuring proper energy transfer to the secondary side while supporting a tracked soft-start of the secondary output.The L6986I module takes a 24 V input and converts it to a 5.3 V output. The reference voltage at the feedback (FB) pin is typically 0.85 V. You can set the output voltage by adjusting the voltage divider using resistors R_{85} and R_{87}, according to the Eq. (2):

$$V_{\text{out,IsoBuck}} = 0.85\left(1+\frac{R_{85}}{R_{87}}\right) = 5.3\ (\text{V}). \tag{2}$$

Then considering that $V_{\text{out,IsoBuck}}$ is floating, the secondary side voltage can be calculated using a simplified equation:

$$V_{\text{out,sec}} = NV_{\text{out,IsoBuck}} - R_{\text{sec}}I_{\text{sec}} - V_{\text{F,D9}} \simeq 30\ (\text{V}), \tag{3}$$

where N is the turn ratio, R_{sec} is the resistance of the secondary side winding, I_{sec} is the secondary side current and $V_{\text{F,D9}}$ is the forward voltage of the flyback diode (D_9 in Figure 7). The transformer was selected according to the suggestions of the datasheet of the module; its characteristics are summarized in Table 5.

The circuitry after the transformer (see Figure 7), is used to generate the $+V_{\text{DRV}}$ and $-V_{\text{DRV}}$. On the upper part of the circuit, there is a simple linear voltage regulator composed of a NPN bipolar-junction-transistor (BJT) and an adjustable voltage reference (i.e., TL431). The TL431 is used to control the BJT in a linear voltage regulation region by acting as a precise voltage reference and feedback controller. It regulates the transistor's base current, adjusting its conduction to maintain a stable output voltage. The BJT operates in its linear region, acting as a pass element that provides current to the load. In this configuration, the TL431 continuously compares the output voltage with its internal 2.5 V reference and adjusts the cathode current accordingly. A voltage divider composed of R_{91} and R_{93} (see Figure 7) sets the desired output voltage according to Eq. (4):

$$V_{\text{TL431}} = V_{\text{ref}}\left(1+\frac{R_{91}}{R_{93}}\right) \simeq 18\ (\text{V}), \tag{4}$$

where V_{ref} is 2.5 V. TL431 modulates the base current of the transistor, through a bias resistor, ensuring stable operation even under varying load conditions. This design allows for higher current handling since the BJT amplifies current, while the TL431 ensures precise voltage regulation. The negative rail of the gate driver supply is instead generated by the zener diode, which has a zener voltage of 4.5 V.

To verify the behavior of the gate driver supply circuit, a simulation is performed using eDSim software (see Figure 8); a simulation tool developed by STMicroelectronics for power electronics and analog circuit design, utilizing components from the same manufacturer. In the simulation, the ten transistors are represented by an equivalent resistor-capacitor (RC) circuit, which is the

Table 4 Logic and driver board tasks

Feature	Description		
Power supply	+3.3 V	+5 V	+24 V
I/O connectivity	CAN	UART	USB
Sensed signal	DC-bus voltage	Key-in voltage	Current sensor
Supported peripheral	Sin/Cos encoder	SSI encoder	PT1000
Gate driver circuitry	Four dual isolated DC/DC	Six isolated gate drivers	

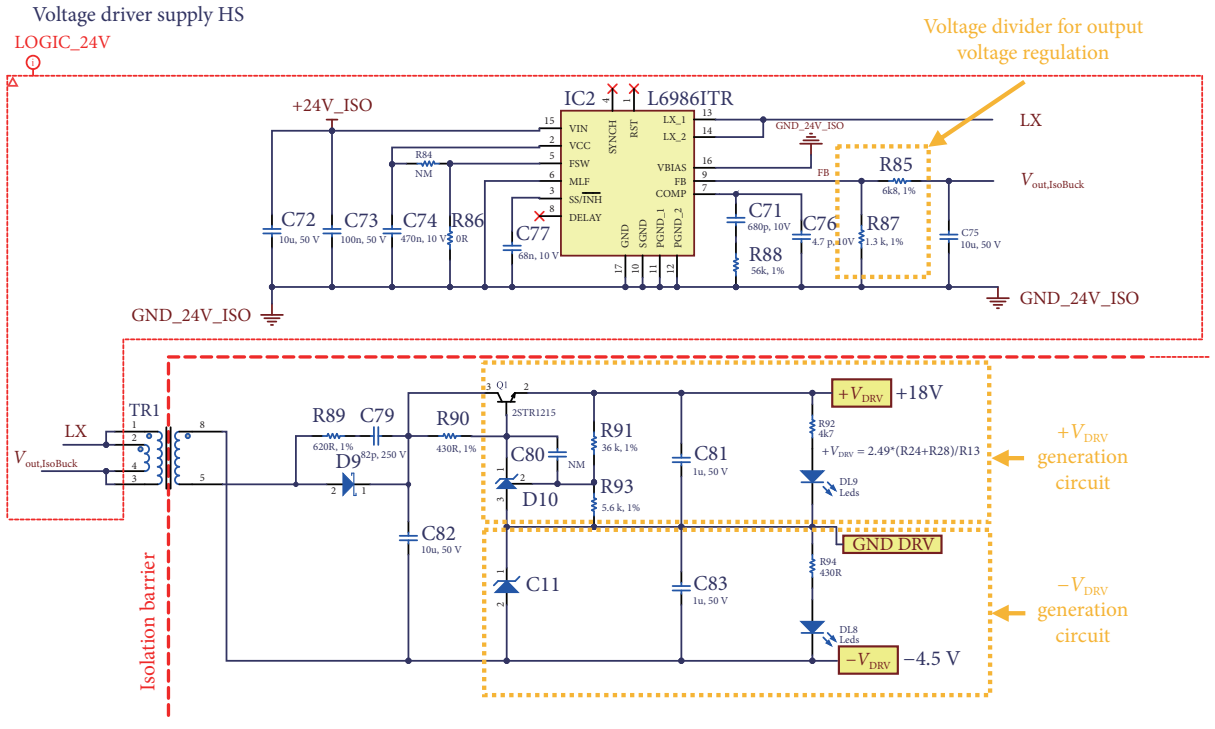


Figure 7 Iso-buck L6986I: in the upper part of the schematic the voltage divider required to control the output voltage is highlighted; on the bottom side the dual isolated supply +18 V and −4.5 V circuit generation is shown.

Table 5 Coilcraft ZA9668-AE characteristics

Parameter	Symbol	Value	Unit
Input voltage	V_{in}	5	V
Output voltage	$V_{out,sec}$	29	V
Power	P	5.8	W
Switching frequency	f_{sw}	500	kHz
Inductance at 0 A	L	18	μH
Saturation current	I_{sat}	3.5	A
Primary DC resistance max	R_{prim}	0.075	Ω
Secondary DC resistance max	R_{sec}	1.49	Ω
Leakage inductance	L_1	0.24	μH
Turn ratio	N	5.8	/

equivalent circuit seen by the gate driver supply. External ceramic capacitors are included in the simulation because they provide the peak gate current as will be explained in Section 3.3.2. Analyzing the waveforms in Figure 9 reveals that the gate current (I_{gate}) displays a pronounced initial peak, which is constrained by the total gate resistance. Following this peak, the current gradually decreases as the equivalent gate capacitor charges. As desired, the peak current is entirely supplied by the bypass capacitors, while the L6986I module is responsible only for recharging them with the secondary-side output current I_{OUT2}. The secondary absorbs an average current of 54.3 mA, resulting in an average power consumption of 1.6 W, while the peak absorption is 4.14 W. Both results are within the specified limits of the components. Both $+V_{DRV}$ and $-V_{DRV}$ remain stable under load conditions with a measured ripple of 1% on the positive rail and 4% on the negative rail.

2.3.2 Gate driver circuit

The 1EDI60N12AF isolated gate driver has been selected for its

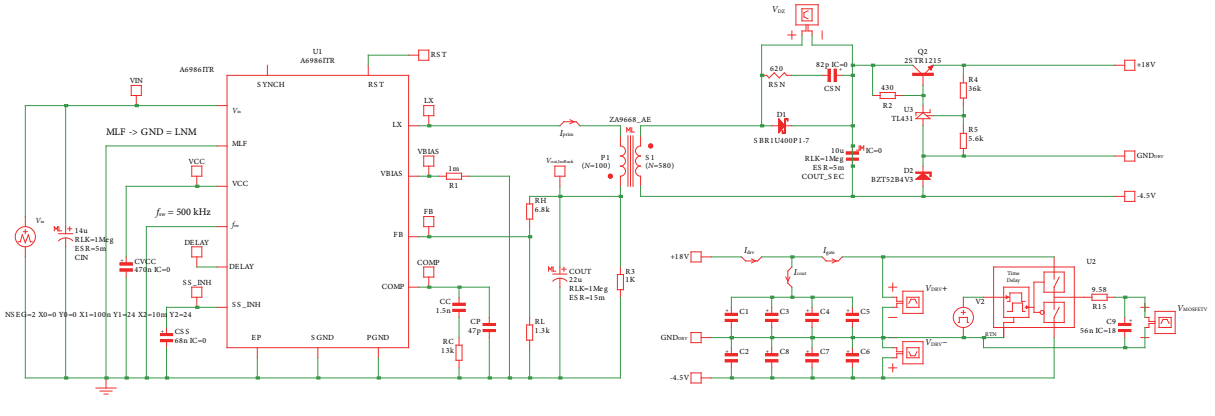


Figure 8 Isolated dual rail gate driver power supply simulation in ST-eDSim environment. On the bottom right corner it is shown the equivalent RC circuit modeling the series and parallels of the gate resistances and capacitances.

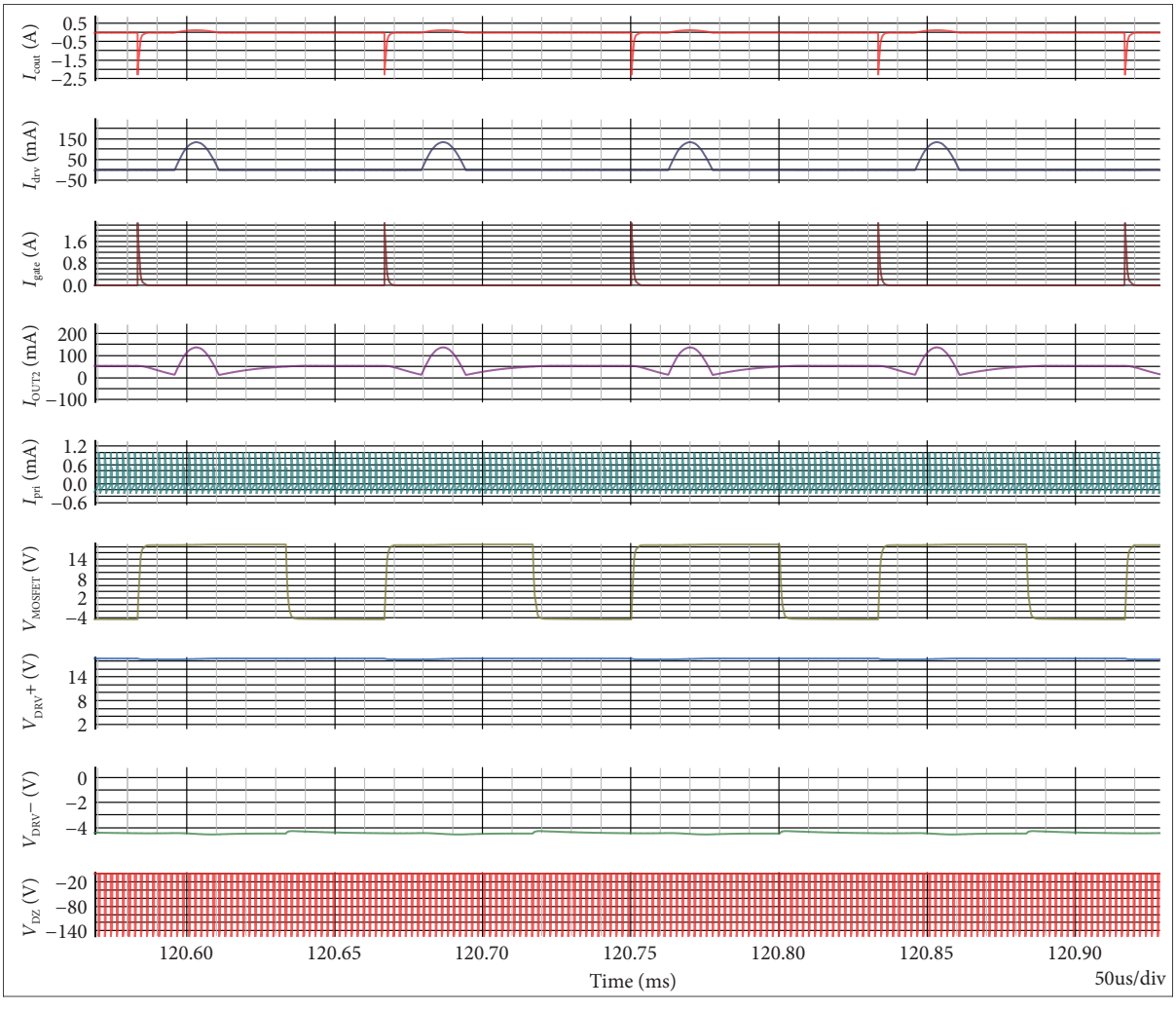


Figure 9 eDSim simulation results.

high-performance and fast and efficient switching of power MOSFETs and IGBTs in high-power applications. It provides an output peak current of 10 A, ensuring strong gate drive capability for rapid charging and discharging of the transistor's gate capacitance, which helps minimize switching losses and improve overall efficiency. One of the key advantages of the 1EDI60N12AF is its separate rail-to-rail driver outputs, which improve gate control flexibility. This feature simplifies gate resistor selection, allowing for fine-tuning of the switching speed to balance efficiency and EMI concerns. By offering better dV/dt control, the driver helps to mitigate voltage transients and enhances system reliability, particularly in environments with high switching frequencies and demanding electrical conditions. Figure 10 shows the gate driver circuit. Between $+V_{DRV}$ and GND_{DRV}, as well as between $-V_{DRV}$ and GND_{DRV}, a bank of capacitors was added to supply the peak gate current and stabilize the gate driver's power supply, as described in Section 2.3.1. These capacitors are crucial for delivering the high transient currents needed to rapidly charge and discharge the gate capacitance of power transistors, preventing voltage drops and minimizing supply fluctuations during fast switching transitions. This configuration ensures the gate driver operates within its optimal conditions, enhancing the overall reliability and efficiency of the system. So, the bypass capacitance C_{bypass} is selected using the relations in Eqs. (5) and (6), to limit the voltage drop ΔV_{DRV} at the input terminals of the gate driver.

$$\begin{cases} I_c = C_{bypass}\dfrac{dV_{DRV}}{dt} \\ \displaystyle\int_{t_{on}} I_c dt = Q_{G,tot} \end{cases} \Longrightarrow Q_{G,tot} = C_{bypass}\Delta V_{DRV}\,, \tag{5}$$

$$C_{bypass} > \frac{Q_{G,tot}}{\Delta V_{DRV}}\,. \tag{6}$$

where I_c is the bypass capacitor current and $Q_{G,tot}$ is the total charge stored in those capacitors.

2.3.3 *Logic and driver PCB*

In Figure 11 the logic and driver board is shown. On the top side, the board includes a DC-link capacitor pre-charge circuit that uses negative temperature coefficient (NTC) thermistors to safely charge the capacitors, activated via the key-in signal. The precharge current flows to the DC-bus board through the electrical connection provided by the spacers described in Section 2.2. The key-in signal is also used to power-up the isolated DC/DC converter responsible for generating the main power supply, alongside the four isolated DC/DC converter dedicated to powering the gate drivers. Finally, an external MCU is centrally located, managing control and communication functions. On the bottom side, the two spacers just described are highlighted. The center of the board hosts six gate drivers responsible and are placed exactly below the corresponding gate drive dual-supply to minimize the length of the tracks. More-

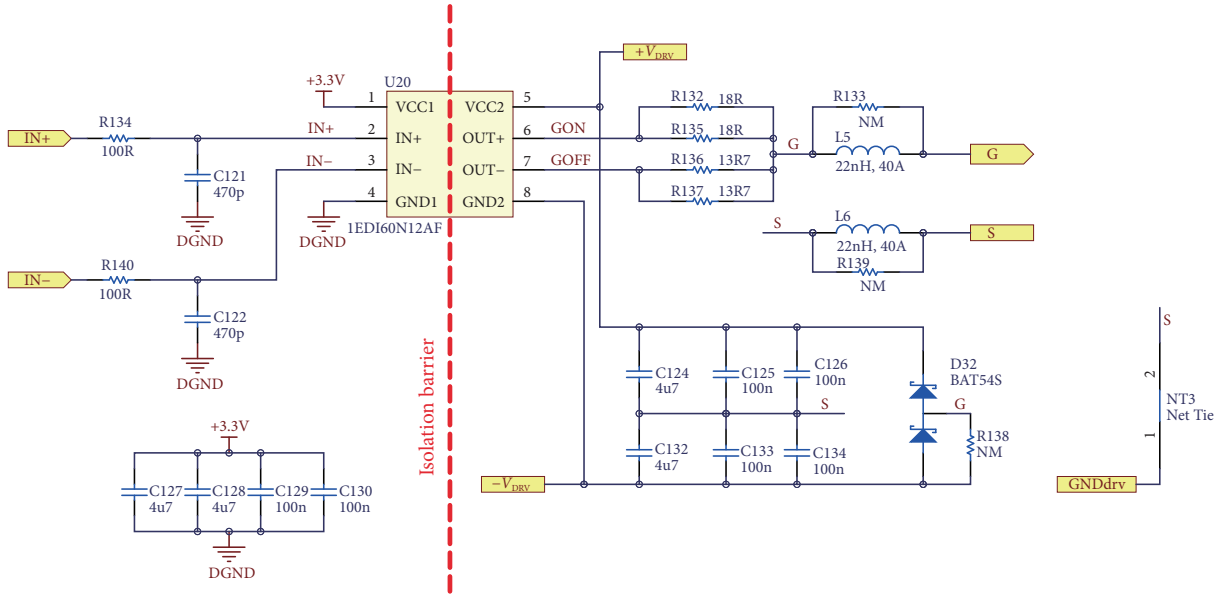


Figure 10 Gate driver circuit based on 1EDI60N12AF.

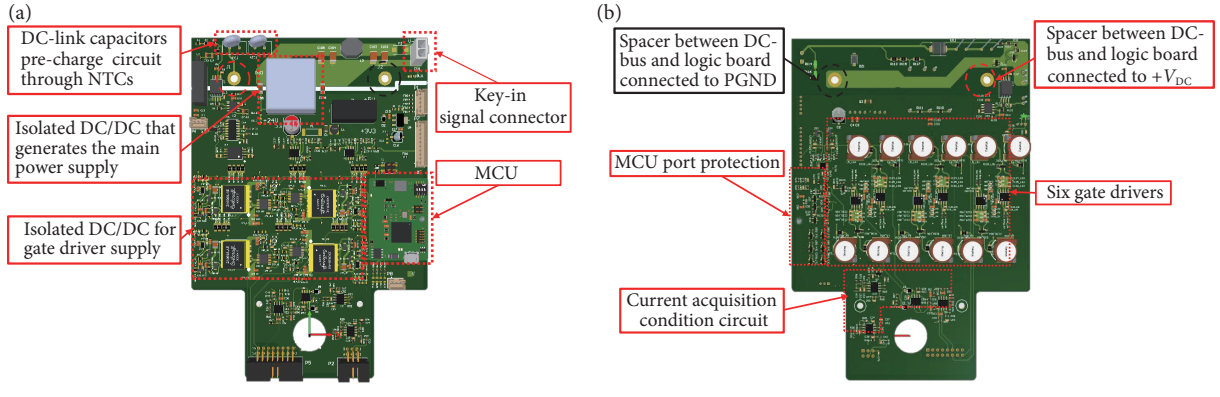


Figure 11 Logic and driver board. (a) Top view, and **(b)** bottom view.

over, additional circuitry is shown, including MCU port protection and a current acquisition conditioning circuit that filters and adapts the sensed signal for the analog to digital converter (ADC) inputs.

3 Thermal design

The aim of the thermal design is both the size of the heat sink and the evaluation of the parameters of the Cauer model for the whole system, which represents the first step in assessing the reliability of the inverter. In an overload condition, the current request can reach up to 900 A_{rms} from the inverter and could last up to 30 s. MOSFETs are the most critical components of the system and because Si technology is used, a maximum junction temperature of 150 °C should be allowed in this condition. The heat flow produced by the transistors should be taken out by the heat sink, that should be sized accordingly. Thus, a Cauer model must be built for the transistors, and the authors followed the method described in Refs. [7, 19, 20]. Throughout a MATLAB swarm curve-fitting of the junction to case impedance curve $Z_{th,j-c}$, it is possible to derive a Foster model of the junction to case thermal network. Foster model can be easily converted into a Cauer model.

$$Z_{th,j-c}(t) = \sum_{i}^{n} R_{th,i} \cdot (1 - e^{-t/\tau_i}), \quad (7)$$

where $R_{th,i}$ is the ith thermal impedance and τ_i is the corresponding thermal constant: both are found by fitting the curves in MATLAB. The ith thermal capacitance $C_{th,i}$ can be easily derived by applying:

$$C_{th,i} = \frac{\tau_i}{R_{th,i}}. \quad (8)$$

The results, already converted to the corresponding Cauer model, returned for the selected part number: MOSFET IPF067N20NM6[21] are shown in Table 6. The thermal resistance from the case to the heat sink was evaluated instead following the guideline in Ref. [22]. An IMS PCB was used for this design, whose bottleneck is the thermal conductivity of the substrate, represented by the thin dielectric substrate of 0.15 mm between the copper layer and the main aluminum layer, and by the thermal interface layer of 0.1 mm. The thermal resistance of the case-to-heatsink $R_{th,c-h}$ is the sum of four components in Eq. (9), which can be reduced to three, due to the very thin solder mask in Eq. (10):

$$R_{th,c-h} = \frac{d_{sold}}{K_{sold}\, S_{MOS}} + \frac{d_{ins}}{K_{ins}\, S_{MOS}} + \frac{d_{Al}}{K_{Al}\, S_{MOS}} + \frac{d_{th}}{K_t\, S_{MOS}}, \quad (9)$$

$$R_{th,c-h} = \frac{d_{ins}}{K_{ins}\, S_{MOS}} + \frac{d_{Al}}{K_{Al}\, S_{MOS}} + \frac{d_{th}}{K_{th}\, S_{MOS}}, \quad (10)$$

Table 6 MOSFET IPF067N20NM6 junction to case thermal network

$R_{th,i}$ (K/W)	$C_{th,i}$ (J/K)	τ_i (s)
2.519×10^{-2}	1.134×10^{-3}	2.451×10^{-5}
1.715×10^{-1}	8.009×10^{-3}	1.370×10^{-3}
2.996×10^{-1}	1.307×10^{-1}	3.916×10^{-2}

where d_{ins}, d_{Al}, and d_{th} are the thicknesses of the insulator, aluminum, and thermal interface substrate, respectively. The same applies to the thermal conductivities K_{ins}, K_{Al} and K_{th}. S_{MOS} is, instead, the MOSFET thermal pad. All thicknesses and thermal conductivity were taken equal to the references values in Ref. [23]: d_{ins} = 0.15 mm, d_{Al} = 1.5 mm and d_{th} = 0.1 mm; K_{ins} = 3 W/mK, K_{Al} = 237 W/mK and K_{th} = 1.6 W/mK. Therefore, the resultant thermal resistance for the part number considered is: $R_{th,c-h}$ = 1.167 K/W. The respective thermal capacitance is 0.4 J/K.

An algorithm was then implemented in MATLAB to compute the MOSFET switching losses based on the available datasheet information. The algorithm mentioned above based on Ref. [13] takes into account the non-linearity of the reverse-transfer capacitance C_{rss}, the non-linearity of the channel current I_{ch} during the rise and fall of currents in Eq. (11) and the parasitic inductances on the drain and source due to the type of package. In addition, reverse-recovery losses are estimated as in Ref. [24].

$$I_{ch} = k_1 \left(V_{GS} - V_{th}\right)^x + k_2 \,, \tag{11}$$

where k_1, k_2 and x are just coefficients that match the V_{GS}–I_{ch}, V_{GS} is the gate-source voltage and V_{th} is the turn-on threshold voltage. Switching losses, both on and off, depend on drain-source voltage V_{DS} and drain current I_D and on the device junction temperature T_j:

$$\begin{cases} E_{on} = E_{on}(V_{DS}, I_D, T_j) \\ E_{off} = E_{off}(V_{DS}, I_D, T_j) \end{cases} . \tag{12}$$

The output of the algorithm consists of two 3D look-up tables which can then be uploaded in PLECS. The algorithm finds E_{on} and E_{off} offline, and is based on the work in Ref. [13]. The software then simply evaluates the switching losses $P_{sw,MOSFET}$ as in Eq. (13) at each simulation step.

$$P_{sw,MOSFET} = \left(E_{on} + E_{off}\right) f_{sw} \,, \tag{13}$$

In Figures 12(a) and 12(b), these 3D look-up tables are shown. As a matter of clearance, the figures mentioned above refer to T_j = 175 °C, but tables for 25 °C are also uploaded in the thermal model.

Conduction losses are evaluated by uploading the datasheet $V_{DS} - I_D$ curve in PLECS. The entire motor drive architecture can also be modeled in PLECS to calculate the power losses produced by the inverter, in this work, ten MOSFETS are put in parallel. In Figure 13, the main schematic is presented. A 10 s simulation was carried out at 3000 rpm and with phase current, I_{ph}, of 600 A_{rms} to estimate the power losses caused by the device, in this overload condition. Results of the power losses, junction temperature oscil-

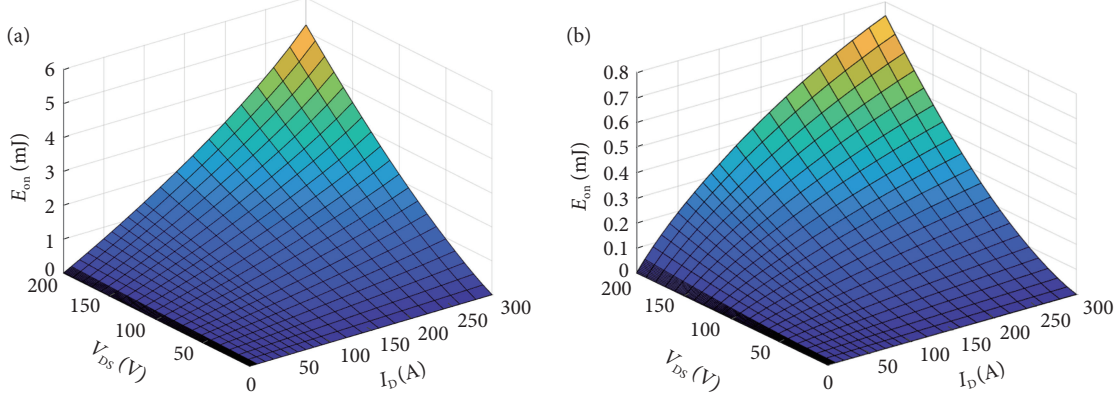


Figure 12 MATLAB script result. (a) E_{on} losses, and **(b)** E_{off} losses for MOSFET IPF067N20NM6.

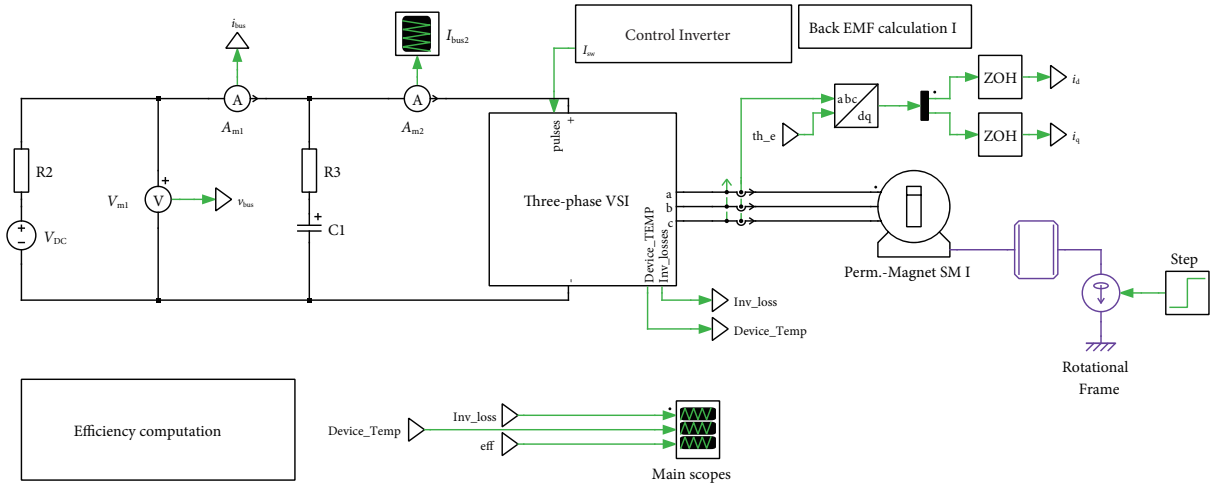


Figure 13 PLECS main schematic digital twin.

lation and efficiency are shown in Figure 14.

As can be seen, the power losses produced by the inverter are 1072 W when steady state is reached. The efficiency was calculated through the same PLECS simulation, taking into account that the electrical and thermal domains are separated in the software. Therefore, the following formula was applied[13]:

$$\eta = 1 - \frac{P_{\text{loss}}}{P_{\text{in}}}, \tag{14}$$

where P_{in} is the average input power over a switching period $1/f_{\text{sw}}$ and P_{loss} represents the sum of the power losses of each transistor of the inverter. As the junction temperature changes, the switching losses are automatically updated by the software according to the uploaded 3D look-up tables. A maximum temperature jump of 60 K was chosen for the heat sink with an ambient temperature of 40 °C, considering that the race could be held in summer; therefore, a thermal resistance lower than 0.06 K/W is sought. Another MATLAB script was implemented to size the heat sink. Calculations of the size of the heat sink followed the Refs. [25,26]: first a profile was selected, TRE-S 1319 and then its parameters were put into a MATLAB script to evaluate its heatsink-to-ambient thermal resistance $R_{\text{th,h-a}}$ for a given profile length. The main formulas employed are explained in the following sentences and they represent a simplified mathematical model for the heat-sink sizing under forced convection. As specified in Refs. [25,26], the process was iterated until the desired thermal resistance, $R_{\text{th,h-a}} \leqslant 0.06$ K/W was achieved, while maintaining acceptable air velocity and volumetric flow, taking into account the cooling effect provided by the motorbike during the race. Initially, the air speed V_{f} under forced convection must be sought through an iterative method and employing the following formula:

$$V_{\text{f}} = \sqrt{\frac{\frac{2\Delta P_{\text{hs}}}{\rho}}{K_{\text{e}} + 4f_{\text{app}}\frac{L}{2s} + K_{\text{c}}}}, \tag{15}$$

where ΔP_{hs} (N/m²) is the pressure drop that an equivalent fan could reach, L is the profile length (m), s is the spacing between fins, ρ is the air density (Kg/m³), K_{e} and K_{c} are pressure loss coefficients expressed as

$$\begin{cases} K_{\text{c}} = 0.4\,(1-\sigma^2) + 0.4 \\ K_{\text{e}} = (1-\sigma^2) - 0.4\sigma \end{cases}, \tag{16}$$

with $\sigma = \frac{s}{s+t}$, t is the fin thickness, and f_{app} is the apparent friction factor defined as

$$f_{\text{app}} = \frac{\sqrt{\left(\frac{3.44}{\sqrt{L/2s\,Re_{\text{Dh}}}}\right)^2 + f_{Re_{\text{Dh}}}^2}}{Re_{\text{Dh}}}, \tag{17}$$

where the hydraulic diameter is defined as $\text{Dh} \approx 2s$, and Re_{Dh} is the Reynolds number based on this hydraulic diameter and $f_{Re_{Dh}}$, accounts for the friction factor:

$$f_{Re_{Dh}} = \frac{24}{(1+s/H_{\text{f}})^2\left[1 - \frac{195s}{\pi^5 H_{\text{f}}}\tanh\left(\pi\frac{H_{\text{f}}}{2s}\right)\right]}, \tag{18}$$

where H_{f} is the fin height. A final check on the speed of the fluid is made to verify that it is reachable in this application, where the forced air does not come from a dedicated fan but from a duct. The same is verified for the volumetric air flow $\dot{V}_{\text{f}}$. Final steps to evaluate the heat sink thermal resistance are the computation of the average heat transfer coefficient of the heat sink h, through:

$$h = \frac{k_{\text{f}} Nu_{\text{s}}}{s}, \tag{19}$$

where Nu_{s} is the average Nusselt number for the heatsink and is defined as

$$Nu_{\text{s}} = \frac{\tanh\left(\sqrt{2\,Nu_{\text{i}}\frac{k_{\text{f}}}{k}\frac{H_{\text{f}}}{s}\frac{H_{\text{f}}}{t}}\right)\left(\frac{t}{L}+1\right)}{\sqrt{2\,Nu_{\text{i}}\frac{k_{\text{f}}}{k}\frac{H_{\text{f}}}{s}\frac{H_{\text{f}}}{t}\left(\frac{t}{L}+1\right)}}\,Nu_{\text{i}}, \tag{20}$$

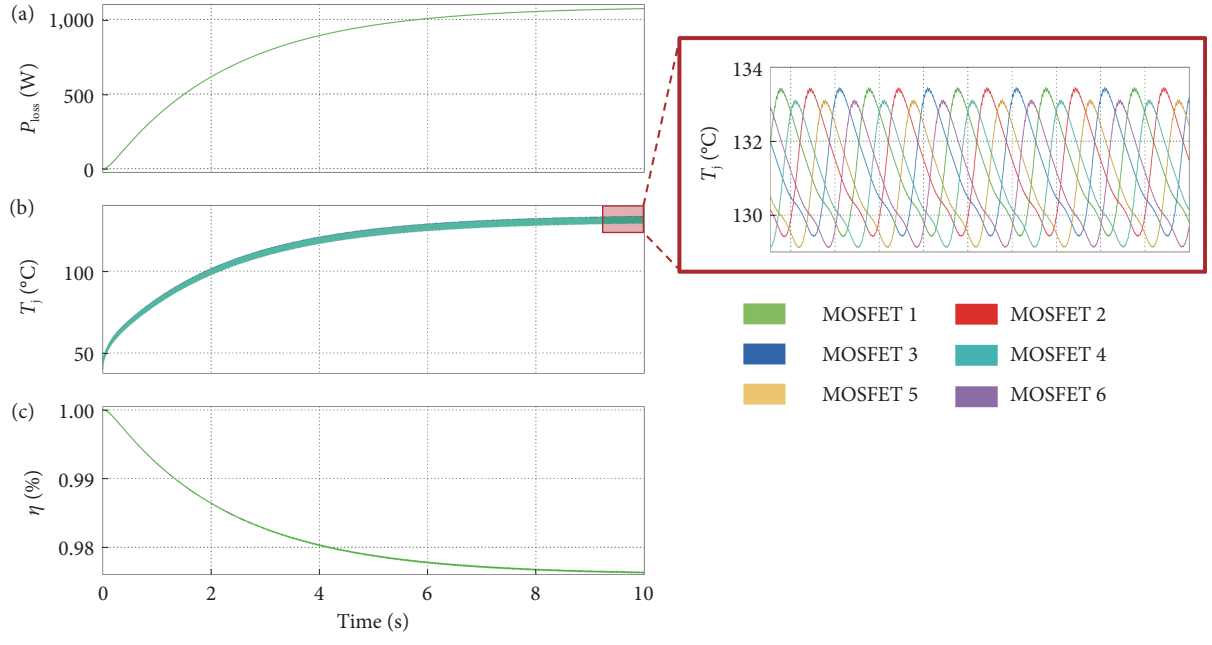


Figure 14 Heat sink sizing simulation results. (a) Inverter losses P_{loss}, **(b)** MOSFET junction temperature T_{j}, and **(c)** inverter efficiency. (3000 rpm and 130 Nm simulation).

where k and k_f are heat sink material thermal conductivity in $W/(m \cdot K)$ of aluminum and air, respectively, and Nu_i is the local Nusselt number, defined as

$$Nu_i = \left[\left(\frac{Re_s s/LPr}{2}\right)^{-3} + \left(0.664\sqrt{Re_s s/LPr^{1/3}}\sqrt{1+\frac{3.65}{\sqrt{Re_s s/L}}}\right)\right]^{-1/3}. \quad (21)$$

Pr is the Prandtl number of the cooling air. Finally the thermal resistance is evaluated by substituting Eqs. (20) and (21) in Eq. (19) and using it in Eq. (22):

$$R_{th,h-a} = \frac{1}{h\,A_{hs}} + \frac{b}{k\,W\,L}, \quad (22)$$

where b is the base height, W is the heat sink width and A_{hs} is the wetted surface of the heat sink and it's expressed in Eq. (23).

$$A_{hs} = L\,(s+2H_f)\,(N_f-1). \quad (23)$$

In Table 7, the main parameters of the TRE-S PRO1319 heat sink are listed, meanwhile, in Figure 15, a summary of the thermal chain composition is shown.

A more advanced optimization, to which the author refers, has been carried out in Ref. [27]. Here we applied a Pareto optimization to minimize the weight of the heat-sink and overall inverter, employing microchannel plates.

Table 7 TRE-S PRO1319 profile heat sink main parameters

Parameter	Symbol	Value	Unit
Height	H	4	mm
Base height	b	14	mm
Width	W	200	mm
Length	L	240	mm
Number of fins	N_f	42	/
Fin thickness	t	1.6	mm
Fin spacing	s	2.9	mm
Reynolds number (hydraulic diameter)	Re_{Dh}	1488.5	/
Air speed	V_f	4.61	m/s
Volumetric air flow	$\dot{V}_f$	0.0219	m^3/s
Thermal resistance	$R_{th,h-a}$	0.0572	K/W
Estimated thermal capacitance	$C_{th,h-a}$	3200	J/K

4 Mechanical design

The converter design employs a compact three-PCB stack architecture to optimize both functionality and spatial efficiency. At the base of the stack lies the power IMS board. Above this, the middle layer consists of the DC-bus board and on the top of the stack sits the logic and driver control PCB, embedded within the center of the capacitor layout, minimizing the overall height of the converter. The converter employs a total of seven busbars three for the AC phases and four for the DC-bus, two for $+V_{DC}$ and two for PGND. The DC busbars provide connection between DC-bus board and the IMS board, while the phase busbars bring the three phases from the power board to the external connectors of the inverter. The power connections between the two power boards are performed by means of connection legs on the busbars as it is possible to see in Figure 16. The cross-section of each busbar is determined by the maximum continuous current it must carry, which in this design is 450 A_{rms}. Given the compact nature of the converter, a high current density of 5 A_{rms}/mm^2 was selected, which led to the determination of a required busbar cross-section of 90 mm^2. To ensure reliable and isolated attachment to the heatsink, each busbar is designed with three holes for plastic isolators and screws, as shown in Figure 16. Furthermore, to facilitate enable connections of the AC and DC power rails, welded radserts, high-performance contact inserts engineered to minimize contact resistance, are integrated directly into the busbars.

The converter's external enclosure is designed as a single 3D-printed unit to provide protection against dust and water infiltration. Finally, waterproof external power connectors with gasket-based sealing are employed, and the entire housing is securely mounted to the heatsink, ensuring mechanical integrity (Figure 17).

5 Lifetime assessment

Lifetime assessment in a three-phase inverter involves evaluating the durability and reliability of its components, in particular power semiconductors, capacitors, and thermal interfaces, under varying electrical and thermal stresses over time. The assessment typically focuses on factors such as temperature cycling, power cycling, and voltage transients, which can cause degradation and eventual failure of critical parts. Failure models and thermal simulations based on mission profiles are employed to predict the remaining useful life of the inverter. Accurate lifetime estimation is essential to ensure the long-term performance, safety, and maintenance planning of power electronic systems in applications such as EVs. The procedure to estimate the reliability of the converter is based on

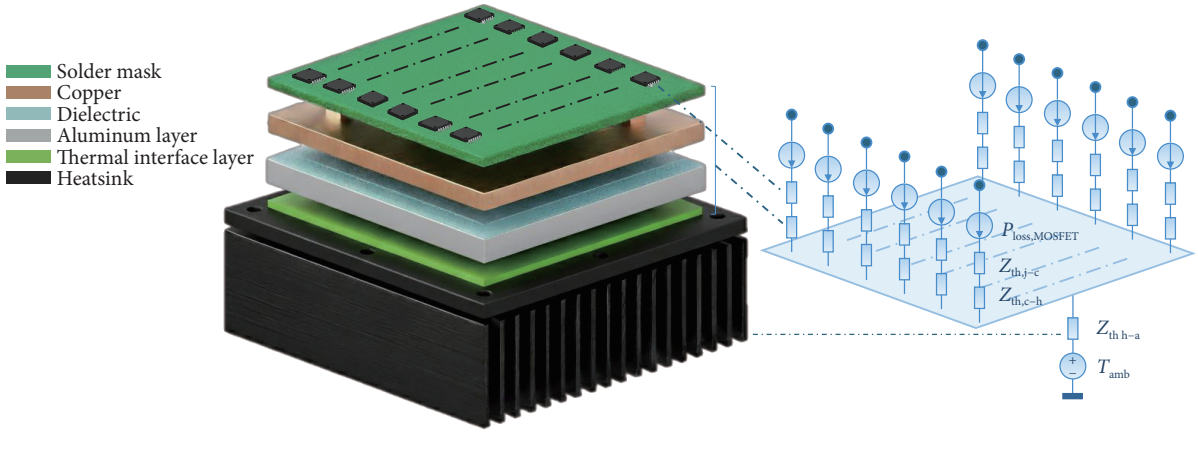


Figure 15 Inverter thermal chain.

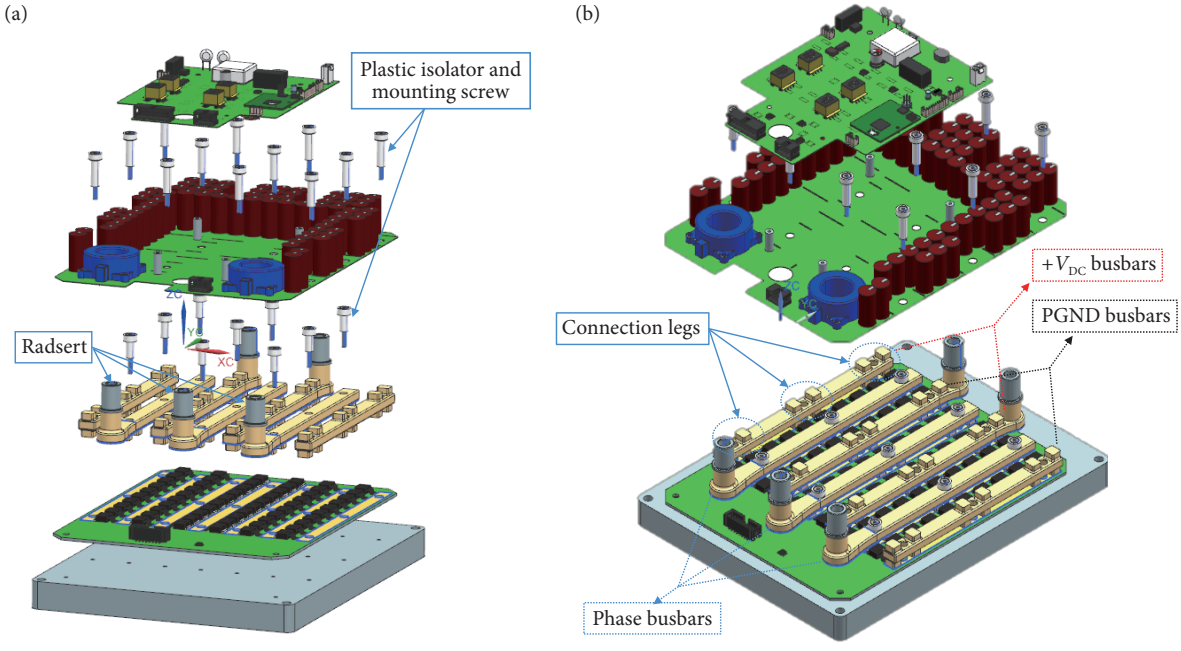


Figure 16 **Internal structure exploded view.**

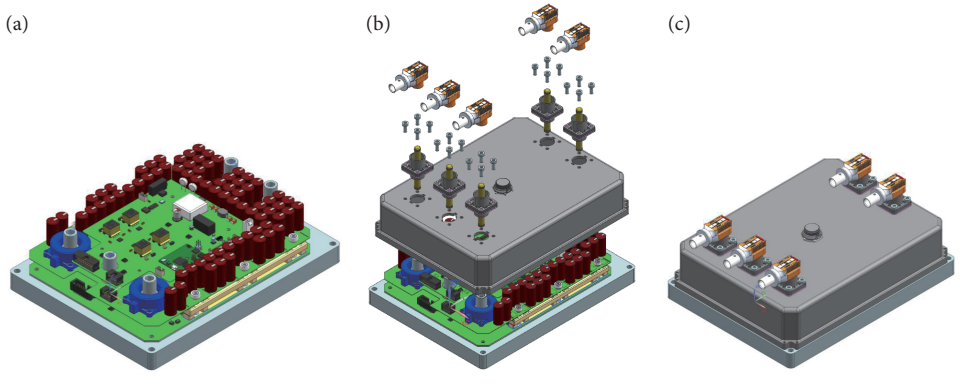


Figure 17 **(a)** Inverter internal assembly, **(b)** external structure exploded view, and **(c)** full inverter assembly.

Refs. [7, 28]. The core objective is to determine life consumption over a mission profile cycle using a data-driven lifetime model. The mission profile, presented in Figure 18, was obtained from a full race log recorded at the Motorland of Aragon circuit in Spain. The relevant signals include the phase current, DC-link voltage, motor speed, and heat-sink temperature.

A combined loss-thermal model initially estimates the MOSFET's junction temperature along with its fluctuations throughout the cycle. These thermal stress parameters are then used as inputs for the lifetime model, which calculates the resulting damage accumulation. To incorporate uncertainties in both model parameters and thermal stresses, a Monte Carlo analysis is subsequently performed. This analysis generates a probability density function (PDF) based on the Weibull distribution, providing the lifetime distribution of the devices. Finally, the cumulative density function (CDF) of the Weibull distribution is applied to assess the inverter's reliability at the system level. The described procedure is summarized in Figure 19.

5.1 MOSFET junction temperature evaluation

To estimate the junction temperature of the devices a PLECS simulation was conducted based on the mission profile. A traditional simulation using the inverter schematic and a control algorithm was not feasible due to the length of the mission profile and the required time-step; therefore, a different approach is proposed. The simplified simulation leverages key input signals, namely, the phase current, DC-bus voltage, and heat-sink temperature, to reconstruct the instantaneous current passing through each of the MOSFETs in the inverter's power stage and to finally compute the junction temperature. The phase current waveform is obtained through Eq. (24):

$$I_{ph}(t) = \sqrt{2}\sin\left(\int_0^T 2\pi\,\frac{n\mathrm{PP}}{60}\mathrm{d}t + \varphi\right) = \sqrt{2}\sin\left(\theta_{el} + \varphi\right), \quad (24)$$

where n is the motor speed in rpm, PP are the pole pairs. The current through each MOSFET is calculated by comparing the modeled phase current with a triangular waveform, and the resulting signal is then divided by the number of parallel MOSFETs, as shown in Figure 20.

The MOSFET current, along with the DC-link voltage and the estimated junction temperature feedback, are the inputs of two lookup tables (LUTs), computed in Section 3, to calculate the conduction and switching losses. The MOSFET power losses then serve as the input for the thermal network model in Figure 21. This model, which integrates manufacturer data for junction-to-case thermal impedance and the system's case-to-heat-sink char-

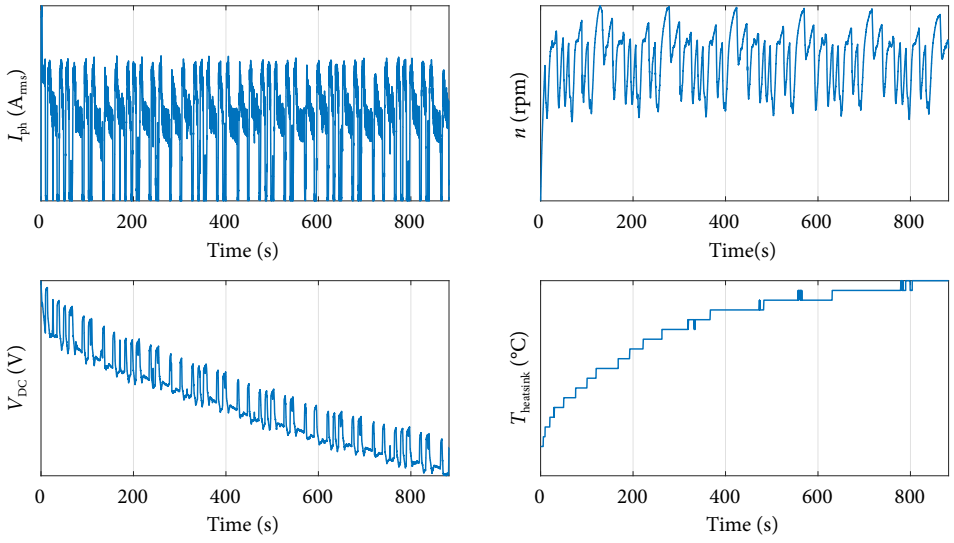


Figure 18 Mission profile data recorded during a session at the Motorland of Aragon circuit. (**a**) Phase current I_{ph}, (**b**) motor speed n, (**c**) DC-bus voltage V_{DC}, and (**d**) heat-sink temperature $T_{heatsink}$. These signals are used as input for the loss-thermal model.

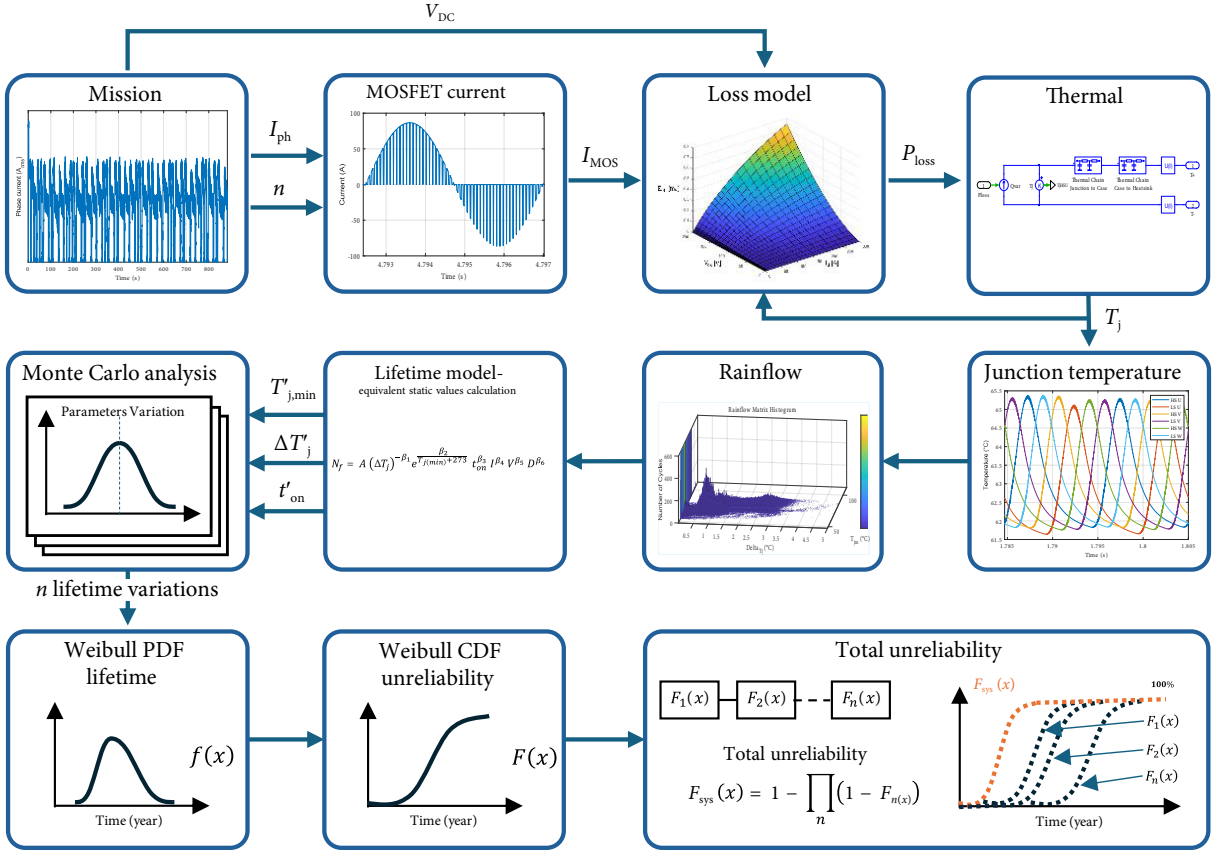


Figure 19 Lifetime assessment workflow.

acteristics (from Section 4), allows for the dynamic calculation of the junction temperature over time, accurately capturing thermal responses to varying loads, see the oscillation examples of T_j in Figure 22.

5.2 Reliability analysis

In this section, the reliability analysis of the converter is investigated. Firstly, the lifetime estimation is performed on the designed converter with 10 MOSFETs in parallel (N_p = 10) and with the race mission profile. A comparative analysis is then conducted to determine the change in inverter lifetime when the mission profile is overloaded by 25% and 50%, maintaining N_p constant. In addition, the effects of the reduction of the number of parallel MOSFETs on the lifetime are considered, selecting N_p = 8 and then N_p = 6. Since the degradation of MOSFETs is related to the thermal stress cycles to which they are subjected a rainflow counting algorithm is performed on the junction temperature trend derived in Section 5.1. Rainflow analysis returns the number of cycles n_i, which are related to a given peak-to-peak junction temperature variation ΔT_j, and a mean junction temperature,

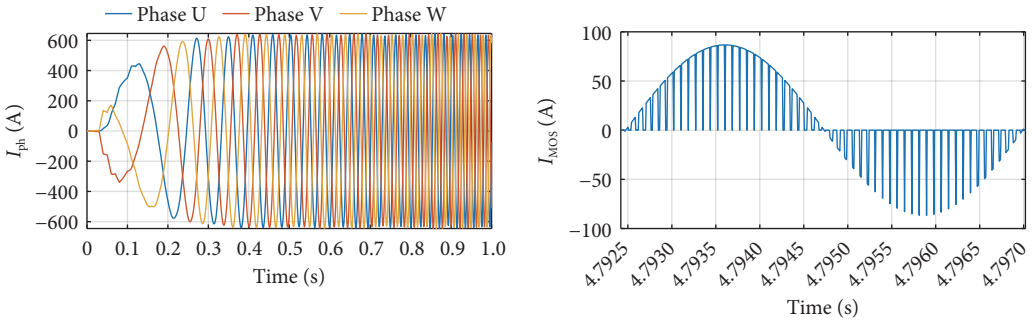


Figure 20 Generated phase current from the RMS value and the speed of the motor in rpm. (a) Variable frequency three-phase sinusoidal current waveforms (I_{ph}), and **(b)** current passing through each MOSFET (I_{MOS}), when eight MOSFETs are placed in parallel.

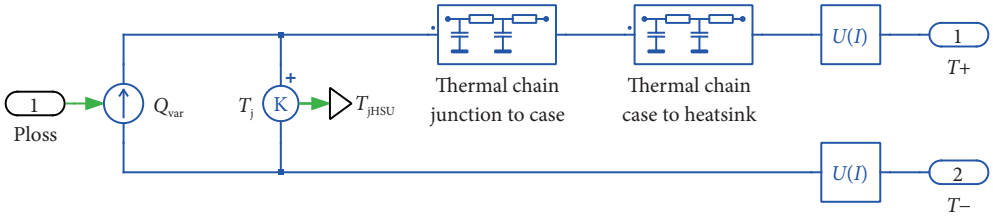


Figure 21 Thermal chain from the junction to heat-sink in order to compute the junction temperature.

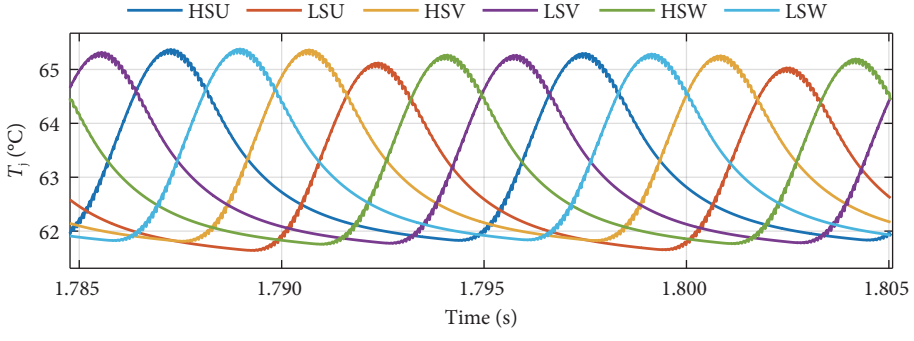


Figure 22 Junction temperature T_j of the high-side (HS) and low-side (LS) MOSFET of the three legs with the simplified simulation.

$T_{j,mean}$. In Figure 23, the set of rainflow diagrams is shown for each combination of N_p = {6, 8, 10} and load condition: rated mission profile, +25% and +50% overload. The lifetime model (i.e., CIPS2008)[7] as shown in Eq. (25) was originally developed for Si IGBT modules[29].

$$N_f = A\,(\Delta T_j)^{\beta_1}\,e^{\frac{\beta_2}{T_{j(min)}+273}}\,t_{on}^{\beta_3}\,I^{\beta_4}\,V^{\beta_5}\,D^{\beta_6}, \tag{25}$$

Moreover, the model coefficients provided in Ref. [7] pertain to an IGBT module with entirely different specifications. A detailed overview of the existing lifetime models and their parameters has been provided in Ref. [30]. However, it is important to recognize that existing models and their published parameters are based on specific assumptions and limited experimental conditions, which limit their broad applicability. As demonstrated in the comparative study in Ref. [31], using an inappropriate lifetime model can result in predictions that deviate by up to two orders of magnitude. To deal with this concern, in Ref. [8] a generic lifetime model is proposed. A key difficulty in lifetime prediction is the lack of suitable models for new chip and packaging technologies. To address this, authors collected over 200 testing results from the literature and developed a generic lifetime model using regression techniques. Given that some parameters, such as bond wire diameter and quantity, are often unavailable in practice, the model is formulated in a simplified form based on the CIPS2008 model as shown in Eq. (26):

$$N_f = A\,\Delta T_j^{-n}\,e^{\frac{\beta_1}{T_{j,max}+273}}\,t_{on}^{\beta_2}, \tag{26}$$

where ΔT_j, $T_{j,max} = T_{j,mean} + \Delta T_j/2$, and the heating time t_{on} come from rainflow counting (Figure 23). The parameters of Eq. (26), summarized in the Table 8, were selected from those available in Ref. [8], based on a silicon device with aluminum bond wires and a silver sintered die attach.

With the results of the rainflow counting, it is possible to compute the lifespan of the power devices. The operational lifespan is typically quantified as LC (lifetime consumption) that measures the fraction of the MOSFET total life consumed during operation. For this study, the LC is calculated using a widely adopted Miner's rule-based damage model[32], expressed in Eq. (27):

$$LC = \sum_i \frac{n_i}{(N_f)_i}, \tag{27}$$

where n_i represents the number of cycles for a given thermal stress, output of the rainflow diagram and $(N_f)_i$ is the number of cycles to failure for the same thermal stress. Eq. (27) supposes independency of each thermal loading event.

The uncertainty in the model parameters, such as the material properties and the estimated junction temperature, is addressed through a Monte Carlo analysis, where these parameters are varied through a normal distribution to generate a range of potential outcomes. The Monte Carlo analysis requires consideration of

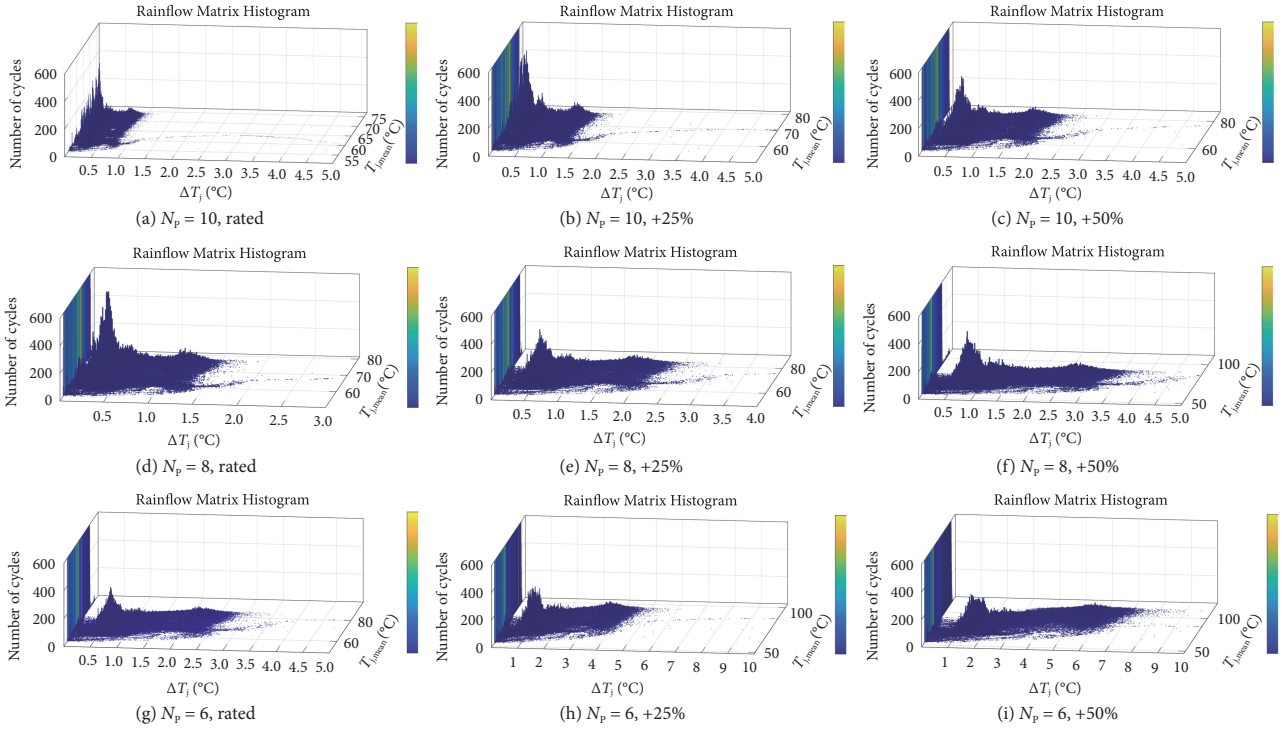


Figure 23 Rainflow diagrams for different number of parallels (N_p) and load conditions.

Table 8 General lifetime model parameters

A	n	β_1	β_2
1.14×10^9	3.12	2402	−0.39

varying thermal loads ($T_{j,min}$, ΔT_j and t_{on}). These are simplified through the calculation of equivalent static values, yielding a single constant that represents the overall loading history[7]. The simulation is performed on a set of 10 000 samples with a confidence level of 99% and a variation percentage of 5%. Using the derived parameter variations, the lifetime distribution of the power devices is established and can be represented by a weibull PDF. The corresponding CDF, often referred to as the unreliability function, then allows for the evaluation of the inverter's reliability at both the component and system levels. Based on this analysis, the predicted life of the device or system is expressed in terms of B_x lifetime, which is the operating time at which there is an x% probability of failure. In this paper, it is assumed that a single MOSFET failure, would result in malfunction and a forthcoming failure of the whole converter. A damaged MOSFET causes an unbalanced current distribution among the healthy components leading to a system level fault condition. Therefore, the system-level reliability analysis is done with a series connection[33] of the component-level reliability block diagram (RBD), as shown in Figure 24. The total unreliability of the system, $F_{sys}(x)$, is ultimately derived from the unreliability of its components. This relationship is defined by Eq. (28), where $F_i(x)$ is the unreliability function of the i-th device in the inverter:

$$F_{sys}(x) = 1 - \prod_{i=1}^{n} (1 - F_i(x)) \tag{28}$$

Figure 25 shows a comparison of the obtained lifetime estimation related to the case studies presented in Figure 23, and in Table 9, the B_1 for the different cases is presented. B_1 is a useful parameter that represents the lifetime corresponding to a 1% probability of system failure. Since all the components considered for the reliability evaluation are connected in series, the system level unreliability is computed as follows:

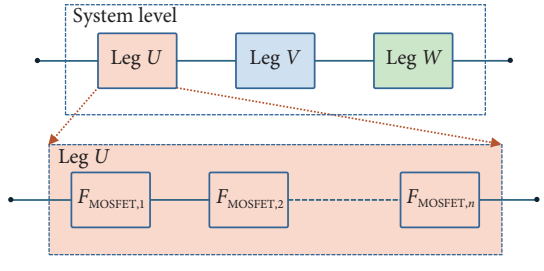
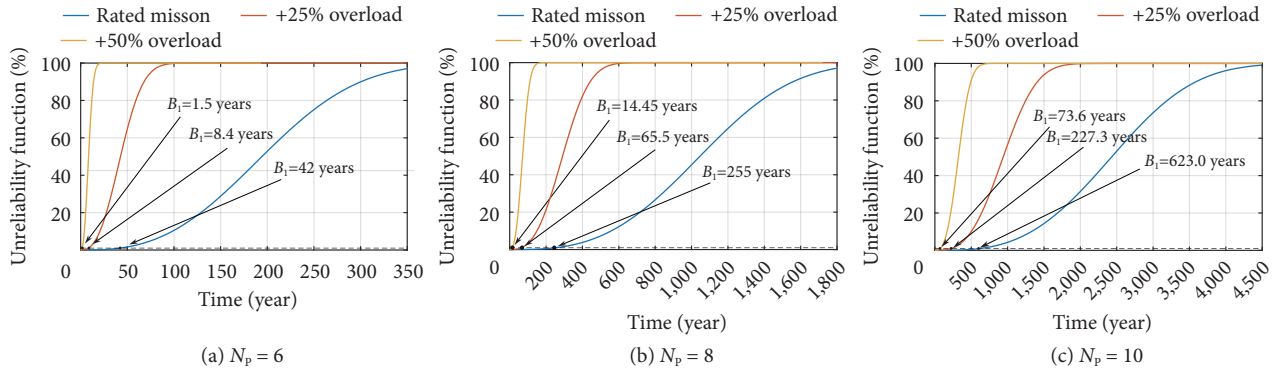


Figure 24 RBD of the complete system, due to the assumption a single fault causes the damage of all the converter, all the components are considered in series.

$$F_{sys}(x) = 1 - (1 - F_{MOSFET})^{N_{MOSFET}}, \tag{29}$$

where F_{MOSFET} is the unreliability of a single MOSFET computed through the CDF of the Weibull distribution and N_{MOSFET} is the total number of MOSFETs obtained by multiplying 6 switches required for the topology by the number of parallels N_p.

Assuming 250 operating hours per year, including testbench, validation, and final race event, the expected lifetimes are presented in Table 9. As detailed in Section 2.1, the converter has been intentionally oversized; as a result, its life consumption under the rated mission profile, with 10 MOSFETs in parallel, remains quite low. As a consequence, the results obtained for configurations with 10 and 8 parallels under rated load and +25% overload (Figure 25) are high due to the low electrical and thermal stress imposed and the reduced usage time. However, it is worth noting that increasing the load as well as reducing the number of parallel MOSFETs leads to a decrease in lifetime as expected, proving the consistency of the model. With six parallel devices, the lifetime results at the rated load are acceptable; however, under a 50% overload cycle, the lifetime drops to B_1 = 1.5 years, which was deemed unacceptable. Increasing the number of parallel MOSFETs to N_p = 8 significantly improves the results, with the lifetime



(a) $N_P = 6$ (b) $N_P = 8$ (c) $N_P = 10$

Figure 25 Lifetime unreliability functions for the case analysis.

Table 9 B_1 in years comparison for the different load conditions

B_1	Rated load	+25% overload	+50% overload
$N_p = 6$	42	8.4	1.5
$N_p = 8$	255	65.5	14.5
$N_p = 10$	623	227.3	73.6

remaining high even under a +50% overload. Considering that the additional cost of 12 MOSFETs (4 per leg) was feasible, a further increase to $N_p = 10$ was selected for the final design to accommodate potential higher overloads and account for uncertainties in the lifetime model.

6 Future improvements

Future developments will focus on optimizing the converter design by leveraging the findings of this paper to create a smaller, more cost-effective solution tailored to the specific mission profile and motorsport requirements for high power density. By analyzing the system's operational demands and simulation results, it becomes possible to reduce the number of parallels without compromising performance while maintaining an acceptable lifetime, resulting in a lighter and economically viable design. An integral part of this optimization includes accurate capacitor lifetime estimation, which will be performed following the same workflow described in this paper. A further step to improve the accuracy of the simulations is to tailor the lifetime model parameters specifically to the selected device through accelerated aging tests. By aligning the model parameters with the real characteristics and behavior of the chosen device, the resulting predictions of degradation and failure mechanisms will be significantly more reliable. Another future work is the evaluation of the impact of the bearing current in our system and design a suitable countermeasure. As stated in Ref. [34] in inverter-fed drive systems, bearing currents are primarily induced by the common-mode voltage generated by the inverter. Due to the motor's parasitic parameters, a portion of the high-frequency common-mode voltage couples through the parasitic capacitance between the stator windings and the rotor, producing a bearing voltage across the bearing. When this bearing voltage exceeds a critical threshold, high-frequency bearing currents are generated. However, in this application, where the battery pack voltage is limited to 126 V, this effect can be reduced and may not require additional suppression measures such as passive filters or particular PWM modulation techniques.

7 Conclusions

This paper presents a detailed analysis and design of a low-voltage, high-current voltage source inverter tailored for competitive motorsport applications. A comprehensive lifetime assessment methodology was integrated as a core component of the converter design process. A notable contribution of this work is the use of a switching loss model, rather than relying solely on datasheet curves, as the initial step in the lifetime evaluation workflow, enabling a more realistic assessment of device longevity. The study includes in-depth analysis often overlooked in similar works, such as a detailed evaluation of the thermal path from the transistor junction to ambient. The proposed methodology is applicable to any parallelized inverter design that considers converter lifetime. Simulation results indicate that increasing the number of parallel devices yields significant lifetime improvements. Specifically, increasing from $N_p = 6$ to $N_p = 10$ under a 50% overload condition led to an improvement from 1.5 to 73.6 years. Furthermore, based on the results reported in Table 9 of Section 5.2, it can be observed that the use of 10 MOSFETs is not strictly necessary. Depending on the operating condition of interest and the specific application, the use of 6 MOSFETs may be sufficient. This leads to a reduction in the converter's volume and weight of about 30%, thereby increasing the power density while maintaining the same output power required by the mission profile. With six parallel MOSFETs, the peak power handling capability is reduced; therefore, the required DC-link capacitance is lower. As a result, the number of DC-link capacitors can be reduced from a minimum of 56 in the $N_p = 10$ case to a minimum of 38. The removal of four MOSFETs also shortens the power board by approximately 4 cm, which in turn allows the heatsink size to be reduced as well. However, the design choice was to use 10 parallel devices for this first prototype, as the additional cost was acceptable and offered further reliability margin. It is important to note that this lifetime model only accounts for electrical failure modes; other potential failure sources remain unaddressed and should be considered as part of a broader design validation strategy. Future work will focus on a more cost-effective optimization based on the specific race load profile, as well as the development of a physical prototype. This will allow alignment between the modeled and actual system parameters, and enable evaluation of deviations from the predicted performance.

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Additional information

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Declaration of competing interest

The authors have no competing interests to declare that are relevant to the content of this article.

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